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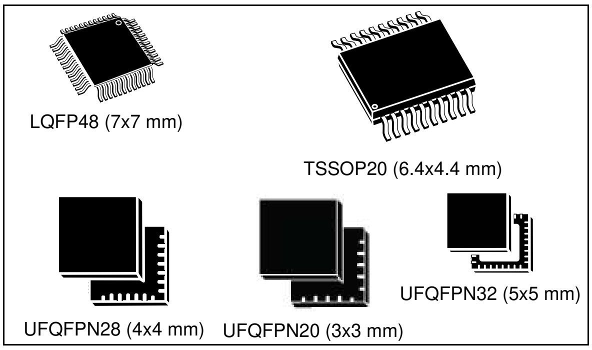
STM8L151C2/K2/G2/F2
STM8L151C3/K3/G3/F3

8-bit ultra-low-power MCU, up to 8 KB Flash, up to 256 B data EEPROM, RTC, timers, USART, I2C, SPI, ADC, comparators

Datasheet - production data

Features

- Operating conditions
  - Operating power supply: 1.65 to 3.6 V (without BOR), 1.8 to 3.6 V (with BOR)
  - Temperature range: -40 to 85 or 125 °C
- Low power features
  - 5 low-power modes: Wait, Low power run, Low-power wait, Active-halt with RTC, Halt
  - Ultra-low leakage per I/0: 50 nA
  - Fast wakeup from Halt: 5 µs
- Advanced STM8 core
  - Harvard architecture and 3-stage pipeline
  - Max freq: 16 MHz, 16 CISC MIPS peak
  - Up to 40 external interrupt sources
- Reset and supply management
  - Low-power, ultra safe BOR reset with 5 selectable thresholds
  - Ultra-low power POR/PDR
  - Programmable voltage detector (PVD)
- Clock management
  - 32 kHz and 1-16 MHz crystal oscillators
  - Internal 16 MHz factory-trimmed RC
  - Internal 38 kHz low consumption RC
  - Clock security system
- Low power RTC
  - BCD calendar with alarm interrupt
  - Digital calibration with +/- 0.5 ppm accuracy
  - LSE security system
  - Auto-wakeup from Halt w/ periodic interrupt
- Memories
  - Up to 8 Kbyte of Flash program memory plus 256 byte of data EEPROM with ECC
  - Flexible write/read protection modes
  - 1 Kbyte of RAM



- DMA
  - 4 channels supporting ADC, SPI, I^{2}C, USART, timers
  - 1 channel for memory-to-memory
- 12-bit ADC up to 1 Msps/28 channels
  - Temp. sensor and internal ref. voltage
- 2 ultra-low-power comparators
  - 1 with fixed threshold and 1 rail to rail
  - Wakeup capability
- Timers
  - Two 16-bit timers with 2 channels (IC, OC, PWM), quadrature encoder (TIM2, TIM3)
  - One 8-bit timer with 7-bit prescaler (TIM4)
  - 1 Window and 1 independent watchdog
  - Beeper timer with 1, 2 or 4 kHz frequencies
- Communication interfaces
  - One synchronous serial interface (SPI)
  - Fast I^{2}C 400 kHz
  - One USART
- Up to 41 I/Os, all mappable on interrupt vectors
- Up to 20 capacitive sensing channels supporting touchkey, proximity touch, linear touch, and rotary touch sensors
- Development support
  - Fast on-chip programming and non-intrusive debugging with SWIM
  - Bootloader using USART
- 96-bit unique ID

Contents

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1 Introduction

This document describes the features, pinout, mechanical data and ordering information for the low-density STM8L151x2/3 devices: STM8L151x2 and STM8L151x3 microcontrollers with a Flash memory density of up to 8 Kbyte.

For further details on the STMicroelectronics ultra-low-power family please refer to *Section 2.2: Ultra-low-power continuum on page 13*.

For detailed information on device operation and registers, refer to the reference manual (RM0031).

For information on to the Flash program memory and data EEPROM, refer to the programming manual (PM0054).

For information on the debug module and SWIM (single wire interface module), refer to the STM8 SWIM communication protocol and debug module user manual (UM0470).

For information on the STM8 core, refer to the STM8 CPU programming manual (PM0044).

Low-density devices provide the following benefits:

- Integrated system
  - Up to 8 Kbyte of low-density embedded Flash program memory
  - 256 byte of data EEPROM
  - 1 Kbyte of RAM
  - Internal high-speed and low-power low speed RC.
  - Embedded reset
- Ultra-low-power consumption
  - 1 µA in Active-halt mode
  - Clock gated system and optimized power management
  - Capability to execute from RAM for Low power wait mode and Low power run mode
- Advanced features
  - Up to 16 MIPS at 16 MHz CPU clock frequency
  - Direct memory access (DMA) for memory-to-memory or peripheral-to-memory access.
- Short development cycles
  - Application scalability across a common family product architecture with compatible pinout, memory map and modular peripherals.
  - Wide choice of development tools

STM8L ultra-low-power microcontrollers can operate either from 1.8 to 3.6 V (down to 1.65 V at power-down) or from 1.65 to 3.6 V. They are available in the -40 to +85 °C and -40 to +125 °C temperature ranges.

These features make the STM8L ultra-low-power microcontroller families suitable for a wide range of applications:

- Medical and hand-held equipment
- Application control and user interface
- PC peripherals, gaming, GPS and sport equipment
- Alarm systems, wired and wireless sensors
- Metering

The devices are offered in five different packages from 20 to 48 pins. Different sets of peripherals are included depending on the device. Refer to *Section 3* for an overview of the complete range of peripherals proposed in this family.

All STM8L ultra-low-power products are based on the same architecture with the same memory mapping and a coherent pinout.

Figure 1 shows the block diagram of the STM8L low-density family.

2 Description

The low-density STM8L151x2/3 ultra-low-power devices feature an enhanced STM8 CPU core providing increased processing power (up to 16 MIPS at 16 MHz) while maintaining the advantages of a CISC architecture with improved code density, a 24-bit linear addressing space and an optimized architecture for low power operations.

The family includes an integrated debug module with a hardware interface (SWIM) which allows non-intrusive in-application debugging and ultrafast Flash programming.

All low-density STM8L151x2/3 microcontrollers feature embedded data EEPROM and low-power low-voltage single-supply program Flash memory.

The devices incorporate an extensive range of enhanced I/Os and peripherals, a 12-bit ADC, two comparators, a real-time clock, two 16-bit timers, one 8-bit timer, as well as standard communication interfaces such as an SPI, an I^2C interface, and one USART. The modular design of the peripheral set allows the same peripherals to be found in different ST microcontroller families including 32-bit families. This makes any transition to a different family very easy, and simplified even more by the use of a common set of development tools.

2.1 Device overview

Table 1. Low-density STM8L151x2/3 low power device features and peripheral counts

Features		STM8L151F3	STM8L151G3	STM8L151K3/ STM8L151C3	STM8L151F2	STM8L151G2	STM8L151K2/ STM8L151C2
Flash (Kbyte)		8			4		
Data EEPROM (byte)		256					
RAM (Kbyte)		1					
Timers	Basic	1 (8-bit)					
	General purpose	2 (16-bit)					
Commun -ication interfaces	SPI	1					
	I2C	1					
	USART	1					
GPIOs		18 (1)	26 (1)	30(2)/41(1)(2)	18 (1)	26 (1)	30(2)/41(1)(2)
12-bit synchronized ADC (number of channels)		1 (10)	1 (18)	1 (23/28)(3)	1 (10)	1 (18)	1 (23/28)(3)
Comparators (COMP1/COMP2)		2					
Others		RTC, window watchdog, independent watchdog, 16-MHz and 38-kHz internal RC, 1- to 16-MHz and 32-kHz external oscillator					
CPU frequency		16 MHz					
Operating voltage		1.8 to 3.6 V (down to 1.65 V at power-down) with BOR 1.65 to 3.6 V without BOR					
Operating temperature		– 40 to +85 °C / – 40 to +125 °C					
Packages		TSSOP20 UFQFPN20	UFQFPN28	UFQFPN32 LQFP48	TSSOP20 UFQFPN20	UFQFPN28	UFQFPN32 LQFP48

1. The number of GPIOs given in this table includes the NRST/PA1 pin but the application can use the NRST/PA1 pin as general purpose output only (PA1).
2. 26 GPIOs in the STM8L151K3 and 40 GPIOs in the STM8L151C3.
3. 22 channels in the STM8L151K3 and 28 channels in the STM8L151C3.

2.2 Ultra-low-power continuum

The ultra-low-power low-density STM8L151x2/3 devices are fully pin-to-pin, software and feature compatible. Besides the full compatibility within the family, the devices are part of STMicroelectronics microcontrollers ultra-low-power strategy which also includes STM8L101xx and STM8L15xxx. The STM8L and STM32L families allow a continuum of performance, peripherals, system architecture, and features.

They are all based on STMicroelectronics 0.13 µm ultra-low leakage process.

Note: 1 The STM8L151xx and STM8L152xx are pin-to-pin compatible with STM8L101xx devices.

Performance

All families incorporate highly energy-efficient cores with both Harvard architecture and pipelined execution: advanced STM8 core for STM8L families and ARM® Cortex®-M3 core for STM32L family. In addition specific care for the design architecture has been taken to optimize the mA/DMIPS and mA/MHz ratios.

This allows the ultra-low-power performance to range from 5 up to 33.3 DMIPs.

Shared peripherals

STM8L151xx/152xx and STM8L15xxx share identical peripherals which ensure a very easy migration from one family to another:

- Analog peripherals: ADC1 and comparators COMP1/COMP2
- Digital peripherals: RTC and some communication interfaces

Common system strategy

To offer flexibility and optimize performance, the STM8L151xx/152xx and STM8L15xxx devices use a common architecture:

- Same power supply range from 1.8 to 3.6 V, down to 1.65 V at power down
- Architecture optimized to reach ultra-low consumption both in low power modes and Run mode
- Fast startup strategy from low power modes
- Flexible system clock
- Ultra-safe reset: same reset strategy for both STM8L15x and STM32L15xxx including power-on reset, power-down reset, brownout reset and programmable voltage detector.

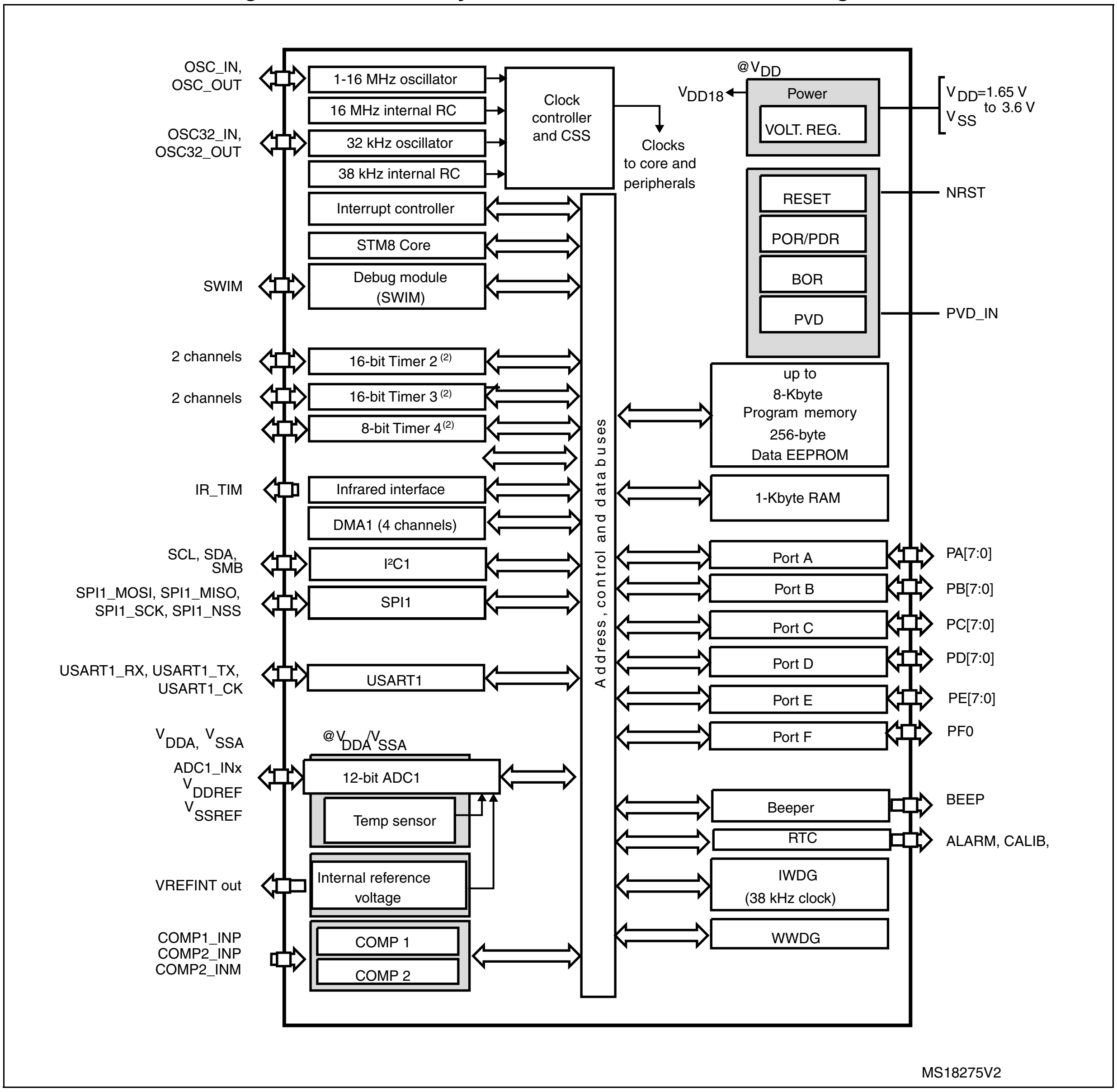
Features

ST ultra-low-power continuum also lies in feature compatibility:

- More than 10 packages with pin count from 20 to 100 pins and size down to 3 x 3 mm
- Memory density ranging from 4 to 128 Kbyte

3 Functional overview

Figure 1. Low-density STM8L151x2/3 device block diagram



1. **Legend**:
   ADC: Analog-to-digital converter
   BOR: Brownout reset
   DMA: Direct memory access
   I²C: Inter-integrated circuit multi master interface
   IWDG: Independent watchdog
   POR/PDR: Power on reset / power down reset
   RTC: Real-time clock
   SPI: Serial peripheral interface
   SWIM: Single wire interface module
   USART: Universal synchronous asynchronous receiver transmitter
   WWDG: Window watchdog
2. There is no TIM1 on STM8L151x2, STM8L151x3 devices.

3.1 Low-power modes

The low-density STM8L151x2/3 devices support five low power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Wait mode**: The CPU clock is stopped, but selected peripherals keep running. An internal or external interrupt or a Reset can be used to exit the microcontroller from Wait mode (WFE or WFI mode). Wait consumption: refer to *Table 20*.
- **Low power run mode**: The CPU and the selected peripherals are running. Execution is done from RAM with a low speed oscillator (LSI or LSE). Flash and data EEPROM are stopped and the voltage regulator is configured in ultra-low-power mode. The microcontroller enters Low power run mode by software and can exit from this mode by software or by a reset.
  All interrupts must be masked. They cannot be used to exit the microcontroller from this mode. Low power run mode consumption: refer to *Table 21*.
- **Low power wait mode:** This mode is entered when executing a Wait for event in Low power run mode. It is similar to Low power run mode except that the CPU clock is stopped. The wakeup from this mode is triggered by a Reset or by an internal or external event (peripheral event generated by the timers, serial interfaces, DMA controller (DMA1), comparators and I/O ports). When the wakeup is triggered by an event, the system goes back to Low power run mode.
  All interrupts must be masked. They cannot be used to exit the microcontroller from this mode. Low power wait mode consumption: refer to *Table 22*.
- **Active-halt mode**: CPU and peripheral clocks are stopped, except RTC. The wakeup can be triggered by RTC interrupts, external interrupts or reset. Active-halt consumption: refer to *Table 23* and *Table 24*.
- **Halt mode**: CPU and peripheral clocks are stopped, the device remains powered on. The RAM content is preserved. The wakeup is triggered by an external interrupt or reset. A few peripherals have also a wakeup from Halt capability. Switching off the internal reference voltage reduces power consumption. Through software configuration it is also possible to wake up the device without waiting for the internal reference voltage wakeup time to have a fast wakeup time of 5 µs. Halt consumption: refer to *Table 25*.

3.2 Central processing unit STM8

3.2.1 Advanced STM8 Core

The 8-bit STM8 core is designed for code efficiency and performance with an Harvard architecture and a 3-stage pipeline.

It contains 6 internal registers which are directly addressable in each execution context, 20 addressing modes including indexed indirect and relative addressing, and 80 instructions.

Architecture and registers

- Harvard architecture
- 3-stage pipeline
- 32-bit wide program memory bus - single cycle fetching most instructions
- X and Y 16-bit index registers - enabling indexed addressing modes with or without offset and read-modify-write type data manipulations
- 8-bit accumulator
- 24-bit program counter - 16 Mbyte linear memory space
- 16-bit stack pointer - access to a 64 Kbyte level stack
- 8-bit condition code register - 7 condition flags for the result of the last instruction

Addressing

- 20 addressing modes
- Indexed indirect addressing mode for lookup tables located anywhere in the address space
- Stack pointer relative addressing mode for local variables and parameter passing

Instruction set

- 80 instructions with 2-byte average instruction size
- Standard data movement and logic/arithmetic functions
- 8-bit by 8-bit multiplication
- 16-bit by 8-bit and 16-bit by 16-bit division
- Bit manipulation
- Data transfer between stack and accumulator (push/pop) with direct stack access
- Data transfer using the X and Y registers or direct memory-to-memory transfers

3.2.2 Interrupt controller

The low-density STM8L151x2/3 feature a nested vectored interrupt controller:

- Nested interrupts with 3 software priority levels
- 32 interrupt vectors with hardware priority
- Up to 40 external interrupt sources on 11 vectors
- Trap and reset interrupts

3.3 Reset and supply management

3.3.1 Power supply scheme

The device requires a 1.65 V to 3.6 V operating supply voltage (V_{DD}). The external power supply pins must be connected as follows:

- V_{SS1}; V_{DD1} = 1.8 to 3.6 V, down to 1.65 V at power down: external power supply for I/Os and for the internal regulator. Provided externally through V_{DD1} pins, the corresponding ground pin is V_{SS1}.
- $V_{SSA;}$ V_{DDA} = 1.8 to 3.6 V, down to 1.65 V at power down: external power supplies for analog peripherals (minimum voltage to be applied to V_{DDA} is 1.8 V when the ADC1 is used). V_{DDA} and V_{SSA} must be connected to V_{DD1} and V_{SS1}, respectively.
- V_{SS2}; V_{DD2} = 1.8 to 3.6 V, down to 1.65 V at power down: external power supplies for I/Os. V_{DD2} and V_{SS2} must be connected to V_{DD1} and V_{SS1}, respectively.
- V_{REF+}; V_{REF-} (for ADC1): external reference voltage for ADC1. Must be provided externally through V_{REF+} and V_{REF-} pin.

3.3.2 Power supply supervisor

The device has an integrated ZEROPOWER power-on reset (POR)/power-down reset (PDR), coupled with a brownout reset (BOR) circuitry. At power-on, BOR is always active, and ensures proper operation starting from 1.8 V. After the 1.8 V BOR threshold is reached, the option byte loading process starts, either to confirm or modify default thresholds, or to disable BOR permanently (in which case, the V_{DD} min value at power down is 1.65 V).

Five BOR thresholds are available through option bytes, starting from 1.8 V to 3 V. To reduce the power consumption in Halt mode, it is possible to automatically switch off the internal reference voltage (and consequently the BOR) in Halt mode. The device remains under reset when V_{DD} is below a specified threshold, $V_{POR/PDR}$ or V_{BOR}, without the need for any external reset circuit.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. This PVD offers 7 different levels between 1.85 V and 3.05 V, chosen by software, with a step around 200 mV. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.3.3 Voltage regulator

The low-density STM8L151x2/3 embeds an internal voltage regulator for generating the 1.8 V power supply for the core and peripherals.

This regulator has two different modes:

- Main voltage regulator mode (MVR) for Run, Wait for interrupt (WFI) and Wait for event (WFE) modes.
- Low power voltage regulator mode (LPVR) for Halt, Active-halt, Low power run and Low power wait modes.

When entering Halt or Active-halt modes, the system automatically switches from the MVR to the LPVR in order to reduce current consumption.

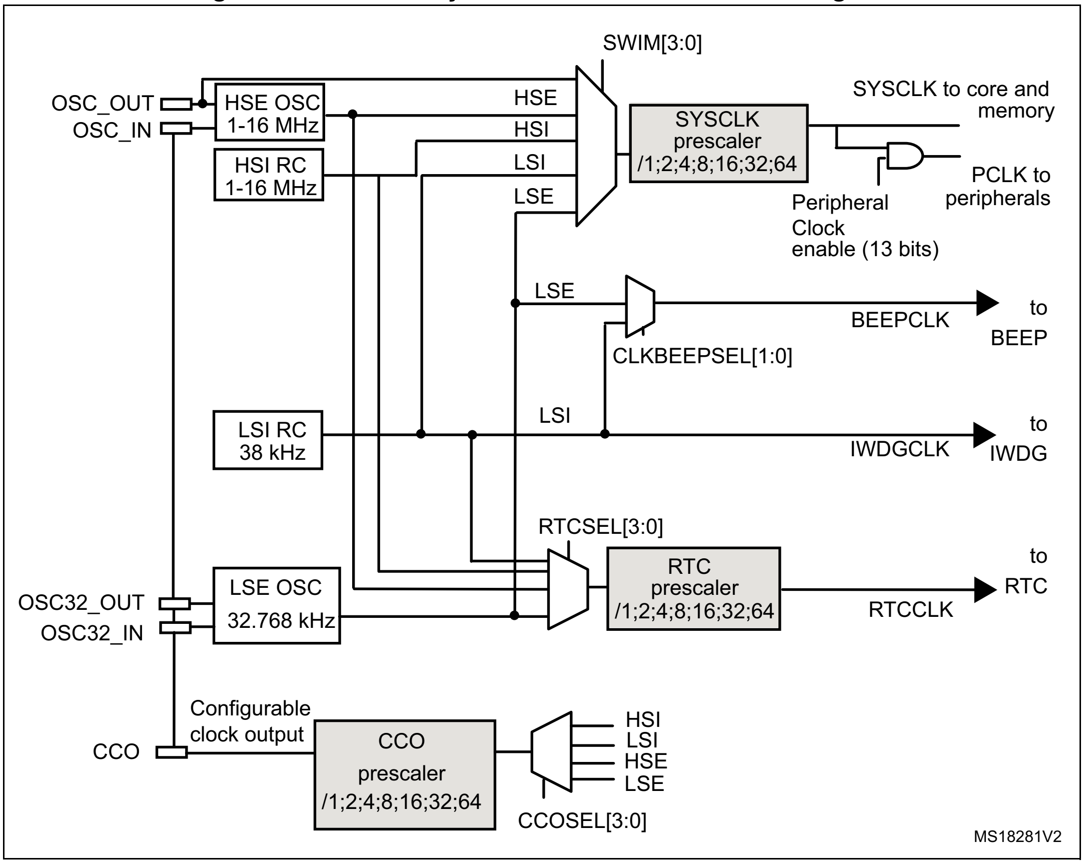
3.4 Clock management

The clock controller distributes the system clock (SYSCLK) coming from different oscillators to the core and the peripherals. It also manages clock gating for low power modes and ensures clock robustness.

Features

- **Clock prescaler:** to get the best compromise between speed and current consumption the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler
- **Safe clock switching:** Clock sources can be changed safely on the fly in run mode through a configuration register.
- **Clock management:** To reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **System clock sources:** 4 different clock sources can be used to drive the system clock:
  - 1-16 MHz High speed external crystal (HSE)
  - 16 MHz High speed internal RC oscillator (HSI)
  - 32.768 kHz Low speed external crystal (LSE)
  - 38 kHz Low speed internal RC (LSI)
- **RTC clock sources:** the above four sources can be chosen to clock the RTC whatever the system clock.
- **Startup clock:** After reset, the microcontroller restarts by default with an internal 2 MHz clock (HSI/8). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- **Clock security system (CSS):** This feature can be enabled by software. If a HSE clock failure occurs, the system clock is automatically switched to HSI.
- **Configurable main clock output (CCO):** This outputs an external clock for use by the application.

Figure 2. Low-density STM8L151x2/3 clock tree diagram



3.5 Low power real-time clock

The real-time clock (RTC) is an independent binary coded decimal (BCD) timer/counter.

Six byte locations contain the second, minute, hour (12/24 hour), week day, date, month, year, in BCD (binary coded decimal) format. Correction for 28, 29 (leap year), 30, and 31 day months are made automatically.

It provides a programmable alarm and programmable periodic interrupts with wakeup from Halt capability.

- Periodic wakeup time using the 32.768 kHz LSE with the lowest resolution (of 61 µs) is from min. 122 µs to max. 3.9 s. With a different resolution, the wakeup time can reach 36 hours
- Periodic alarms based on the calendar can also be generated from every second to every year

3.6 Memories

The low-density STM8L151x2/3 devices have the following main features:

- Up to 1 Kbyte of RAM
- The non-volatile memory is divided into three arrays:
  - Up to 8 Kbyte of low-density embedded Flash program memory
  - 256 byte of data EEPROM
  - Option bytes.

The EEPROM embeds the error correction code (ECC) feature.

The option byte protects part of the Flash program memory from write and readout piracy.

3.7 DMA

A 4-channel direct memory access controller (DMA1) offers a memory-to-memory and peripherals-from/to-memory transfer capability. The 4 channels are shared between the following IPs with DMA capability: ADC1, I2C1, SPI1, USART1, the three Timers.

3.8 Analog-to-digital converter

- 12-bit analog-to-digital converter (ADC1) with 25 channels (including 1 fast channel), temperature sensor and internal reference voltage
- Conversion time down to 1 µs with f_{SYSCLK}= 16 MHz
- Programmable resolution
- Programmable sampling time
- Single and continuous mode of conversion
- Scan capability: automatic conversion performed on a selected group of analog inputs
- Analog watchdog
- Triggered by timer

Note: ADC1 can be served by DMA1.

3.9 Ultra-low-power comparators

The low-density STM8L151x2/3 embed two comparators (COMP1 and COMP2) sharing the same current bias and voltage reference. The voltage reference can be internal or external (coming from an I/O).

- One comparator with fixed threshold (COMP1).
- One comparator rail to rail with fast or slow mode (COMP2). The threshold can be one of the following:
  - External I/O
  - Internal reference voltage or internal reference voltage sub multiple (1/4, 1/2, 3/4)

The two comparators can be used together to offer a window function. They can wake up from Halt mode.

3.10 System configuration controller and routing interface

The system configuration controller provides the capability to remap some alternate functions on different I/O ports. TIM4 and ADC1 DMA channels can also be remapped.

The highly flexible routing interface controls the routing of internal analog signals to ADC1, COMP1, COMP2, and the internal reference voltage V_{REFINT}. It also provides a set of registers for efficiently managing the charge transfer acquisition sequence (*Section 3.11: Touch sensing*).

3.11 Touch sensing

Low-density STM8L151x2/3 devices provide a simple solution for adding capacitive sensing functionality to any application. Capacitive sensing technology is able to detect finger presence near an electrode which is protected from direct touch by a dielectric (example, glass, plastic). The capacitive variation introduced by a finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle. It consists of charging the electrode capacitance and then transferring a part of the accumulated charges into a sampling capacitor until the voltage across this capacitor has reached a specific threshold. In low-density STM8L15xxx devices, the acquisition sequence is managed either by software or by hardware and it involves analog I/O groups, the routing interface, and timers.Reliable touch sensing solutions can be quickly and easily implemented using the free STM8 Touch Sensing Library.

3.12 Timers

Low-density STM8L151x2/3devices contain two 16-bit general purpose timers (TIM2 and TIM3) and one 8-bit basic timer (TIM4).

All the timers can be served by DMA1.

Table 2 compares the features of the advanced control, general-purpose and basic timers.

Table 2. Timer feature comparison

Timer	Counter resolution	Counter type	Prescaler factor	DMA1 request generation	Capture/compare channels	Complementary outputs
TIM2	16-bit	up/down	Any power of 2 from 1 to 128	Yes	2	None
TIM3						
TIM4	8-bit	up	Any power of 2 from 1 to 32768		0	

3.12.1 16-bit general purpose timers

- 16-bit autoreload (AR) up/down-counter
- 7-bit prescaler adjustable to fixed power of 2 ratios (1…128)
- 2 individually configurable capture/compare channels
- PWM mode
- Interrupt capability on various events (capture, compare, overflow, break, trigger)
- Synchronization with other timers or external signals (external clock, reset, trigger and enable)

3.12.2 8-bit basic timer

The 8-bit timer consists of an 8-bit up auto-reload counter driven by a programmable prescaler. It can be used for timebase generation with interrupt generation on timer overflow.

3.13 Watchdog timers

The watchdog system is based on two independent timers providing maximum security to the applications.

3.13.1 Window watchdog timer

The window watchdog (WWDG) is used to detect the occurrence of a software fault, usually generated by external interferences or by unexpected logical conditions, which cause the application program to abandon its normal sequence.

3.13.2 Independent watchdog timer

The independent watchdog peripheral (IWDG) can be used to resolve processor malfunctions due to hardware or software failures.

It is clocked by the internal LSI RC clock source, and thus stays active even in case of a CPU clock failure.

3.14 Beeper

The beeper function outputs a signal on the BEEP pin for sound generation. The signal is in the range of 1, 2 or 4 kHz.

3.15 Communication interfaces

3.15.1 SPI

The serial peripheral interface (SPI1) provides half/ full duplex synchronous serial communication with external devices.

- Maximum speed: 8 Mbit/s ($f_{SYSCLK}/2$) both for master and slave
- Full duplex synchronous transfers
- Simplex synchronous transfers on 2 lines with a possible bidirectional data line
- Master or slave operation - selectable by hardware or software
- Hardware CRC calculation
- Slave/master selection input pin

Note: SPI1 can be served by the DMA1 Controller.

3.15.2 I^2C

The I^2C bus interface (I^2C1) provides multi-master capability, and controls all I^2C bus-specific sequencing, protocol, arbitration and timing.

- Master, slave and multi-master capability
- Standard mode up to 100 kHz and fast speed modes up to 400 kHz.
- 7-bit and 10-bit addressing modes.
- SMBus 2.0 and PMBus support
- Hardware CRC calculation

Note: I^2C1 can be served by the DMA1 Controller.

3.15.3 USART

The USART interface (USART1) allows full duplex, asynchronous communications with external devices requiring an industry standard NRZ asynchronous serial data format. It offers a very wide range of baud rates.

- 1 Mbit/s full duplex SCI
- SPI1 emulation
- High precision baud rate generator
- SmartCard emulation
- IrDA SIR encoder decoder
- Single wire half duplex mode

Note: USART1 can be served by the DMA1 Controller.

3.16 Infrared (IR) interface

The low-density STM8L151x2/3 devices contain an infrared interface which can be used with an IR LED for remote control functions. Two timer output compare channels are used to generate the infrared remote control signals.

3.17 Development support

Development tools

Development tools for the STM8 microcontrollers include:

- The STice emulation system offering tracing and code profiling
- The STVD high-level language debugger including C compiler, assembler and integrated development environment
- The STVP Flash programming software

The STM8 also comes with starter kits, evaluation boards and low-cost in-circuit debugging/programming tools.

Single wire data interface (SWIM) and debug module

The debug module with its single wire data interface (SWIM) permits non-intrusive real-time in-circuit debugging and fast memory programming.

The single-wire interface is used for direct access to the debugging module and memory programming. The interface can be activated in all device operation modes.

The non-intrusive debugging module features a performance close to a full-featured emulator. Beside memory and peripherals, CPU operation can also be monitored in real-time by means of shadow registers.

Bootloader

The low-density STM8L151x2/3 ultra-low-power devices feature a built-in bootloader (see *UM0560: STM8 bootloader user manual*).

The bootloader is used to download application software into the device memories, including RAM, program and data memory, using standard serial interfaces. It is a complementary solution to programming via the SWIM debugging interface.

4 Pinout and pin description

Figure 3. STM8L151Cx LQFP48 package pinout

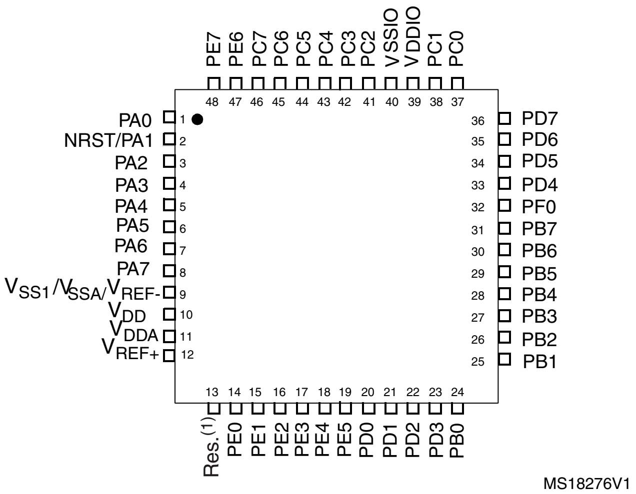


Figure 4. STM8L151Kx UFQFPN32 package pinout