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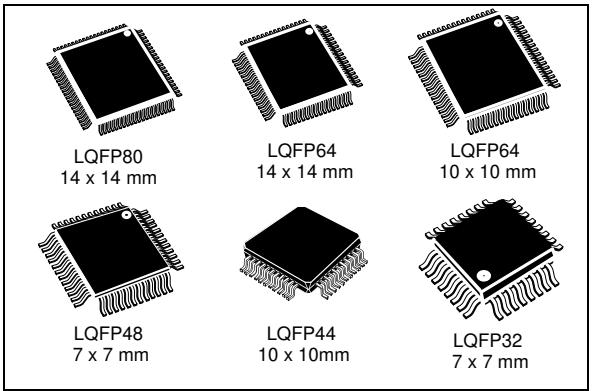
STM8S207xx STM8S208xx

Performance line, 24 MHz STM8S 8-bit MCU, up to 128 KB Flash, integrated EEPROM, 10-bit ADC, timers, 2 UARTs, SPI, I²C, CAN

Datasheet - production data

Features

- Core
  - Max f_{CPU}: up to 24 MHz, 0 wait states @ $f_{CPU} \leq$ 16 MHz
  - Advanced STM8 core with Harvard architecture and 3-stage pipeline
  - Extended instruction set
  - Max 20 MIPS @ 24 MHz
- Memories
  - Program: up to 128 Kbytes Flash; data retention 20 years at 55 °C after 10 kcycles
  - Data: up to 2 Kbytes true data EEPROM; endurance 300 kcycles
  - RAM: up to 6 Kbytes
- Clock, reset and supply management
  - 2.95 to 5.5 V operating voltage
  - Low power crystal resonator oscillator
  - External clock input
  - Internal, user-trimmable 16 MHz RC
  - Internal low power 128 kHz RC
  - Clock security system with clock monitor
  - Wait, active-halt, & halt low power modes
  - Peripheral clocks switched off individually
  - Permanently active, low consumption power-on and power-down reset
- Interrupt management
  - Nested interrupt controller with 32 interrupts
  - Up to 37 external interrupts on 6 vectors
- Timers
  - 2x 16-bit general purpose timers, with 2+3 CAPCOM channels (IC, OC or PWM)
  - Advanced control timer: 16-bit, 4 CAPCOM channels, 3 complementary outputs, dead-time insertion and flexible synchronization
  - 8-bit basic timer with 8-bit prescaler
  - Auto wakeup timer
  - Window watchdog, independent watchdog



- Communications interfaces
  - High speed 1 Mbit/s active beCAN 2.0B
  - UART with clock output for synchronous operation - LIN master mode
  - UART with LIN 2.1 compliant, master/slave modes and automatic resynchronization
  - SPI interface up to 10 Mbit/s
  - I²C interface up to 400 Kbit/s
- 10-bit ADC with up to 16 channels
- I/Os
  - Up to 68 I/Os on an 80-pin package including 18 high sink outputs
  - Highly robust I/O design, immune against current injection
  - Development support
  - Single wire interface module (SWIM) and debug module (DM)
- 96-bit unique ID key for each device

Table 1. Device summary

Reference	Part number
STM8S207xx	STM8S207MB, STM8S207M8, STM8S207RB, STM8S207R8, STM8S207R6, STM8S207CB, STM8S207C8, STM8S207C6, STM8S207SB, STM8S207S8, STM8S207S6, STM8S207K8, STM8S207K6
STM8S208xx	STM8S208MB, STM8S208RB, STM8S208R8, STM8S208R6, STM8S208CB, STM8S208C8, STM8S208C6, STM8S208SB, STM8S208S8, STM8S208S6

Contents

1 Introduction 9

2 Description 10

3 Block diagram 12

4 Product overview 13

4.1 Central processing unit STM8 13

4.2 Single wire interface module (SWIM) and debug module (DM) 14

4.3 Interrupt controller 14

4.4 Flash program and data EEPROM memory 14

4.5 Clock controller 16

4.6 Power management 17

4.7 Watchdog timers 17

4.8 Auto wakeup counter 18

4.9 Beeper 18

4.10 TIM1 - 16-bit advanced control timer 18

4.11 TIM2, TIM3 - 16-bit general purpose timers 18

4.12 TIM4 - 8-bit basic timer 19

4.13 Analog-to-digital converter (ADC2) 19

4.14 Communication interfaces 19

4.14.1 UART1 20

4.14.2 UART3 20

4.14.3 SPI 21

4.14.4 I^2C 22

4.14.5 beCAN 22

5 Pinouts and pin description 23

5.1 Package pinouts 23

5.2 Alternate function remapping 32

6 Memory and register map 34

6.1 Memory map 34

6.2 Register map 35

7 Interrupt vector mapping 46

8 Option bytes 47

9 Unique ID 51

10 Electrical characteristics 52

10.1 Parameter conditions 52

10.1.1 Minimum and maximum values 52

10.1.2 Typical values 52

10.1.3 Typical curves 52

10.1.4 Typical current consumption 52

10.1.5 Pin loading conditions 53

10.1.6 Loading capacitor 53

10.1.7 Pin input voltage 53

10.2 Absolute maximum ratings 54

10.3 Operating conditions 56

10.3.1 VCAP external capacitor 57

10.3.2 Supply current characteristics 58

10.3.3 External clock sources and timing characteristics 65

10.3.4 Internal clock sources and timing characteristics 67

10.3.5 Memory characteristics 69

10.3.6 I/O port pin characteristics 70

10.3.7 Reset pin characteristics 78

10.3.8 SPI serial peripheral interface 80

10.3.9 I^2C interface characteristics 83

10.3.10 10-bit ADC characteristics 85

10.3.11 EMC characteristics 88

11 Package characteristics 91

11.1 Package information 92

11.1.1 LQFP80 package information 92

11.1.2 LQFP64 package information 95

11.1.3 LQFP48 package information 99

11.1.4 LQFP44 package information 102

11.1.5 LQFP32 package information 105
11.2 Thermal characteristics 108
11.2.1 Reference document 108
11.2.2 Selecting the product temperature range 109

12 STM8 development tools 110
12.1 Emulation and in-circuit debugging tools 110
12.2 Software tools 111
12.2.1 STM8 toolset 111
12.2.2 C and assembly toolchains 111
12.3 Programming tools 111

13 Ordering information 112

14 Revision history 113

List of tables

Table 1. Device summary . . . 1
Table 2. STM8S20xxx performance line features . . . 11
Table 3. Peripheral clock gating bit assignments in CLK_PCKENR1/2 registers . . . 16
Table 4. TIM timer features . . . 19
Table 5. Legend/abbreviations for pinout table . . . 28
Table 6. Pin description . . . 28
Table 7. Flash, Data EEPROM and RAM boundary addresses . . . 35
Table 8. I/O port hardware register map . . . 35
Table 9. General hardware register map . . . 37
Table 10. CPU/SWIM/debug module/interrupt controller registers . . . 44
Table 11. Interrupt mapping . . . 46
Table 12. Option bytes . . . 47
Table 13. Option byte description . . . 48
Table 14. Unique ID registers (96 bits) . . . 51
Table 15. Voltage characteristics . . . 54
Table 16. Current characteristics . . . 55
Table 17. Thermal characteristics . . . 55
Table 18. General operating conditions . . . 56
Table 19. Operating conditions at power-up/power-down . . . 57
Table 20. Total current consumption with code execution in run mode at V_{DD} = 5 V . . . 58
Table 21. Total current consumption with code execution in run mode at V_{DD} = 3.3 V . . . 59
Table 22. Total current consumption in wait mode at V_{DD} = 5 V . . . 60
Table 23. Total current consumption in wait mode at V_{DD} = 3.3 V . . . 60
Table 24. Total current consumption in active halt mode at V_{DD} = 5 V, T_A -40 to 85° C . . . 61
Table 25. Total current consumption in active halt mode at V_{DD} = 3.3 V . . . 61
Table 26. Total current consumption in halt mode at V_{DD} = 5 V . . . 62
Table 27. Total current consumption in halt mode at V_{DD} = 3.3 V . . . 62
Table 28. Wakeup times . . . 62
Table 29. Total current consumption and timing in forced reset state . . . 63
Table 30. Peripheral current consumption . . . 63
Table 31. HSE user external clock characteristics . . . 65
Table 32. HSE oscillator characteristics . . . 66
Table 33. HSI oscillator characteristics . . . 67
Table 34. LSI oscillator characteristics . . . 68
Table 35. RAM and hardware registers . . . 69
Table 36. Flash program memory/data EEPROM memory . . . 69
Table 37. I/O static characteristics . . . 70
Table 38. Output driving current (standard ports) . . . 72
Table 39. Output driving current (true open drain ports) . . . 72
Table 40. Output driving current (high sink ports) . . . 72
Table 41. NRST pin characteristics . . . 78
Table 42. SPI characteristics . . . 80
Table 43. I^2C characteristics . . . 83
Table 44. ADC characteristics . . . 85
Table 45. ADC accuracy with R_{AIN} < 10 kΩ , V_{DDA} = 5 V . . . 86
Table 46. ADC accuracy with R_{AIN} < 10 kΩ R_{AIN}, V_{DDA} = 3.3 V . . . 86
Table 47. EMS data . . . 88
Table 48. EMI data . . . 89

Table 49. ESD absolute maximum ratings . . . 89
Table 50. Electrical sensitivities . . . 90
Table 51. LQFP80 - 80-pin, 14 x 14 mm low-profile quad flat package mechanical data . . . 92
Table 52. LQFP64 - 64-pin, 14 x 14 mm low-profile quad flat package mechanical data . . . 95
Table 53. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data . . . 96
Table 54. LQFP48 - 48-pin, 7x 7 mm low-profile quad flat package mechanical . . . 99
Table 55. LQFP44 - 44-pin, 10 x 10 mm low-profile quad flat package mechanical data . . . 103
Table 56. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package mechanical data . . . 106
Table 57. Thermal characteristics . . . 108
Table 58. Document revision history . . . 113

List of figures

Figure 1. STM8S20xxx block diagram . . . 12
Figure 2. Flash memory organization . . . 15
Figure 3. LQFP 80-pin pinout . . . 23
Figure 4. LQFP 64-pin pinout . . . 24
Figure 5. LQFP 48-pin pinout . . . 25
Figure 6. LQFP 44-pin pinout . . . 26
Figure 7. LQFP 32-pin pinout . . . 27
Figure 8. Memory map . . . 34
Figure 9. Supply current measurement conditions . . . 52
Figure 10. Pin loading conditions . . . 53
Figure 11. Pin input voltage . . . 53
Figure 12. f_{CPUmax} versus V_{DD} . . . 57
Figure 13. External capacitor C_{EXT} . . . 57
Figure 14. Typ. $I_{DD(RUN)}$ vs V_{DD}, HSI RC osc, f_{CPU} = 16 MHz . . . 64
Figure 15. Typ. $I_{DD(WFI)}$ vs V_{DD}, HSI RC osc, f_{CPU} = 16 MHz . . . 64
Figure 16. HSE external clock source . . . 65
Figure 17. HSE oscillator circuit diagram . . . 66
Figure 18. Typical HSI frequency variation vs V_{DD} at 4 temperatures . . . 67
Figure 19. Typical LSI frequency variation vs V_{DD} @ 25 °C . . . 68
Figure 20. Typical V_{IL} and V_{IH} vs V_{DD} @ 4 temperatures . . . 71
Figure 21. Typical pull-up resistance vs V_{DD} @ 4 temperatures . . . 71
Figure 22. Typical pull-up current vs V_{DD} @ 4 temperatures . . . 72
Figure 23. Typ. V_{OL} @ V_{DD} = 5 V (standard ports) . . . 73
Figure 24. Typ. V_{OL} @ V_{DD} = 3.3 V (standard ports) . . . 73
Figure 25. Typ. V_{OL} @ V_{DD} = 5 V (true open drain ports) . . . 74
Figure 26. Typ. V_{OL} @ V_{DD} = 3.3 V (true open drain ports) . . . 74
Figure 27. Typ. V_{OL} @ V_{DD} = 5 V (high sink ports) . . . 75
Figure 28. Typ. V_{OL} @ V_{DD} = 3.3 V (high sink ports) . . . 75
Figure 29. Typ. V_{DD} - V_{OH} @ V_{DD} = 5 V (standard ports) . . . 76
Figure 30. Typ. V_{DD} - V_{OH} @ V_{DD} = 3.3 V (standard ports) . . . 76
Figure 31. Typ. V_{DD} - V_{OH} @ V_{DD} = 5 V (high sink ports) . . . 77
Figure 32. Typ. V_{DD} - V_{OH} @ V_{DD} = 3.3 V (high sink ports) . . . 77
Figure 33. Typical NRST V_{IL} and V_{IH} vs V_{DD} @ 4 temperatures . . . 78
Figure 34. Typical NRST pull-up resistance vs V_{DD} @ 4 temperatures . . . 79
Figure 35. Typical NRST pull-up current vs V_{DD} @ 4 temperatures . . . 79
Figure 36. Recommended reset pin protection . . . 79
Figure 37. SPI timing diagram - slave mode and CPHA = 0 . . . 81
Figure 38. SPI timing diagram - slave mode and CPHA = 1(1) . . . 81
Figure 39. SPI timing diagram - master mode(1) . . . 82
Figure 40. Typical application with I^2C bus and timing diagram . . . 84
Figure 41. ADC accuracy characteristics . . . 87
Figure 42. Typical application with ADC . . . 87
Figure 43. LQFP80 - 80-pin, 14 x 14 mm low-profile quad flat package outline . . . 92
Figure 44. LQFP80 recommended footprint . . . 93
Figure 45. LQFP80 marking example (package top view) . . . 94
Figure 46. LQFP64 - 64-pin 14 mm x 14 mm low-profile quad flat package outline . . . 95
Figure 47. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package outline . . . 96
Figure 48. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat recommended footprint . . . 97

Figure 49. LQFP64 marking example (package top view) 98
Figure 50. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline 99
Figure 51. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat recommended footprint 100
Figure 52. LQFP48 marking example (package top view) 101
Figure 53. LQFP44 - 44-pin, 10 x 10 mm low-profile quad flat package outline 102
Figure 54. LQFP44 - 44-pin, 10 x 10 mm low-profile quad flat recommended footprint 104
Figure 55. LQFP44 marking example (package top view) 104
Figure 56. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package outline 105
Figure 57. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat recommended footprint 106
Figure 58. LQFP32 marking example (package top view) 107
Figure 59. STM8S207xx/208xx performance line ordering information scheme(1) 112

1 Introduction

This datasheet contains the description of the STM8S20xxx features, pinout, electrical characteristics, mechanical data and ordering information.

- For complete information on the STM8S microcontroller memory, registers and peripherals, please refer to the STM8S microcontroller family reference manual (RM0016).
- For information on programming, erasing and protection of the internal Flash memory please refer to the STM8S Flash programming manual (PM0051).
- For information on the debug and SWIM (single wire interface module) refer to the STM8 SWIM communication protocol and debug module user manual (UM0470).
- For information on the STM8 core, please refer to the STM8 CPU programming manual (PM0044).

2 Description

The STM8S20xxx performance line 8-bit microcontrollers offer from 32 to 128 Kbytes Flash program memory. They are referred to as high-density devices in the STM8S microcontroller family reference manual.

All STM8S20xxx devices provide the following benefits: reduced system cost, performance robustness, short development cycles, and product longevity.

The system cost is reduced thanks to an integrated true data EEPROM for up to 300 k write/erase cycles and a high system integration level with internal clock oscillators, watchdog, and brown-out reset.

Device performance is ensured by 20 MIPS at 24 MHz CPU clock frequency and enhanced characteristics which include robust I/O, independent watchdogs (with a separate clock source), and a clock security system.

Short development cycles are guaranteed due to application scalability across a common family product architecture with compatible pinout, memory map and modular peripherals. Full documentation is offered with a wide choice of development tools.

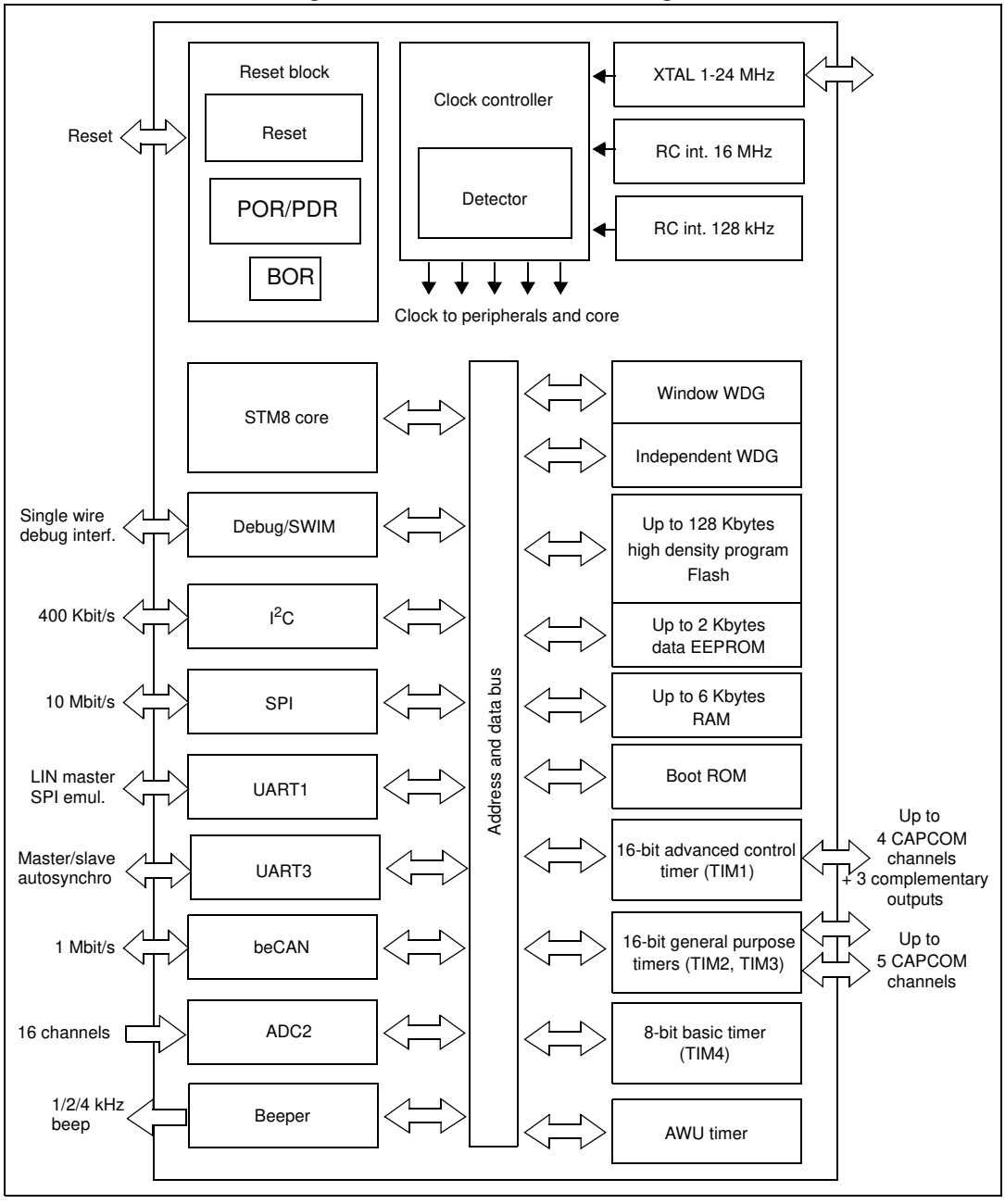
Product longevity is ensured in the STM8S family thanks to their advanced core which is made in a state-of-the art technology for applications with 2.95 V to 5.5 V operating supply.

Table 2. STM8S20xxx performance line features

Device	Pin count	Max. number of GPIOs (I/O)	Ext. interrupt pins	Timer CAPCOM channels	Timer complementary outputs	A/D converter channels	High sink I/Os	High density Flash program memory (bytes)	Data EEPROM (bytes	RAM (bytes)	beCAN interface
STM8S207MB	80	68	37	9	3	16	18	128 K	2048	6 K	
STM8S207M8	80	68	37	9	3	16	18	64 K	2048	6 K	
STM8S207RB	64	52	36	9	3	16	16	128 K	2048	6 K	
STM8S207R8	64	52	36	9	3	16	16	64 K	1536	6 K	
STM8S207R6	64	52	36	9	3	16	16	32 K	1024	6 K	
STM8S207CB	48	38	35	9	3	10	16	128 K	2048	6 K	
STM8S207C8	48	38	35	9	3	10	16	64 K	1536	6 K	No
STM8S207C6	48	38	35	9	3	10	16	32 K	1024	6 K	
STM8S207SB	44	34	31	8	3	9	15	128 K	1536	6 K	
STM8S207S8	44	34	31	8	3	9	15	64 K	1536	6 K	
STM8S207S6	44	34	31	8	3	9	15	32 K	1024	6 K	
STM8S207K8	32	25	23	8	3	7	12	64 K	1024	6 K	
STM8S207K6	32	25	23	8	3	7	12	32 K	1024	6 K	
STM8S208MB	80	68	37	9	3	16	18	128 K	2048	6 K	
STM8S208RB	64	52	37	9	3	16	16	128 K	2048	6 K	
STM8S208R8	64	52	37	9	3	16	16	64 K	2048	6 K	
STM8S208R6	64	52	37	9	3	16	16	32 K	2048	6 K	
STM8S208CB	48	38	35	9	3	10	16	128 K	2048	6 K	
STM8S208C8	48	38	35	9	3	10	16	64 K	2048	6 K	Yes
STM8S208C6	48	38	35	9	3	10	16	32 K	2048	6 K	
STM8S208SB	44	34	31	8	3	9	15	128 K	1536	6 K	
STM8S208S8	44	34	31	8	3	9	15	64 K	1536	6 K	
STM8S208S6	44	34	31	8	3	9	15	32 K	1536	6 K	

3 Block diagram

Figure 1. STM8S20xxx block diagram



1. Legend:
   ADC: Analog-to-digital converter
   beCAN: Controller area network
   BOR: Brownout reset
   I²C: Inter-integrated circuit multimaster interface
   Independent WDG: Independent watchdog
   POR/PDR: Power on reset / power down reset
   SPI: Serial peripheral interface
   SWIM: Single wire interface module
   UART: Universal asynchronous receiver transmitter
   Window WDG: Window watchdog

4 Product overview

The following section intends to give an overview of the basic features of the STM8S20xxx functional modules and peripherals.

For more detailed information please refer to the corresponding family reference manual (RM0016).

4.1 Central processing unit STM8

The 8-bit STM8 core is designed for code efficiency and performance.

It contains 6 internal registers which are directly addressable in each execution context, 20 addressing modes including indexed indirect and relative addressing and 80 instructions.

Architecture and registers

- Harvard architecture
- 3-stage pipeline
- 32-bit wide program memory bus - single cycle fetching for most instructions
- X and Y 16-bit index registers - enabling indexed addressing modes with or without offset and read-modify-write type data manipulations
- 8-bit accumulator
- 24-bit program counter - 16-Mbyte linear memory space
- 16-bit stack pointer - access to a 64 K-level stack
- 8-bit condition code register - 7 condition flags for the result of the last instruction

Addressing

- 20 addressing modes
- Indexed indirect addressing mode for look-up tables located anywhere in the address space
- Stack pointer relative addressing mode for local variables and parameter passing

Instruction set

- 80 instructions with 2-byte average instruction size
- Standard data movement and logic/arithmetic functions
- 8-bit by 8-bit multiplication
- 16-bit by 8-bit and 16-bit by 16-bit division
- Bit manipulation
- Data transfer between stack and accumulator (push/pop) with direct stack access
- Data transfer using the X and Y registers or direct memory-to-memory transfers

4.2 Single wire interface module (SWIM) and debug module (DM)

The single wire interface module and debug module permits non-intrusive, real-time in-circuit debugging and fast memory programming.

SWIM

Single wire interface module for direct access to the debug module and memory programming. The interface can be activated in all device operation modes. The maximum data transmission speed is 145 bytes/ms.

Debug module

The non-intrusive debugging module features a performance close to a full-featured emulator. Beside memory and peripherals, also CPU operation can be monitored in real-time by means of shadow registers.

- R/W to RAM and peripheral registers in real-time
- R/W access to all resources by stalling the CPU
- Breakpoints on all program-memory instructions (software breakpoints)
- Two advanced breakpoints, 23 predefined configurations

4.3 Interrupt controller

- Nested interrupts with three software priority levels
- 32 interrupt vectors with hardware priority
- Up to 37 external interrupts on six vectors including TLI
- Trap and reset interrupts

4.4 Flash program and data EEPROM memory

- Up to 128 Kbytes of high density Flash program single voltage Flash memory
- Up to 2K bytes true data EEPROM
- Read while write: Writing in data memory possible while executing code in program memory.
- User option byte area

Write protection (WP)

Write protection of Flash program memory and data EEPROM is provided to avoid unintentional overwriting of memory that could result from a user software malfunction.

There are two levels of write protection. The first level is known as MASS (memory access security system). MASS is always enabled and protects the main Flash program memory, data EEPROM and option bytes.

To perform in-application programming (IAP), this write protection can be removed by writing a MASS key sequence in a control register. This allows the application to write to data EEPROM, modify the contents of main program memory or the device option bytes.

A second level of write protection, can be enabled to further protect a specific area of memory known as UBC (user boot code). Refer to *Figure 2*.

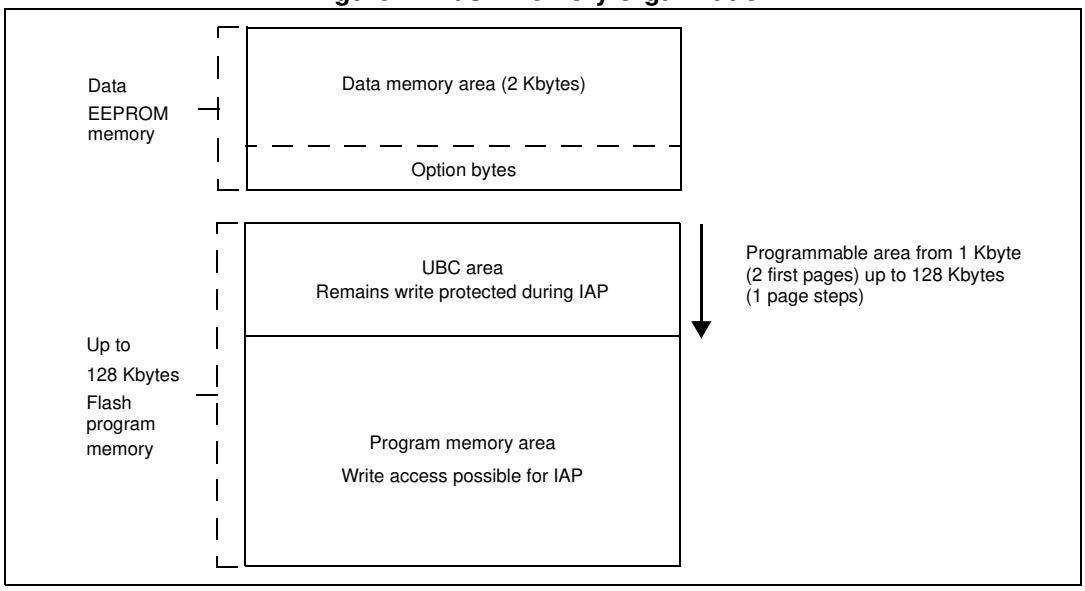
The size of the UBC is programmable through the UBC option byte (*Table 13.*), in increments of 1 page (512 bytes) by programming the UBC option byte in ICP mode.

This divides the program memory into two areas:

- Main program memory: Up to 128 Kbytes minus UBC
- User-specific boot code (UBC): Configurable up to 128 Kbytes

The UBC area remains write-protected during in-application programming. This means that the MASS keys do not unlock the UBC area. It protects the memory used to store the boot program, specific code libraries, reset and interrupt vectors, the reset routine and usually the IAP and communication routines.

Figure 2. Flash memory organization



Read-out protection (ROP)

The read-out protection blocks reading and writing the Flash program memory and data EEPROM memory in ICP mode (and debug mode). Once the read-out protection is activated, any attempt to toggle its status triggers a global erase of the program and data memory. Even if no protection can be considered as totally unbreakable, the feature provides a very high level of protection for a general purpose microcontroller.

4.5 Clock controller

The clock controller distributes the system clock (f_{MASTER}) coming from different oscillators to the core and the peripherals. It also manages clock gating for low power modes and ensures clock robustness.

Features

- ***Clock prescaler*:** To get the best compromise between speed and current consumption the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler.
- ***Safe clock switching*:** Clock sources can be changed safely on the fly in run mode through a configuration register. The clock signal is not switched until the new clock source is ready. The design guarantees glitch-free switching.
- ***Clock management*:** To reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- ***Master clock sources*:** Four different clock sources can be used to drive the master clock:
  - 1-24 MHz high-speed external crystal (HSE)
  - Up to 24 MHz high-speed user-external clock (HSE user-ext)
  - 16 MHz high-speed internal RC oscillator (HSI)
  - 128 kHz low-speed internal RC (LSI)
- ***Startup clock*:** After reset, the microcontroller restarts by default with an internal 2 MHz clock (HSI/8). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- ***Clock security system (CSS)*:** This feature can be enabled by software. If an HSE clock failure occurs, the internal RC (16 MHz/8) is automatically selected by the CSS and an interrupt can optionally be generated.
- ***Configurable main clock output (CCO)*:** This outputs an external clock for use by the application.

Table 3. Peripheral clock gating bit assignments in CLK_PCKENR1/2 registers

Bit	Peripheral clock	Bit	Peripheral clock	Bit	Peripheral clock	Bit	Peripheral clock
PCKEN17	TIM1	PCKEN13	UART3	PCKEN27	beCAN	PCKEN23	ADC
PCKEN16	TIM3	PCKEN12	UART1	PCKEN26	Reserved	PCKEN22	AWU
PCKEN15	TIM2	PCKEN11	SPI	PCKEN25	Reserved	PCKEN21	Reserved
PCKEN14	TIM4	PCKEN10	I^2C	PCKEN24	Reserved	PCKEN20	Reserved

4.6 Power management

For efficient power management, the application can be put in one of four different low-power modes. You can configure each mode to obtain the best compromise between lowest power consumption, fastest start-up time and available wakeup sources.

- ***Wait mode***: In this mode, the CPU is stopped, but peripherals are kept running. The wakeup is performed by an internal or external interrupt or reset.
- ***Active halt mode with regulator on***: In this mode, the CPU and peripheral clocks are stopped. An internal wakeup is generated at programmable intervals by the auto wake up unit (AWU). The main voltage regulator is kept powered on, so current consumption is higher than in active halt mode with regulator off, but the wakeup time is faster. Wakeup is triggered by the internal AWU interrupt, external interrupt or reset.
- ***Active halt mode with regulator off:*** This mode is the same as active halt with regulator on, except that the main voltage regulator is powered off, so the wake up time is slower.
- ***Halt mode***: In this mode the microcontroller uses the least power. The CPU and peripheral clocks are stopped, the main voltage regulator is powered off. Wakeup is triggered by external event or reset.

4.7 Watchdog timers

The watchdog system is based on two independent timers providing maximum security to the applications.

Activation of the watchdog timers is controlled by option bytes or by software. Once activated, the watchdogs cannot be disabled by the user program without performing a reset.

Window watchdog timer

The window watchdog is used to detect the occurrence of a software fault, usually generated by external interferences or by unexpected logical conditions, which cause the application program to abandon its normal sequence.

The window function can be used to trim the watchdog behavior to match the application perfectly.

The application software must refresh the counter before time-out and during a limited time window.

A reset is generated in two situations:

1. Timeout: At 16 MHz CPU clock the time-out period can be adjusted between 75 µs up to 64 ms.
2. Refresh out of window: The downcounter is refreshed before its value is lower than the one stored in the window register.

Independent watchdog timer

The independent watchdog peripheral can be used to resolve processor malfunctions due to hardware or software failures.

It is clocked by the 128 kHz LSI internal RC clock source, and thus stays active even in case of a CPU clock failure

The IWDG time base spans from 60 µs to 1 s.

4.8 Auto wakeup counter

- Used for auto wakeup from active halt mode
- Clock source: Internal 128 kHz internal low frequency RC oscillator or external clock
- LSI clock can be internally connected to TIM3 input capture channel 1 for calibration

4.9 Beeper

The beeper function outputs a signal on the BEEP pin for sound generation. The signal is in the range of 1, 2 or 4 kHz.

4.10 TIM1 - 16-bit advanced control timer

This is a high-end timer designed for a wide range of control applications. With its complementary outputs, dead-time control and center-aligned PWM capability, the field of applications is extended to motor control, lighting and half-bridge driver

- 16-bit up, down and up/down autoreload counter with 16-bit prescaler
- Four independent capture/compare channels (CAPCOM) configurable as input capture, output compare, PWM generation (edge and center aligned mode) and single pulse mode output
- Synchronization module to control the timer with external signals
- Break input to force the timer outputs into a defined state
- Three complementary outputs with adjustable dead time
- Encoder mode
- Interrupt sources: 3 x input capture/output compare, 1 x overflow/update, 1 x break

4.11 TIM2, TIM3 - 16-bit general purpose timers

- 16-bit autoreload (AR) up-counter
- 15-bit prescaler adjustable to fixed power of 2 ratios 1…32768
- Timers with 3 or 2 individually configurable capture/compare channels
- PWM mode
- Interrupt sources: 2 or 3 x input capture/output compare, 1 x overflow/update

4.12 TIM4 - 8-bit basic timer

- 8-bit autoreload, adjustable prescaler ratio to any power of 2 from 1 to 128
- Clock source: CPU clock
- Interrupt source: 1 x overflow/update

Table 4. TIM timer features

Timer	Counter size (bits)	Prescaler	Counting mode	CAPCOM channels	Complem. outputs	Ext. trigger	Timer synchr-onization/ chaining
TIM1	16	Any integer from 1 to 65536	Up/down	4	3	Yes	No
TIM2	16	Any power of 2 from 1 to 32768	Up	3	0	No	
TIM3	16	Any power of 2 from 1 to 32768	Up	2	0	No	
TIM4	8	Any power of 2 from 1 to 128	Up	0	0	No	

4.13 Analog-to-digital converter (ADC2)

STM8S20xxx performance line products contain a 10-bit successive approximation A/D converter (ADC2) with up to 16 multiplexed input channels and the following main features:

- Input voltage range: 0 to V_{DDA}
- Dedicated voltage reference (VREF) pins available on 80 and 64-pin devices
- Conversion time: 14 clock cycles
- Single and continuous modes
- External trigger input
- Trigger from TIM1 TRGO
- End of conversion (EOC) interrupt

4.14 Communication interfaces

The following communication interfaces are implemented:

- UART1: Full feature UART, SPI emulation, LIN2.1 master capability, Smartcard mode, IrDA mode, single wire mode.
- UART3: Full feature UART, LIN2.1 master/slave capability
- SPI: Full and half-duplex, 10 Mbit/s
- I^2C: Up to 400 Kbit/s
- beCAN (rev. 2.0A,B) - 3 Tx mailboxes - up to 1 Mbit/s

4.14.1 UART1

Main features

- One Mbit/s full duplex SCI
- SPI emulation
- High precision baud rate generator
- Smartcard emulation
- IrDA SIR encoder decoder
- LIN master mode
- Single wire half duplex mode

Asynchronous communication (UART mode)

- Full duplex communication - NRZ standard format (mark/space)
- Programmable transmit and receive baud rates up to 1 Mbit/s (f_{CPU}/16) and capable of following any standard baud rate regardless of the input frequency
- Separate enable bits for transmitter and receiver
- Two receiver wakeup modes:
  - Address bit (MSB)
  - Idle line (interrupt)
- Transmission error detection with interrupt generation
- Parity control

Synchronous communication

- Full duplex synchronous transfers
- SPI master operation
- 8-bit data communication
- Maximum speed: 1 Mbit/s at 16 MHz (f_{CPU}/16)

LIN master mode

- Emission: Generates 13-bit sync break frame
- Reception: Detects 11-bit break frame

4.14.2 UART3

Main features

- 1 Mbit/s full duplex SCI
- LIN master capable
- High precision baud rate generator

Asynchronous communication (UART mode)

- Full duplex communication - NRZ standard format (mark/space)
- Programmable transmit and receive baud rates up to 1 Mbit/s (f_{CPU}/16) and capable of following any standard baud rate regardless of the input frequency
- Separate enable bits for transmitter and receiver
- Two receiver wakeup modes:
  - Address bit (MSB)
  - Idle line (interrupt)
- Transmission error detection with interrupt generation
- Parity control

LIN master capability

- Emission: Generates 13-bit sync break frame
- Reception: Detects 11-bit break frame

LIN slave mode

- Autonomous header handling - one single interrupt per valid message header
- Automatic baud rate synchronization - maximum tolerated initial clock deviation ±15%
- Sync delimiter checking
- 11-bit LIN sync break detection - break detection always active
- Parity check on the LIN identifier field
- LIN error management
- Hot plugging support

4.14.3 SPI

- Maximum speed: 10 Mbit/s (f_{MASTER}/2) both for master and slave
- Full duplex synchronous transfers
- Simplex synchronous transfers on two lines with a possible bidirectional data line
- Master or slave operation - selectable by hardware or software
- CRC calculation
- 1 byte Tx and Rx buffer
- Slave/master selection input pin

4.14.4 I²C

- I²C master features:
  - Clock generation
  - Start and stop generation
- I²C slave features:
  - Programmable I²C address detection
  - Stop bit detection
- Generation and detection of 7-bit/10-bit addressing and general call
- Supports different communication speeds:
  - Standard speed (up to 100 kHz)
  - Fast speed (up to 400 kHz)

4.14.5 beCAN

The beCAN controller (basic enhanced CAN), interfaces the CAN network and supports the CAN protocol version 2.0A and B. It has been designed to manage a high number of incoming messages efficiently with a minimum CPU load.

For safety-critical applications the beCAN controller provides all hardware functions to support the CAN time triggered communication option (TTCAN).

The maximum transmission speed is 1 Mbit.

Transmission

- Three transmit mailboxes
- Configurable transmit priority by identifier or order request
- Time stamp on SOF transmission

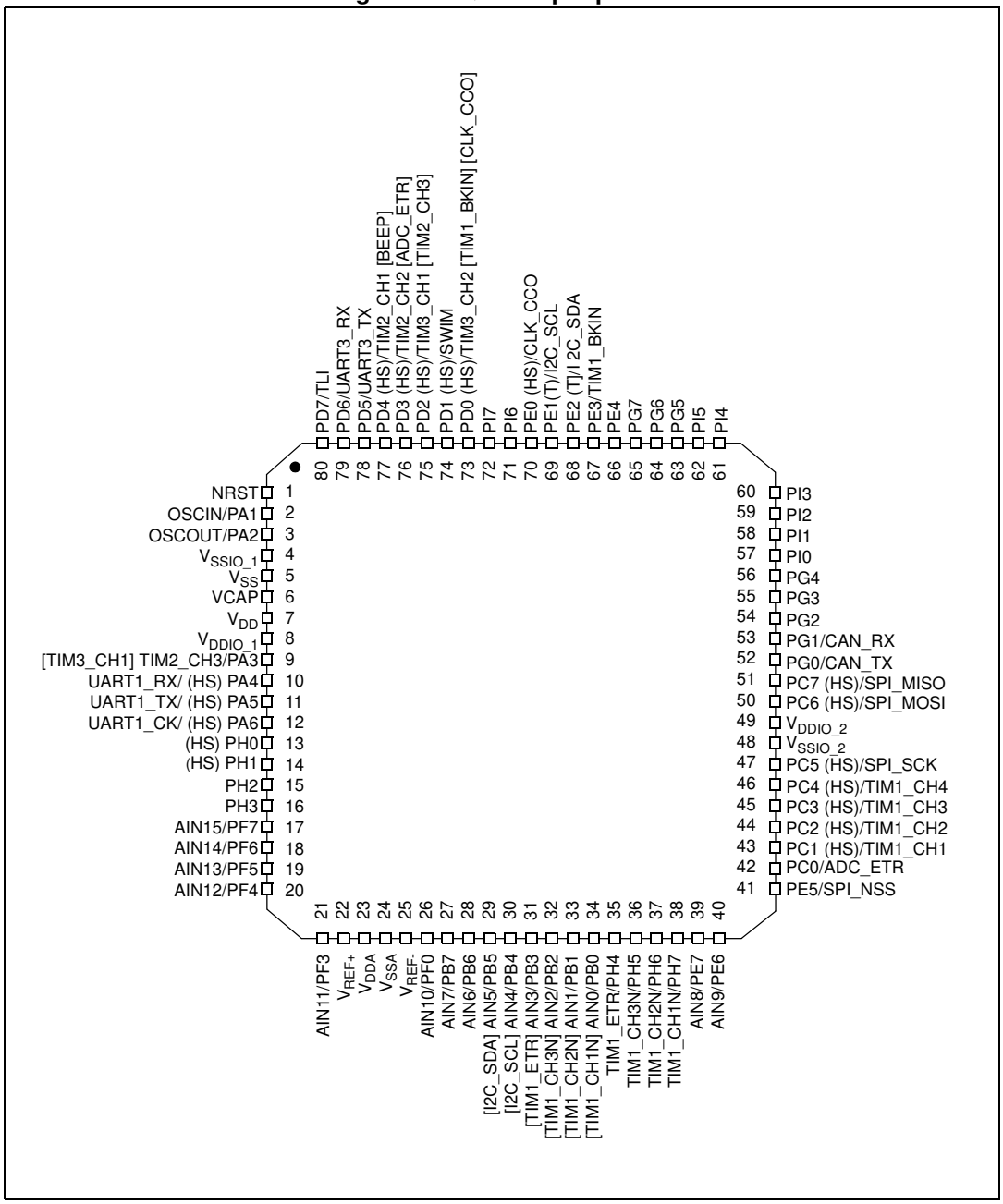
Reception

- 8-, 11- and 29-bit ID
- One receive FIFO (3 messages deep)
- Software-efficient mailbox mapping at a unique address space
- FMI (filter match index) stored with message
- Configurable FIFO overrun
- Time stamp on SOF reception
- Six filter banks, 2 x 32 bytes (scalable to 4 x 16-bit) each, enabling various masking configurations, such as 12 filters for 29-bit ID or 48 filters for 11-bit ID
- Filtering modes:
  - Mask mode permitting ID range filtering
  - ID list mode
- Time triggered communication option
  - Disable automatic retransmission mode
  - 16-bit free running timer
  - Configurable timer resolution
  - Time stamp sent in last two data bytes

5 Pinouts and pin description

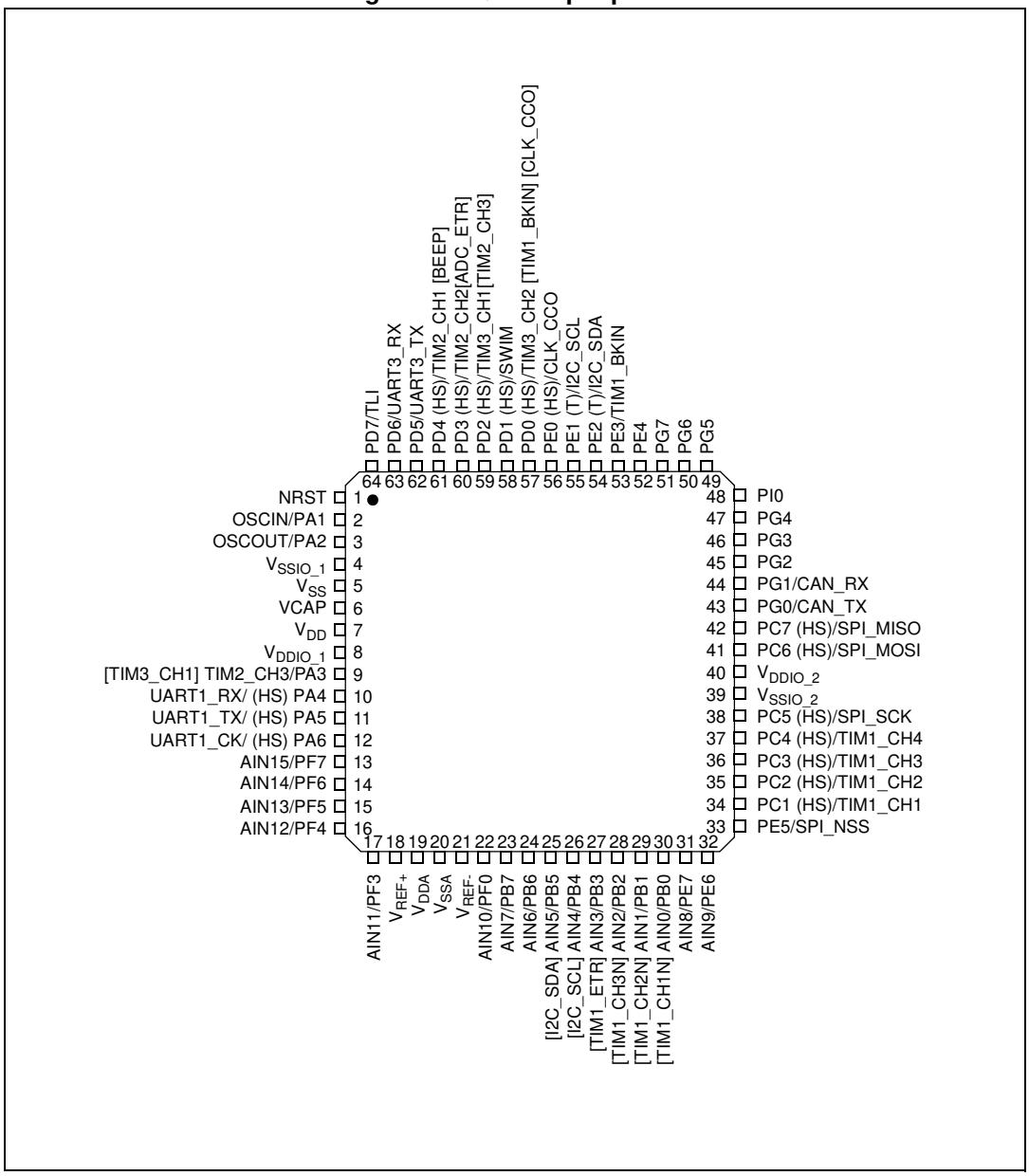
5.1 Package pinouts

Figure 3. LQFP 80-pin pinout



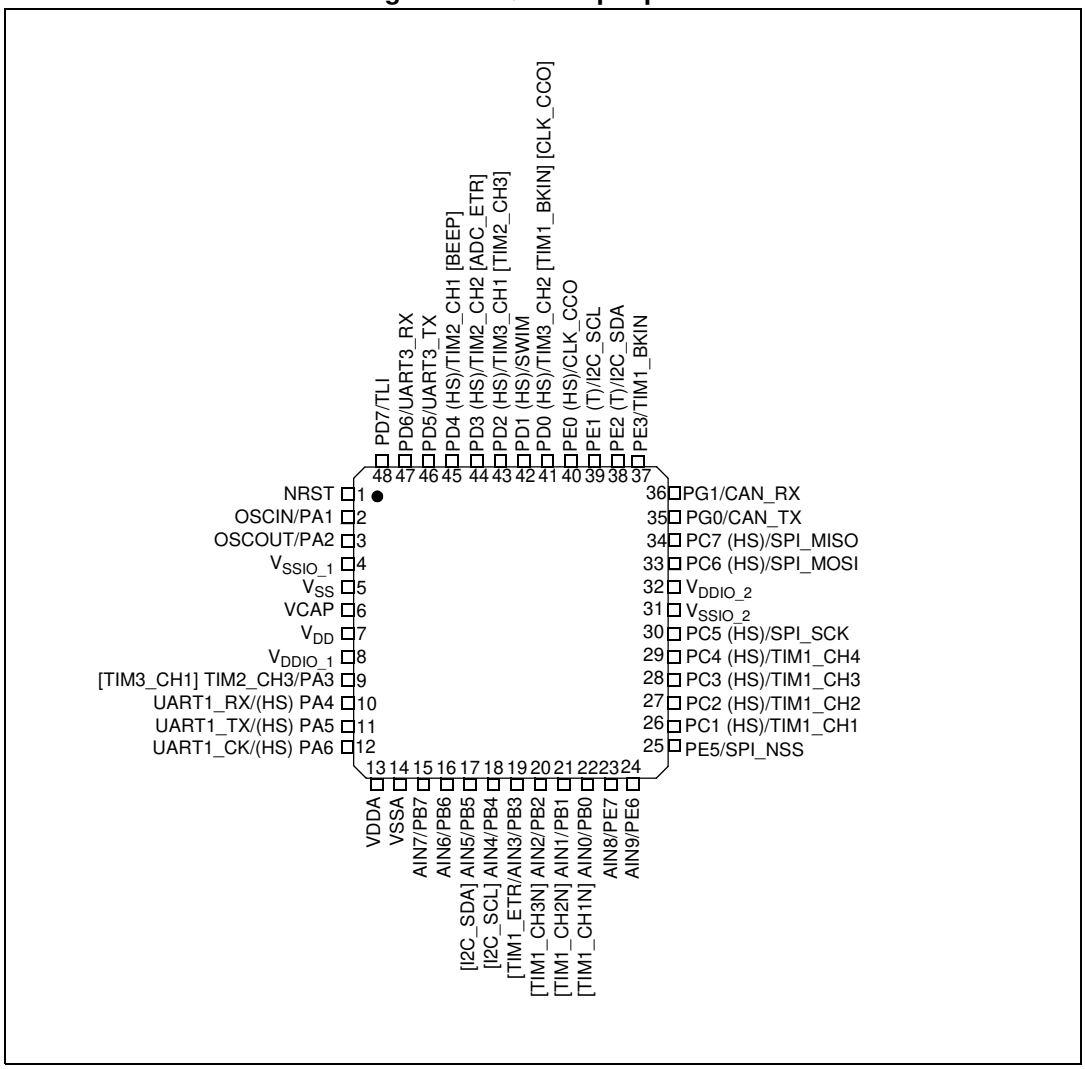
1. (HS) high sink capability.
2. (T) True open drain (P-buffer and protection diode to V_{DD} not implemented).
3. [ ] alternate function remapping option (If the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).
4. CAN_RX and CAN_TX is available on STM8S208xx devices only.

Figure 4. LQFP 64-pin pinout



1. (HS) high sink capability.
2. (T) True open drain (P-buffer and protection diode to V_{DD} not implemented).
3. [ ] alternate function remapping option (If the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).
4. CAN_RX and CAN_TX is available on STM8S208xx devices only.

Figure 5. LQFP 48-pin pinout



1. (HS) high sink capability.
2. (T) True open drain (P-buffer and protection diode to V_{DD} not implemented).
3. [ ] alternate function remapping option (If the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).
4. CAN_RX and CAN_TX is available on STM8S208xx devices only.