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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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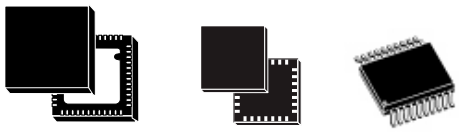
STM8TL52x4 STM8TL53x4

8-bit ultra-low-power touch sensing microcontroller with 16 Kbyte Flash, ProxSense™, timers, USART, SPI, I2C

Datasheet - production data

Features

- Operating conditions
  - Operating power supply: 1.65 V to 3.6 V
  - Temperature range: –40 °C to 85 °C
- Low power features
  - 4 low power modes: Wait, Active-halt with AWU (1 µA), Active-halt with ProxSense™ (10 µA with scan every 200 ms), Halt (0.4 µA)
  - Dynamic power consumption: 150 µA/MHz
  - Fast wakeup from Halt mode: 4.7 µs
  - Ultra-low leakage per I/O: 50 nA
- Advanced STM8 Core
  - Harvard architecture with 3-stage pipeline
  - Max freq.16 MHz,16 CISC MIPS peak
- Memories
  - Up to 16 Kbyte of Flash program including up to 2 Kbyte of data EEPROM
  - Error correction code (ECC)
  - Flexible write and read protection modes
  - In-application and in-circuit programming
  - Data EEPROM capability
  - 4 Kbyte of static RAM
- Clock management
  - Internal 16 MHz factory-trimmed RC
  - Internal 38 kHz low consumption RC driving both the IWDG and the AWU
- Reset and supply management
  - Ultra-low-power, ultra safe power-on reset/ power-down reset
- Interrupt management
  - Nested interrupt controller with software priority control
  - Up to 22 external interrupt sources



UFQFPN48 7x7 mm | UFQFPN28 4x4 mm | TSSOP20

- I/Os
  - Up to 23 with 22 mappable on external interrupt vectors
  - I/Os with programmable input pull-ups, high sink/source capability
- ProxSense™ patented acquisition technology with up to 300 touch sensing channels (20 receiver/transmitter channels and 15 transmitter channels) supporting projected capacitive acquisition method suitable for proximity detection.
- Timers
  - Two 16-bit general purpose timers (TIM2 and TIM3) with up and down counter and two channels (used as IC, OC, PWM)
  - One 8-bit timer (TIM4) with 7-bit prescaler
  - Independent watchdog
  - Window watchdog
  - Auto-wakeup unit
  - Beeper timer with 1, 2 or 4 kHz frequencies
- Communication interfaces
  - SPI synchronous serial interface
  - Fast I^2C Multimaster/slave 400 kHz
  - USART with fractional baud rate generator
- Development support
  - Hardware single wire interface module (SWIM)
  - In-circuit emulation (ICE)

Table 1. Device summary

Reference	Part number
STM8TL52x4	STM8TL52F4, STM8TL52G4
STM8TL53x4	STM8TL53C4, STM8TL53F4, STM8TL53G4

Contents

List of tables

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1 Introduction

This datasheet provides the STM8TL52G4, STM8TL52F4, STM8TL53C4, STM8TL53G4 and STM8TL53F4 pinouts, ordering information, mechanical and electrical device characteristics.

For complete information on the microcontroller memory, registers and peripherals, please refer to the STM8TL5xxx reference manual (RM0312) and to the STM8TL5xxx Flash programming manual (PM0212) for Flash memory related information. For information on the debug module and SWIM (single wire interface module), refer to the STM8 SWIM communication protocol and debug module user manual (UM0470). For information on the STM8 core, refer to the STM8 CPU programming manual (PM0044).

All devices of the STM8TL5xxx product line provide the following benefits:

- Advanced capacitive sensing
  - Patented ProxSense ™ acquisition peripheral, providing high-end acquisition, filtering and environment adaptation
  - Outstanding signal-to-noise ratio for touch and proximity sensing
  - Up to 300 projected capacitive channels
- Reduced system cost
  - Up to 16 Kbyte of low-density embedded Flash program memory including up to 2 Kbyte of data EEPROM
  - High system integration level with internal clock oscillators and watchdogs
  - Smaller battery and cheaper power supplies
- Low power consumption and advanced features
  - Up to 16 MIPS at 16 MHz CPU clock frequency
  - Less than 150 µA/MHz, 0.8 µA in Active-halt mode with AWU, and 0.3 µA in Halt mode
  - Clock gated system and optimized power management
- Short development cycles
  - Application scalability across a common family product architecture with compatible pinout, memory map and modular peripherals
  - Full documentation and a wide choice of development tools
- Product longevity
  - Advanced core and peripherals made in a state-of-the-art technology
  - Product family operating from 1.65 V to 3.6 V supply

Note: ProxSense ™ is a trademark of Azoteq (Pty) Ltd.

2 Description

The STM8TL52x4 and STM8TL53x4 devices feature the enhanced STM8 CPU core providing increased processing power (up to 16 MIPS at 16 MHz) while maintaining the advantages of a CISC architecture with improved code density, a 24-bit linear addressing space and an optimized architecture for low power operations. It uses a ProxSense charge transfer capacitive acquisition method that is capable of near range proximity detection.

The family includes an integrated debug module with a hardware interface (SWIM) which allows non-intrusive in-application debugging and ultrafast Flash programming. All STM8TL52x4 and STM8TL53x4 microcontrollers feature low-power low-voltage single-supply program Flash memory.

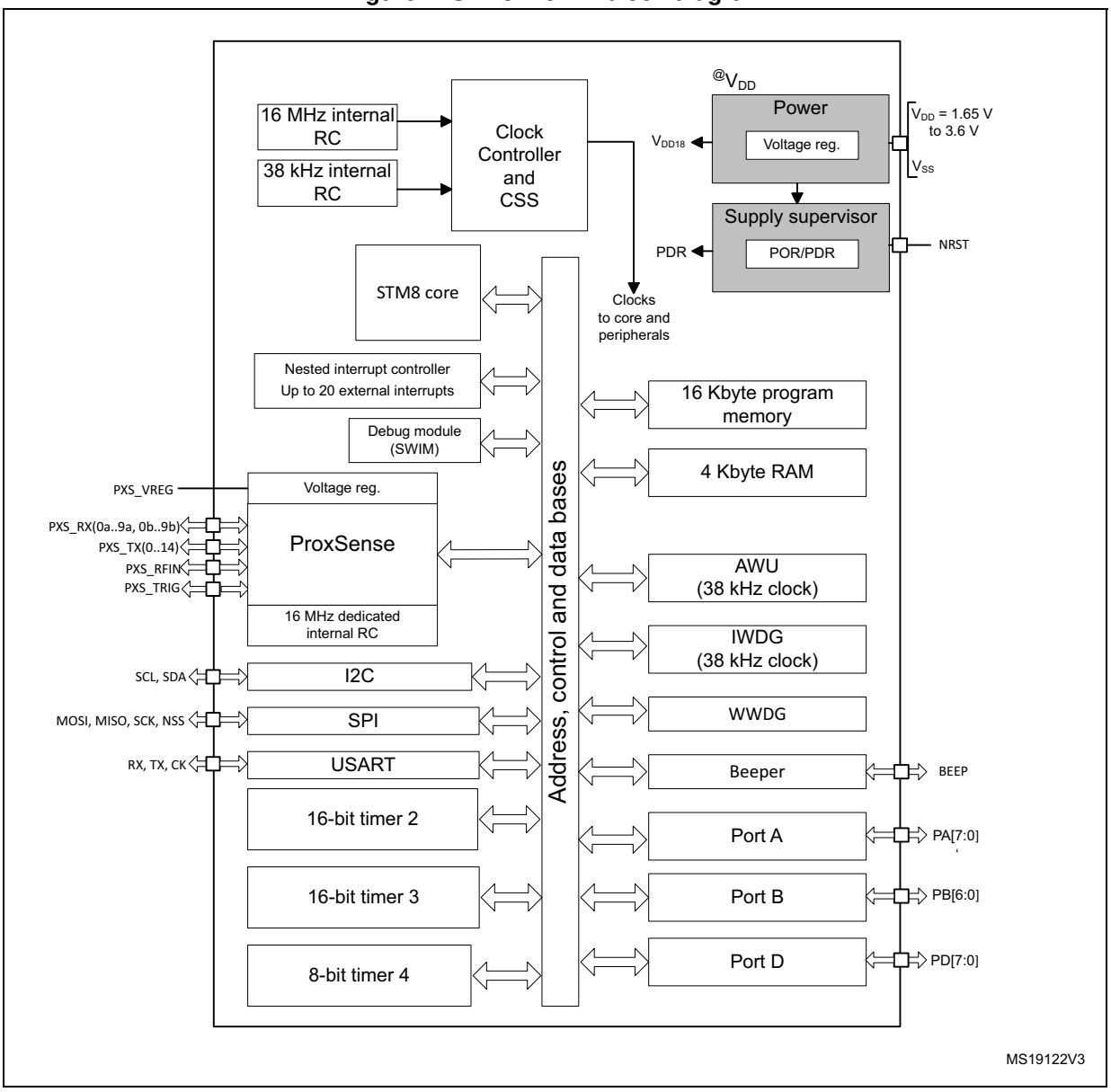
The STM8TL52x4 and STM8TL53x4 devices are based on a generic set of state-of-the-art peripherals. The modular design of the peripheral set allows the same peripherals to be found in different ST microcontroller families including 32-bit families. This makes any transition to a different family very easy, and simplified even more by the use of a common set of development tools.

Table 2. Device features

Features		STM8TL52F4	STM8TL53F4	STM8TL52G4	STM8TL53G4	STM8TL53C4
Flash (Kbyte)		16				
Data EEPROM (Kbyte)		2				
RAM (Kbyte)		4				
Timers	Basic	1 (8-bit)				
	General purpose	2 (16-bit)				
Communication Interfaces	SPI	1				
	I2C	1				
	USART	1				
GPIOs		12		17		23
ProxSense		Up to 12 touch sensing channels (5 receiver/ transmitter channels and 2 transmitter channels)	Up to 30 touch sensing channels (5 receiver/ transmitter channels and 6 transmitter channels)	Up to 25 touch sensing channels (8 receiver/ transmitter channels and 2 transmitter channels)	Up to 72 touch sensing channels (8 receiver/ transmitter channels and 9 transmitter channels)	Up to 300 touch sensing channels (20 receiver/ transmitter channels and 15 transmitter channels)
Others		Window watchdog, independent watchdog, two 16-MHz and one 38-kHz internal RC, auto-wakeup counter, beeper				
CPU frequency		16 MHz				
Operating voltage		1.65 to 3.6 V				
Operating temperature		-40 to +85 °C				
Packages		TSSOP20		UFQFPN28		UFQFPN48

3 Product overview

Figure 1. STM8TL5xx4 block diagram



Legend:

AWU: Auto-wakeup unit
Int. RC: internal RC oscillator
I²C: Inter-integrated circuit multimaster interface
POR/PDR: Power on reset / power down reset
SPI: Serial peripheral interface
SWIM: Single wire interface module
USART: Universal synchronous / asynchronous receiver / transmitter
IWDG: Independent watchdog
WWDG: Window watchdog
ProxSense™: capacitive sensing peripheral

3.1 Central processing unit STM8

The 8-bit STM8 core is designed for code efficiency and performance with an Harvard architecture and a 3-stage pipeline.

It contains 6 internal registers which are directly addressable in each execution context, 20 addressing modes including indexed indirect and relative addressing, and 80 instructions.

Architecture and registers

- Harvard architecture
- 3-stage pipeline
- 32-bit wide program memory bus - single cycle fetching most instructions
- X and Y 16-bit index registers - enabling indexed addressing modes with or without offset and read-modify - write type data manipulations
- 8-bit accumulator
- 24-bit program counter - 16 Mbyte linear memory space
- 16-bit stack pointer - access to a 64 Kbyte level stack
- 8-bit condition code register - 7 condition flags for the result of the last instruction

Addressing

- 20 addressing modes
- Indexed indirect addressing mode for lookup tables located anywhere in the address space
- Stack pointer relative addressing mode for local variables and parameter passing

Instruction set

- 80 instructions with 2-byte average instruction size
- Standard data movement and logic/arithmetic functions
- 8-bit by 8-bit multiplication
- 16-bit by 8-bit and 16-bit by 16-bit division
- Bit manipulation
- Data transfer between stack and accumulator (push/pop) with direct stack access
- Data transfer using the X and Y registers or direct memory-to-memory transfers

3.2 Development tools

Development tools for the STM8 microcontrollers include:

- The ST-Link very low-cost professional tool to debug and program
- The STVD high-level language debugger including C compiler, assembler and integrated development environment
- The STVP Flash programming software
- The STM-STUDIO real-time and non-intrusive graphical interface used to probe application variables and data

The STM8 also comes with starter kits, evaluation boards and low-cost in-circuit debugging/programming tools.

3.3 Single wire data interface (SWIM) and debug module

The debug module with its single wire data interface (SWIM) permits non-intrusive real-time in-circuit debugging and fast memory programming.

The Single wire interface is used for direct access to the debugging module and memory programming. The interface can be activated in all device operation modes.

The non-intrusive debugging module features a performance close to a full-featured emulator. Beside memory and peripherals, also CPU operation can be monitored in real-time by means of shadow registers.

3.4 Interrupt controller

The STM8TL5xx4 devices feature a nested vectored interrupt controller:

- Nested interrupts with 3 software priority levels
- 22 interrupt vectors with hardware priority
- Up to 22 external interrupt sources on 10 vectors
- TRAP and RESET interrupts

3.5 Memory

The STM8TL5xx4 devices have the following main features:

- 4 Kbyte of RAM
- The EEPROM is divided into two memory arrays (see the STM8TL5xxx reference manual (RM0312) for details on the memory mapping):
  - 16 Kbyte of low-density embedded Flash program including up to 2 Kbyte of data EEPROM. Data EEPROM and Flash program areas can be write protected independently by using the memory access security mechanism (MASS).
  - 64 option bytes (one block) of which 5 bytes are already used for the device.
  - Error correction code is implemented on the EEPROM.

3.6 Low power modes

To minimize power consumption, the product features three MCU low power modes:

- Wait mode: CPU clock stopped, selected peripherals at full clock speed.
- Active-halt mode:
  - When wakeup time is programmed in the AWU unit, the CPU and peripheral clocks are stopped. The RAM content is preserved.
  - When a ProxSense acquisition is ongoing, the wakeup is on ProxSense interrupts; the CPU and the other peripheral clocks are stopped.
- Halt mode: CPU and peripheral clocks are stopped, the device remains powered on. Wakeup is triggered by an external interrupt.

The ProxSense peripheral can return to low power mode between each conversion.
The ProxSense acquisition can be operated in Run, Wait and Active-halt modes.

3.7 Voltage regulators

The STM8TL5xx4 devices embed an internal voltage regulator for generating the 1.8 V power supply for the core and peripherals and a second internal voltage regulator providing a stable power supply (around 1.45V) for the ProxSense peripheral.

3.7.1 Dual-mode voltage regulator

This regulator has two different modes: main voltage regulator mode (MVR) and low power voltage regulator mode (LPVR). When in Active-halt mode, the regulator remains in MVR if ProxSense is active. When entering Halt or Active-halt modes, the system automatically switches from the MVR to the LPVR in order to reduce current consumption unless ProxSense is enabled.

3.7.2 ProxSense voltage regulator

This regulator provides a very stable voltage to power the ProxSense peripheral including ProxSense pins in order to be independent of any power supply variations. This regulator is switched on while the ProxSense peripheral is enabled (bit PXSEN = 1) and bit LOW_POWER is set to ‘0’ in register PXS_CR1. Otherwise, when LOW_POWER is set to ‘1’, this regulator is only enabled during conversions (while CIPF = 1 and SYNCPF = 0).

3.8 Clock control

The STM8TL5xx4 embeds a robust clock controller. It is used to distribute the system clock (SYSCLK) to the core and the peripherals and to manage clock gating for low power modes. This system clock is a 16-MHz High Speed Internal RC oscillator (HSI RC), followed by a programmable prescaler.

In addition, a 38 kHz low speed internal RC oscillator is used by the Independent watchdog (IWDG) and Auto-wakeup unit (AWU).

3.9 System configuration controller

The system configuration controller provides the capability to remap some alternate functions on different I/O ports. TIM3 channels can be remapped.

3.10 Independent watchdog

The independent watchdog (IWDG) peripheral can be used to resolve processor malfunctions due to hardware or software failures.

It is clocked by the 38 kHz LSI internal RC clock source, and thus stays active even in case of a CPU clock failure.

3.11 Window watchdog

The window watchdog (WWDG) is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.12 Auto-wakeup counter

The auto-wakeup (AWU) counter is used to wakeup the device from Active-halt mode.

3.13 General purpose and basic timers

STM8TL5xx4 devices contain two 16-bit general purpose timers (TIM2 and TIM3) and one 8-bit basic timer (TIM4).

16-bit general purpose timers

The 16-bit timers consist of 16-bit up/down auto-reload counters driven by a programmable prescaler. They perform a wide range of functions, including:

- Timebase generation
- Measuring the pulse lengths of input signals (input capture)
- Generating output waveforms (output compare, PWM and One pulse mode)
- Interrupt capability on various events (capture, compare, overflow, break, trigger)
- Synchronization with other timers or external signals (external clock, reset, trigger and enable)

8-bit basic timer

The 8-bit timer consists of an 8-bit up auto-reload counter driven by a programmable prescaler. It can be used for timebase generation with interrupt generation on timer overflow.

3.14 Beeper

STM8TL5xx4 devices include a beeper function used to generate a beep signal in the range of 1, 2 or 4 kHz when the LSI clock is operating at a frequency of 38 kHz.

3.15 USART

The USART interface (USART) allows full duplex, asynchronous communications with external devices requiring an industry standard NRZ asynchronous serial data format. It offers a very wide range of baud rates.

- 1 Mbit/s full duplex SCI
- SPI emulation
- High precision baud rate generator
- Single wire half duplex mode

3.16 SPI

The serial peripheral interface (SPI) provides half/ full duplex synchronous serial communication with external devices.

- Maximum speed: 8 Mbit/s ($f_{SYSCLK/2)}$ both for master and slave
- Full duplex synchronous transfers
- Simplex synchronous transfers on 2 lines with a possible bidirectional data line
- Master or slave operation - selectable by hardware or software
- Hardware CRC calculation
- Slave/master selection input pin

3.17 I^2C

The I^2C bus interface (I^2C) provides multi-master capability, and controls all I^2C bus-specific sequencing, protocol, arbitration and timing.

- Master, slave and multi-master capability
- Dual addressing mode capability
- Standard mode up to 100 kHz and fast speed modes up to 400 kHz
- 7-bit and 10-bit addressing modes
- Hardware CRC calculation

3.18 ProxSense

The ProxSense peripheral uses a charge-transfer method to detect capacitance changes.

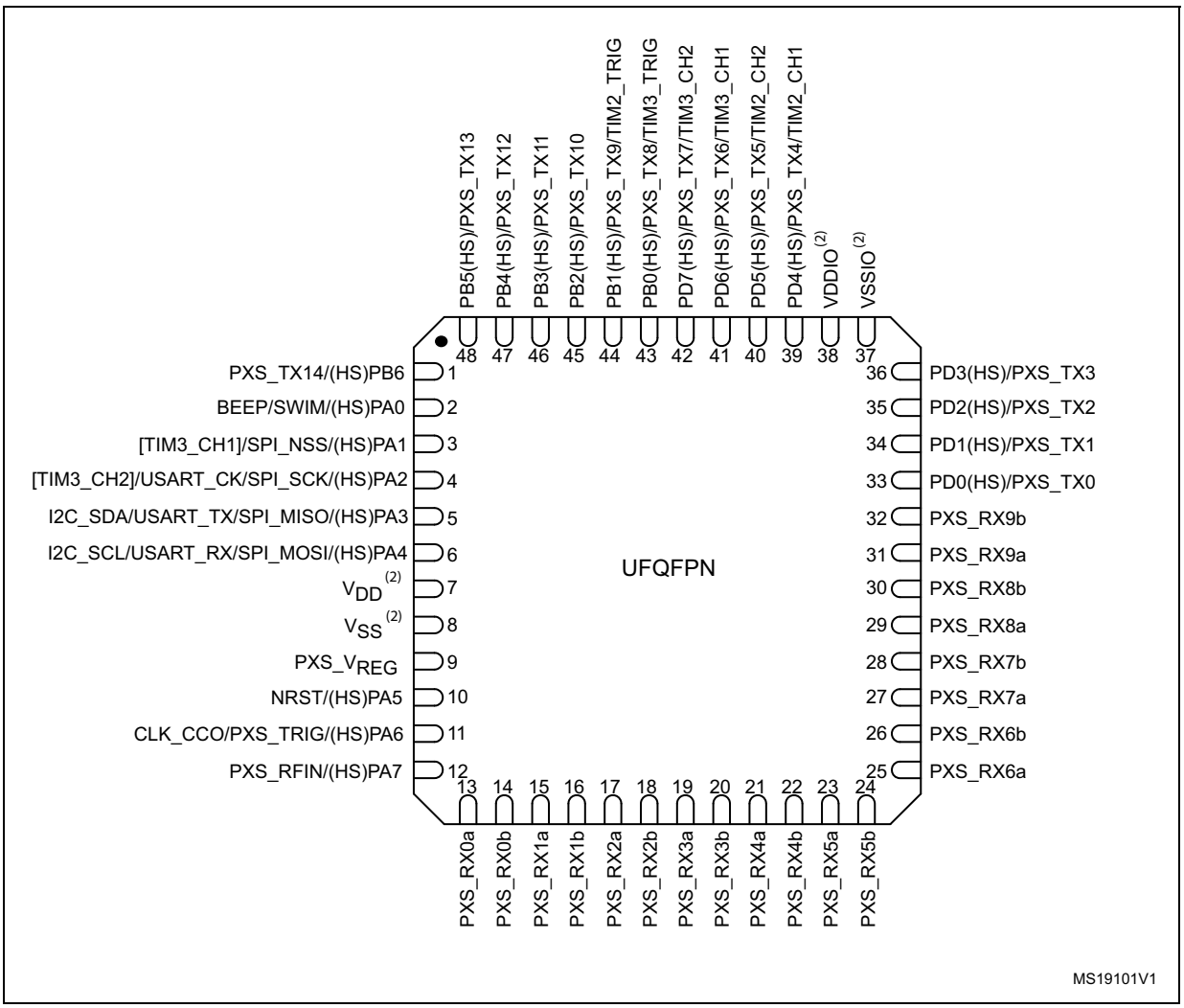
- Up to 300 capacitive sensing channels composed of 15 transmitters and 20 receivers with up to 10 Rx channels acquired in parallel
- Fast acquisition with a typical scan time of 250 µs for 10 Rx channels
- Configurable internal sampling capacitor (C_S)
- Electrode Parasitic Capacitance Compensation (EPCC) to ensure the best sensitivity in all user environments
- RF noise detection, allowing to reject corrupted samples
- External trigger to de-synchronize the acquisition from known noise
- Can be configured to return to low power mode between each conversion
- Acquisition possible in Run, Wait and Active-halt modes

3.19 TouchSensing dedicated library available upon request

- Complete C source code library with firmware examples (MISRA compliant)
- Multifunction capability to combine capacitive sensing functions with traditional MCU features
- Compatible with proximity, touchkey, linear and rotary touch sensor implementation
- Configuration of all ProxSense parameters
- Extra filtering and calibration functions
- TouchSensing user interface through firmware API for status reporting and application configuration
- Compliance with Cosmic, IAR and Raisonance C compilers

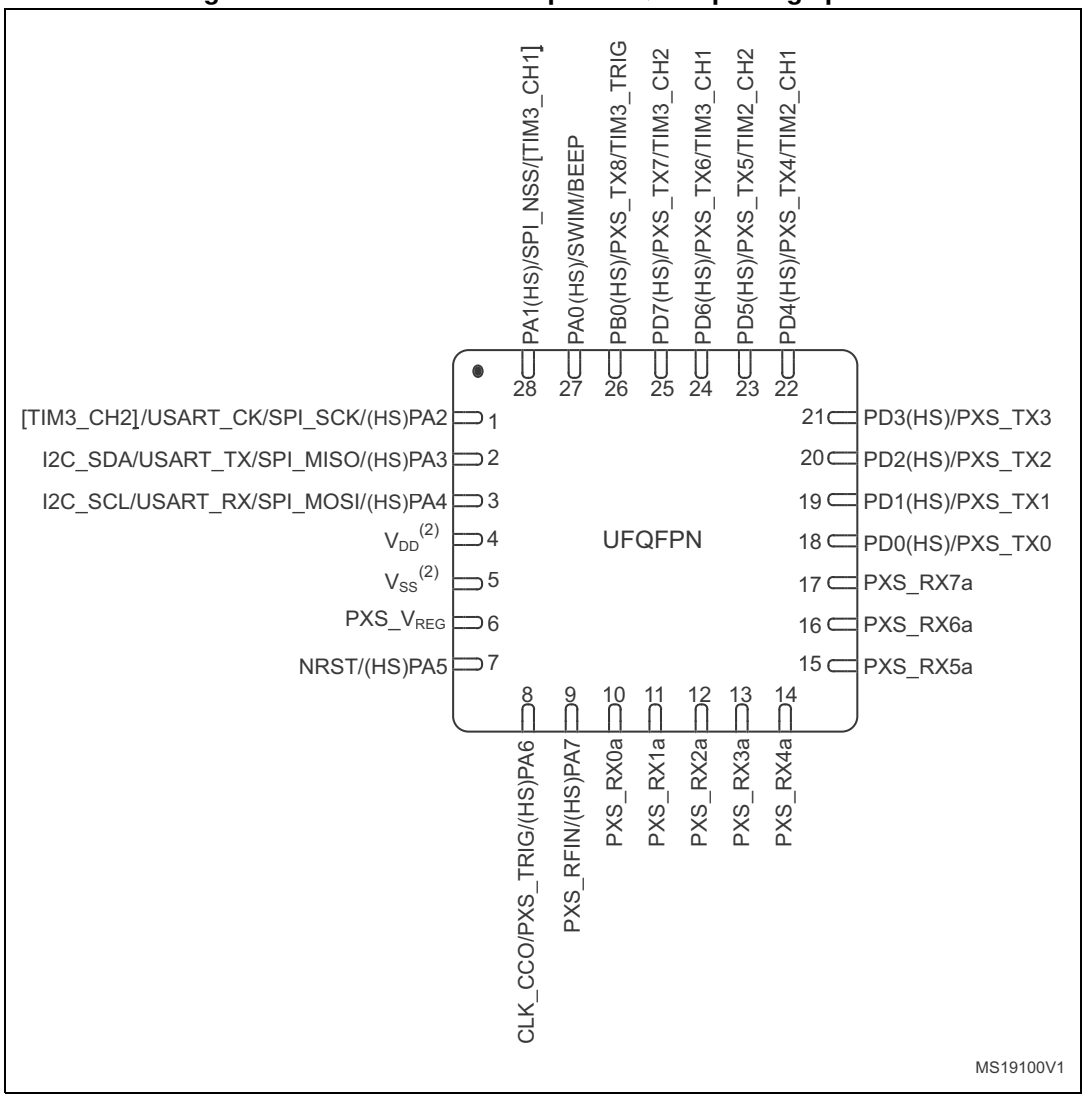
4 Pin description

Figure 2. STM8TL53 48-pin UFQFPN package pinout



1. HS corresponds to 20 mA high sink/source capability.
2. Power supply pins must be correctly decoupled with capacitors near the pins. Please refer to the power supply circuitry details in *Section 9.3.2: Power supply on page 46* and the STM8TL5xxx reference manual (RM0312), Section 6: Power supply.

Figure 3. STM8TL53G4U6 28-pin UFQFPN package pinout



1. HS corresponds to 20 mA high sink/source capability.
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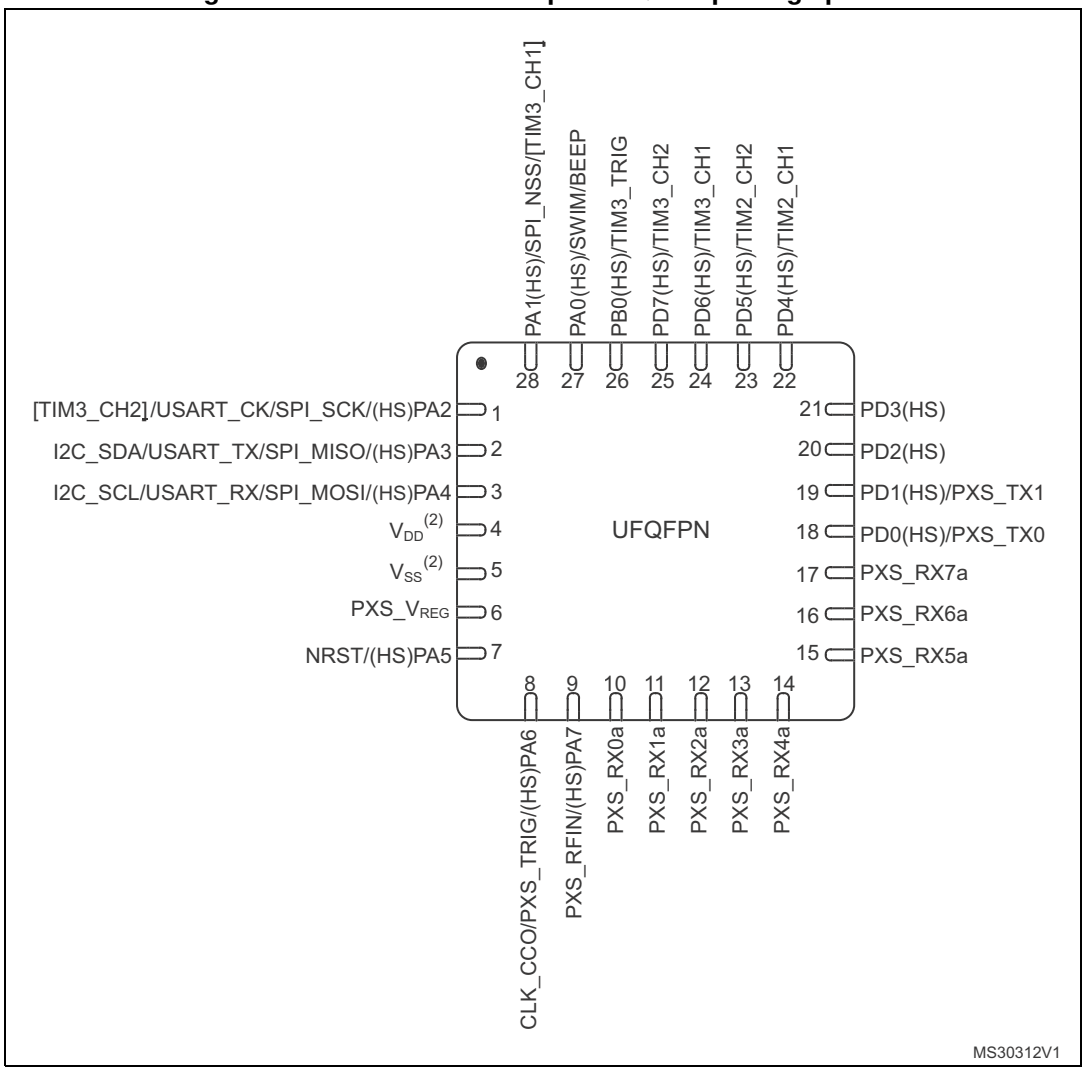
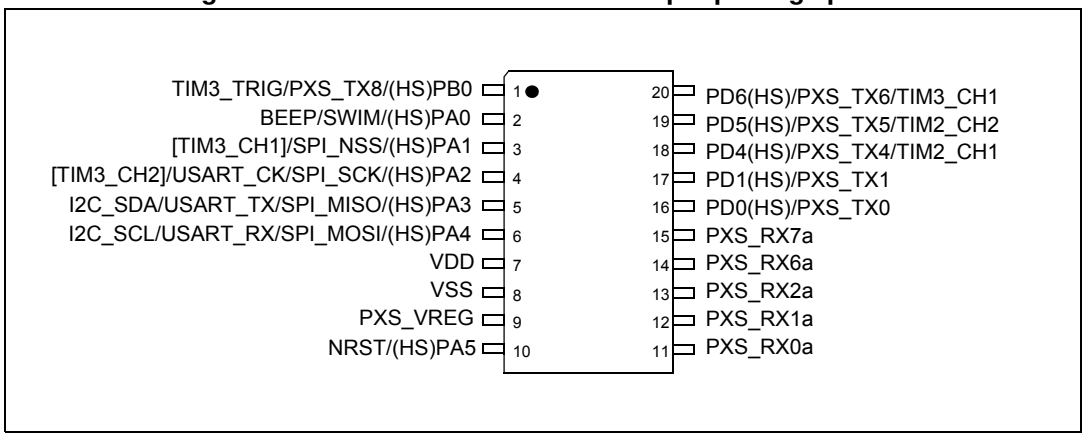
Figure 4. STM8TL52G4U6 28-pin UFQFPN package pinout



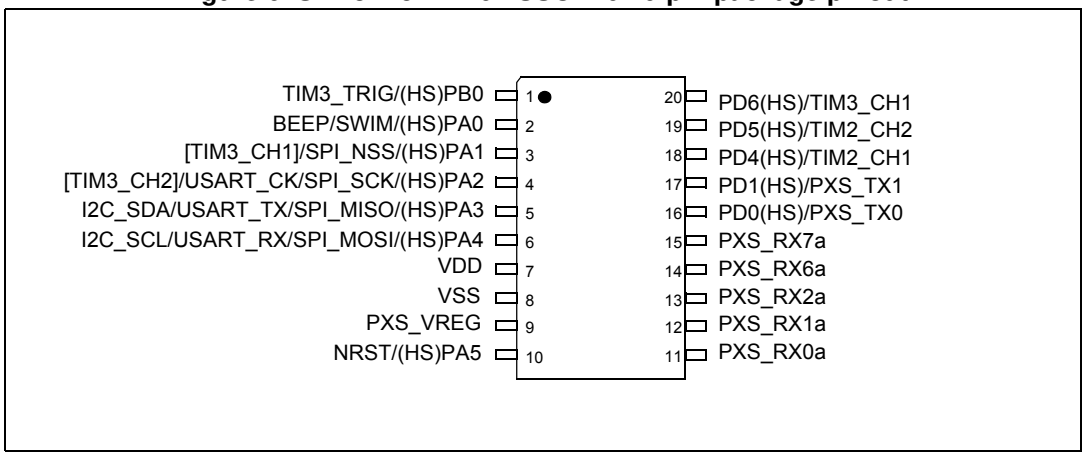
1. HS corresponds to 20 mA high sink/source capability.
2. Power supply pins must be correctly decoupled with capacitors near the pins. Please refer to the power supply circuitry details in *Section 9.3.2: Power supply on page 46* and the STM8TL5xxx reference manual (RM0312) Section 6: Power supply.

Figure 5. STM8TL53F4P6 TSSOP20 20-pin package pinout



1. HS corresponds to 20 mA high sink/source capability.
2. Power supply pins must be correctly decoupled with capacitors near the pins. Please refer to the power supply circuitry details in *Section 9.3.2: Power supply on page 46* and the STM8TL5xxx reference manual (RM0312) Section 6: Power supply.

Figure 6. STM8TL52F4P6 TSSOP20 20-pin package pinout



1. HS corresponds to 20 mA high sink/source capability.
2. Power supply pins must be correctly decoupled with capacitors near the pins. Please refer to the power supply circuitry details in *Section 9.3.2: Power supply on page 46* and the STM8TL5xxx reference manual (RM0312) Section 6: Power supply.

Table 3. Legends/abbreviations

Type	I = input, O = output, S = power supply	
Level	Input	FT = 5 V tolerant, TC = 3 V capable
	Output	HS = high sink/source (20 mA)
Port and control configuration	Input	float = floating, wpu = weak pull-up
	Output	T = true open drain, OD = open drain, PP = push-pull
Reset state	Bold X (pin state after reset release). Unless otherwise specified, the pin state is the same during the reset phase (i.e. “under reset”) and after internal reset release (i.e. at reset state).	

Table 4. STM8TL5xx4 pin description

Pin no.			Pin name	Type	Input				Output			Main function (after reset)	Alternate function	
UFQFPN48	UFQFPN28	TSSOP20			Level	floating	wpu	Ext. interrupt	High sink/source	OD	PP		Default	Remap
1	-	-	PB6/ PXS_TX14	I/O	TC	X	X	X	HS	X	X	Port B6	ProxSense transmit 14	-
2	27	2	PA0[1]/SWIM/ BEEP	I/O	TC	X	X	X	HS	X	X	SWIM	Port A0[1]	-
													SWIM input and output	-
													Beep output	-
3	28	3	PA1/SPI_NSS/ [TIM3_CH1]	I/O	FT	X	X	X	HS	X	X	Port A1	SPI master/ slave select	Timer 3 - channel 1
4	1	4	PA2/SPI_SCK/ USART_CK/ [TIM3_CH2][2]	I/O	FT	X	X	X	HS	X	X	Port A2	SPI clock	Timer 3 - channel 2
													USART synchronous clock	
5	2	5	PA3/SPI_MISO/ USART_TX/ I2C_SDA[2]	I/O	FT	X	X	X	HS	X	X	Port A3	SPI master in/ slave out	-
													USART transmit	-
													I^2C data	-
6	3	6	PA4/SPI_MOSI/ USART_RX/ I2C_SCL	I/O	FT	X	X	X	HS	X	X	Port A4	SPI master out/ slave in	-
													USART receive	-
													I^2C clock	-
7	4	7	VDD	S	-	-	-	-	-	-	-	Digital power supply	-	-

Table 4. STM8TL5xx4 pin description (continued)

Pin no.			Pin name	Type	Input				Output			Main function (after reset)	Alternate function	
UFQFPN48	UFQFPN28	TSSOP20			Level	floating	wpu	Ext. interrupt	High sink/source	OD	PP		Default	Remap
8	5	8	VSS	S	-	-	-	-	-	-	-	Digital ground	-	-
9	6	9	PXS_VREG	S	-	-	-	-	-	-	-	-	ProxSense voltage regulator External decoupling capacitor	-
10	7	10	PA5/NRST(3)	I/O	TC	-	-	-	HS	X	X	Reset	Port A5 (output only)	-
11	8	-	PA6/ PXS_TRIG/ CLK_CCO	I/O	FT	X	X	X	HS	X	X	Port A6	ProxSense external trigger input	-
		-											CLK clock output	-
12	9	-	PA7/PXS_RFIN	I/O	TC	X	X	X	HS	X	X	Port A7	ProxSense antenna input	-
13	10	11	PXS_RX0a	-	-	-	-	-	-	-	-	PXS_RX0a	ProxSense receiver 0a	-
14	-	-	PXS_RX0b	-	-	-	-	-	-	-	-	PXS_RX0b	ProxSense receiver 0b	-
15	11	12	PXS_RX1a	-	-	-	-	-	-	-	-	PXS_RX1a	ProxSense receiver 1a	-
16	-	-	PXS_RX1b	-	-	-	-	-	-	-	-	PXS_RX1b	ProxSense receiver 1b	-
17	12	13	PXS_RX2a	-	-	-	-	-	-	-	-	PXS_RX2a	ProxSense receiver 2a	-
18	-	-	PXS_RX2b	-	-	-	-	-	-	-	-	PXS_RX	ProxSense receiver 2b	-
19	13	-	PXS_RX3a	-	-	-	-	-	-	-	-	PXS_RX3a	ProxSense receiver 3a	-
20	-	-	PXS_RX3b	-	-	-	-	-	-	-	-	PXS_RX3b	ProxSense receiver 3b	-
21	14	-	PXS_RX4a	-	-	-	-	-	-	-	-	PXS_RX4a	ProxSense receiver 4a	-
22	-	-	PXS_RX4b	-	-	-	-	-	-	-	-	PXS_RX4b	ProxSense receiver 4b	-

Table 4. STM8TL5xx4 pin description (continued)

Pin no.			Pin name	Type	Input				Output			Main function (after reset)	Alternate function	
UFQFPN48	UFQFPN28	TSSOP20			Level	floating	wpu	Ext. interrupt	High sink/source	OD	PP		Default	Remap
23	15	-	PXS_RX5a	-	-	-	-	-	-	-	-	PXS_RX5a	ProxSense receiver 5a	-
24	-	-	PXS_RX5b	-	-	-	-	-	-	-	-	PXS_RX5b	ProxSense receiver 5b	-
25	16	14	PXS_RX6a	-	-	-	-	-	-	-	-	PXS_RX6a	ProxSense receiver 6a	-
26	-	-	PXS_RX6b	-	-	-	-	-	-	-	-	PXS_RX6b	ProxSense receiver 6b	-
27	17	15	PXS_RX7a	-	-	-	-	-	-	-	-	PXS_RX7a	ProxSense receiver 7a	-
28	-	-	PXS_RX7b	-	-	-	-	-	-	-	-	PXS_RX7b	ProxSense receiver 7b	-
29	-	-	PXS_RX8a	-	-	-	-	-	-	-	-	PXS_RX8a	ProxSense receiver 8a	-
30	-	-	PXS_RX8b	-	-	-	-	-	-	-	-	PXS_RX8b	ProxSense receiver 8b	-
31	-	-	PXS_RX9a	-	-	-	-	-	-	-	-	PXS_RX9a	ProxSense receiver 9a	-
32	-	-	PXS_RX9b	-	-	-	-	-	-	-	-	PXS_RX9b	ProxSense receiver 9b	-
33	18	16	PD0/PXS_TX0	I/O	TC	X	X	X	HS	X	X	Port D0	ProxSense transmitter 0	-
34	19	17	PD1/PXS_TX1	I/O	TC	X	X	X	HS	X	X	Port D1	ProxSense transmitter 1	-
35	20	-	PD2/PXS_TX2(4)	I/O	TC	X	X	X	HS	X	X	Port D2	ProxSense transmitter 2(4)	-
36	21	-	PD3/PXS_TX3(4)	I/O	TC	X	X	X	HS	X	X	Port D3	ProxSense transmitter 3(4)	-
37	-	-	VSSIO	S	-	-	-	-	-	-	-	IOs ground	-	-
38	-	-	VDDIO	S	-	-	-	-	-	-	-	IOs power supply	-	-
39	22	18	PD4/PXS_TX4(4) / TIM2_CH1	I/O	TC	X	X	X	HS	X	X	Port D4	ProxSense transmitter 4(4)	-
													Timer 2 - channel 1	-

Table 4. STM8TL5xx4 pin description (continued)

Pin no.			Pin name	Type	Input				Output			Main function (after reset)	Alternate function	
UFQFPN48	UFQFPN28	TSSOP20			Level	floating	wpu	Ext. interrupt	High sink/source	OD	PP		Default	Remap
40	23	19	PD5/PXS_TX5(4) / TIM2_CH2	I/O	TC	X	X	X	HS	X	X	Port D5	ProxSense transmitter 5(4)	-
													Timer 2 - channel 2	-
41	24	20	PD6/PXS_TX6(4) / TIM3_CH1	I/O	TC	X	X	X	HS	X	X	Port D6	ProxSense transmitter 6(4)	-
													Timer 3 - channel1	-
42	25		PD7/PXS_TX7(4) / TIM3_CH2	I/O	TC	X	X	X	HS	X	X	Port D7	ProxSense transmitter 7(4)	-
													Timer 3 - channel 2	-
43	26	1	PB0/PXS_TX8(4) / TIM3_ETR	I/O	TC	X	X	X	HS	X	X	Port B0	ProxSense transmitter 8(4)	-
													Timer 3 - external trigger	-
44	-	-	PB1(2)/PXS_TX9 / TIM2_ETR	I/O	TC	X	X	X	HS	X	X	Port B1	ProxSense transmitter 9	-
	-	-											Timer 2 - external trigger	-
45	-	-	PB2/PXS_TX10	I/O	TC	X	X	X	HS	X	X	Port B2	ProxSense transmitter 10	-
46	-	-	PB3/PXS_TX11	I/O	TC	X	X	X	HS	X	X	Port B3	ProxSense transmitter 11	-
47	-	-	PB4/PXS_TX12	I/O	TC	X	X	X	HS	X	X	Port B4	ProxSense transmitter 12	-
48	-	-	PB5/PXS_TX13	I/O	TC	X	X	X	HS	X	X	Port B5	ProxSense transmitter 13	-

1. The PA0/SWIM pin is in input pull-up during the reset phase and after reset release.
2. A pull-up is applied to PA2, PA3 and PB1 during the reset phase. These three pins are input floating after reset release.
3. At power-up, the PA5/NRST pin is a reset input pin with pull-up. To be used as a general purpose pin (PA5), it can be configured only as output open-drain or push-pull, not as a general purpose input. Refer to Section Configuring NRST/PA5 pin as general purpose output in the STM8TL5xxx reference manual (RM0312).
4. Not available for STM8TL52xx.