Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

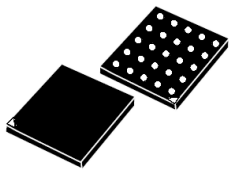
Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

STMPE1601

16-bit enhanced port expander with keypad and PWM controller Xpander Logic™

Features

- 16 GPIOs
  (8 operate at core supply V_{CC} , 8 operate at IO supply V_{IO})
- Operating voltage 1.8 –3.3 V
- Hardware keypad controller (8*8 matrix with 4 optional dedicated keys max)
- Keypad controller capable of detecting key-press in hibernation mode
- 4 basic PWM controllers for LED brightness control
- Interrupt output (open drain) pin
- Optional 32 kHz clock input
- 8-channel programmable level translator
- Advanced power management system
- Ultra-low standby-mode current
- Package TFBGA25 (3 x 3 mm)



TFBGA25

Description

The STMPE1601 is a GPIO (general purpose input/output) port expander able to interface a main digital ASIC via the two-line bidirectional bus (I^2C). A separate GPIO expander IC is often used in mobile multimedia platforms to solve the problems of the limited number of GPIOs typically available on the digital engine.

The STMPE1601 offers great flexibility, as each I/O can be configured as input, output or specific functions. The device is able to scan a keyboard, also provides PWM outputs for brightness control in backlight, and GPIO function. This device has been designed to include very low quiescent current, and a wake-up feature for each I/O, to optimize the power consumption of the IC.

Potential applications of the STMPE1601 include portable media players, game consoles, mobile and smart phones.

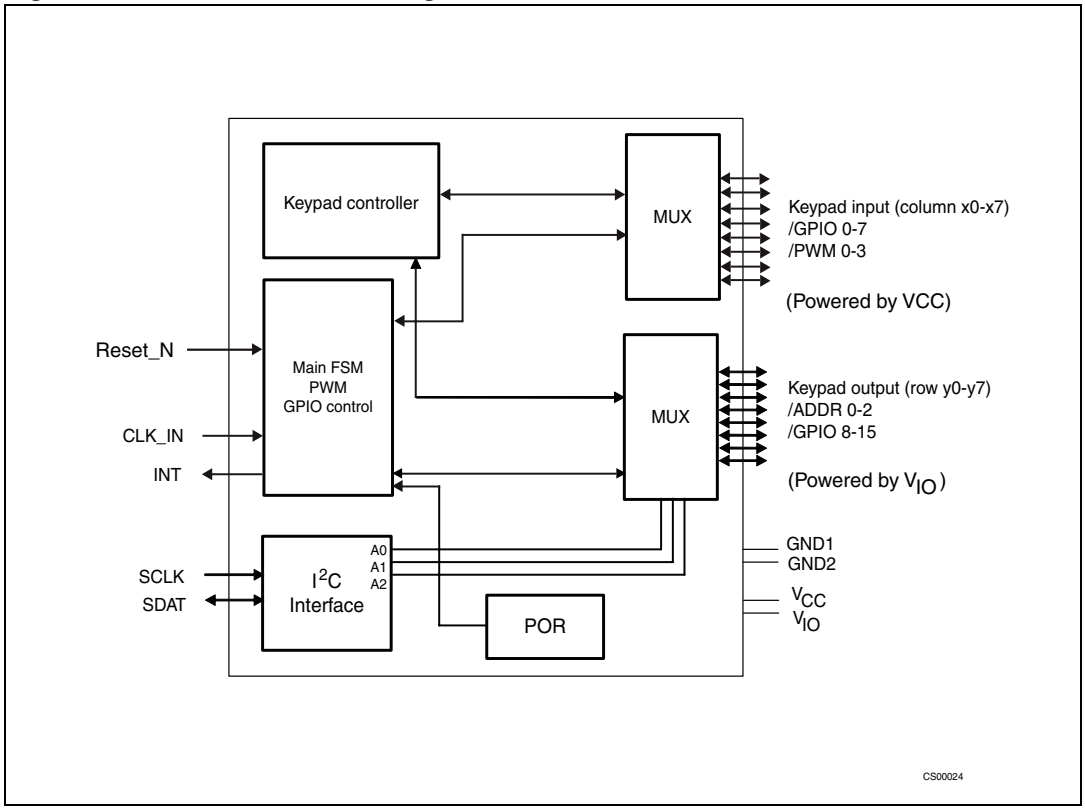
Table 1. Device summary

Order code	Package	Packaging
STMPE1601TBR	TFBGA25	Tape and reel

Contents

1 Block diagram

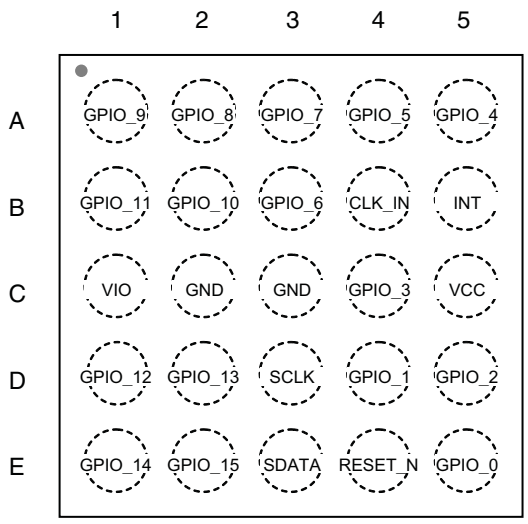
Figure 1. STMPE1601 block diagram



2 Pin settings

2.1 Pin connection

Figure 2. Pin connection (top-through view)



TFBGA25

AM00757V1

2.2 Pin assignment and TFBGA ball location

Table 2. Pin assignment

Ball name	Name	Type	Domain	Description
E5	GPIO_0	I/O	V_{CC}	GPIO 0/ KP_X0/ PWM_0
D4	GPIO_1	I/O	V_{CC}	GPIO 1/ KP_X1/ PWM_1
D5	GPIO_2	I/O	V_{CC}	GPIO 2/ KP_X2/ PWM_2
C4	GPIO_3	I/O	V_{CC}	GPIO 3/ KP_X3/ PWM_3
A5	GPIO_4	I/O	V_{CC}	GPIO 4/ KP_X4
A4	GPIO_5	I/O	V_{CC}	GPIO 5/ KP_X5
B3	GPIO_6	I/O	V_{CC}	GPIO 6/ KP_X6
A3	GPIO_7	I/O	V_{CC}	GPIO 7/ KP_X7
A2	GPIO_8	I/O	V_{IO}	GPIO 8/ KP_Y0
A1	GPIO_9	I/O	V_{IO}	GPIO 9/ KP_Y1
B2	GPIO_10	I/O	V_{IO}	GPIO 10/ KP_Y2

Table 2. Pin assignment (continued)

Ball Name	Name	Type	Domain	Description
B1	GPIO_11	IO	V_{IO}	GPIO 11/ KP_Y3
D1	GPIO_12	IO	V_{IO}	GPIO 12/ KP_Y4
D2	GPIO_13	IO	V_{IO}	GPIO 13/ KP_Y5/ ADDR0
E1	GPIO_14	IO	V_{IO}	GPIO 14/ KP_Y6/ ADDR1
E2	GPIO_15	IO	V_{IO}	GPIO 15/ KP_Y7/ ADDR2
B5	INT	O	V_{CC}	Open drain interrupt output pin. INT pin to be externally pulled up to V_{CC}(or > V_{CC}, < 3.6 V), or pulled down to GND, depending on polarity of interrupt (must not be left floating).
E4	Reset_N	I	V_{CC}	External reset input, active LOW. Reset_N pulse width must be ≥ 20 µs. This pin is internally pulled up to V_{CC}.
E3	SDATA	A	V_{CC}	I^2C DATA (tolerant to 3.6 V)
D3	SCLK	A	V_{CC}	I^2C clock (tolerant to 3.6 V)
B4	CLK_IN	A	V_{CC}	32 kHz input. To be pulled-up to V_{CC} with 10 k resistor if clock is not used. This pin is internally pulled to V_{CC}.
C5	VCC	–	–	1.8 –3.3 V input for I^2C module and digital core
C1	VIO	–	–	1.8 –3.3 V input for GPIO. The VIO must be ≥ V_{CC}.
C2	GND	–	–	Ground
C3	GND	–	–	Ground

2.3 Ball mapping to TFBGA (top through view)

Table 3. Pin mapping

	1	2	3	4	5
A	GPIO_9	GPIO_8	GPIO_7	GPIO_5	GPIO_4
B	GPIO_11	GPIO_10	GPIO_6	CLK_IN	INT
C	VIO	GND	GND	GPIO_3	VCC
D	GPIO_12	GPIO_13	SCLK	GPIO_1	GPIO_2
E	GPIO_14	GPIO_15	SDATA	RESET_N	GPIO_0

2.4 GPIO pin functions

Table 4. GPIO pin functions

Name	Primary function	Alternate function 1	Alternate function 2	Note
GPIO_0	GPIO	Keypad	PWM	–
GPIO_1	GPIO	Keypad	PWM	–
GPIO_2	GPIO	Keypad	PWM	–
GPIO_3	GPIO	Keypad	PWM	–
GPIO_4	GPIO	Keypad	–	–
GPIO_5	GPIO	Keypad	–	–
GPIO_6	GPIO	Keypad	–	–
GPIO_7	GPIO	Keypad	–	–
GPIO_8	GPIO	Keypad	–	–
GPIO_9	GPIO	Keypad	–	–
GPIO_10	GPIO	Keypad	–	–
GPIO_11	GPIO	Keypad	–	–
GPIO_12	GPIO	Keypad	–	–
GPIO_13	GPIO	Keypad	–	I^2C ADDR during RESET
GPIO_14	GPIO	Keypad	–	I^2C ADDR during RESET
GPIO_15	GPIO	Keypad	–	I^2C ADDR during RESET

3 Maximum ratings

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3.1 Absolute maximum ratings

Table 5. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	4.5	V
V_{IN}	Input voltage on GPIO pin	4.5	V
VESD (HBM)	ESD protection on each GPIO pin	2	kV

3.2 Thermal data

Table 6. Thermal data

Symbol	Parameter	Min	Typ	Max	Unit
R_{thJA}	Thermal resistance junction-ambient	-	100	–	°C/W
T_A	Operating ambient temperature	-40	25	85	°C
T_J	Operating junction temperature	-40	25	125	°C

4 Electrical specification

4.1 DC electrical characteristics

Table 7. DC electrical characteristics

Symbol	Parameter	Test conditions	Value			Unit
			Min	Typ	Max	
V_{CC}	1.8 V supply voltage		1.65	–	3.6	V
V_{IO}	IO supply voltage		1.65	–	3.6	V
I_{CC}	Active current	V_{IO} V_{CC} = 1.8 V T= 25 °C	–	1.2	1.6	mA
I_{SLEEP}	Sleep current		–	18	25	µA
$I_{HIBERNATE}$	Hibernate current		–	0.5	1.5	µA
I_{CC}	Active current	V_{IO} V_{CC} = 3.3 V T= 25 °C	–	3.0	3.8	mA
I_{SLEEP}	Sleep current		–	50	60	µA
$I_{HIBERNATE}$	Hibernate current(1)		–	1.2	3	µA
I_{CC}	Active current	V_{IO} V_{CC} = 1.8 V T= 85 °C	–	–	2	mA
I_{SLEEP}	Sleep current		–	–	32	µA
$I_{HIBERNATE}$	Hibernate current		–	–	2	µA
I_{CC}	Active current	V_{IO} V_{CC} = 3.3 V T= 85 °C	–	–	4.8	mA
I_{SLEEP}	Sleep current		–	–	75	µA
$I_{HIBERNATE}$	Hibernate current(1)		–	–	5	µA
INT	Open drain output current		–	4	–	mA

1. If only the basic GPIO function is required, the STMPE1601 can be designed to work mostly in hibernate mode. Active mode is used only when there are changes in the I/O status.

4.2 Input/Output DC electrical characteristics

The 1.8 V I/O complies to the EIA/JEDEC standard JESD8-7.

Table 8. I/O DC electrical characteristic

Symbol	Parameter		Value			Unit
			Min	Typ	Max	
V_{il}	Low level input voltage	V_{IO} = 1.8 V	–	–	0.63	V
V_{ih}	High level input voltage	V_{IO} = 1.8 V	1.17	–	–	V
V_{hyst}	Schmitt trigger hysteresis	V_{IO} = 1.8 V	–	0.10	–	V
V_{il}	Low level input voltage	V_{IO} = 3.3 V	–	–	1.15	V
V_{ih}	High level input voltage	V_{IO} = 3.3 V	2.14	–	–	V
V_{hyst}	Schmitt trigger hysteresis	V_{IO} = 3.3 V	–	0.20	–	V

Table 9. DC input specification (1.55 V < V_{CC} < 1.95 V)

Symbol	Parameter	Test conditions	Value			Unit
			Min	Typ	Max	
V_{ol}	Low level output voltage	I_{ol} = 4 mA V_{IO} = 1.8 V	–	–	0.45	V
V_{oh}	High level output voltage	I_{oh} = 4 mA V_{IO} = 1.8 V	1.35	–	–	V
V_{ol}	Low level output voltage	I_{ol} = 4 mA V_{IO} = 3.3 V	–	–	0.83	V
V_{oh}	High level output voltage	I_{oh} = 4 mA V_{IO} = 3.3 V	2.48	–	–	V

Table 10. DC output specification (1.55 V < V_{CC} < 1.95 V)

Symbol	Parameter	Test conditions	Value			Unit
			Min	Typ	Max	
I_{pu}	Pull-up current	V_I = 0 V	15	35	65	µA
R_{up}(1)	Equivalent pull-up resistance	V_{CC} = 3.3 V	30	60	90	kΩ
		V_{CC} = 1.8 V	50	100	150	kΩ
R_{up}(2)	Equivalent pull-up resistance	V_{IO} = 3.3 V	30	60	90	kΩ
		V_{IO} = 1.8 V	50	100	150	kΩ

1. Applicable to GPIO_0 to GPIO_7.
2. Applicable to GPIO_8 to GPIO_15.

5 Register map

All the registers have the size of 8-bit. For each of the module, their registers are residing within the given address range.

Table 11. Register map summary table

Address	Module register	Description	**Auto-increment** (during read/write)
0x00 – 0x07 0x80 – 0x81	Clock and power manager module	Clock and power manager register range	Yes
0x10 – 0x1F	Interrupt controller module	Interrupt controller register range	Yes
0x40 – 0x5F	PWM controller module	PWM controller register range	Yes
0x60 – 0x6F	Keypad controller module	Keypad controller register range	Yes
0x70 – 0x77	Rotator controller module	Rotator controller register range	Yes
0x80 – 0xBF	GPIO controller module	GPIO controller register range	Yes

6 I²C interface

The features supported by the I²C interface are listed below:

- I²C slave device
- Operates at V_{CC} (1.8 - 3.3 V)
- Compliant to Philips I²C specification version 2.1
- Supports standard (up to 100kbps) and fast (up to 400 kbps) modes
- 7-bit and 10-bit device addressing modes
- General Call
- Start/Restart/Stop
- Address up to 8 STMPE1601 devices via the I²C interface

The address is selected by the state of 3 pins. The state of the pins is read upon reset and then the pins can be configured for normal operation. The pins have a pull-up or pull-down to set the address. The I²C interface module allows the connected host system to access the registers in the STMPE1601.

Table 12. I²C addresses

A2	A1	A0	7-bit address
0	0	0	40h
0	0	1	41h
0	1	0	42h
0	1	1	43h
1	0	0	44h
1	0	1	45h
1	1	0	46h
1	1	1	47h

6.1 Minimizing current drain on I²C address lines

The GPIOs 13-15 are used as I²C address input during POR. Pull-up/down resistor of 500 kΩ - 1.5 MΩ is recommended for these address lines. In the case that these pins are driven to an opposite logic level during device operation, there would be a current drain of V_{IO}/R. This amounts to a significant current drain for portable devices.

To minimize the current drain on I²C lines, two methods are recommended:

1. If maximum keypad size is not required, these shared lines should not be used for keypad operation.
2. If the maximum keypad size is required, choose I²C address 0x40, as this requires all 3 address lines to be pulled to ground, minimizing the current drain in the keypad operation. In this mode of operation, the recommended pull up/down resistors on the I²C lines are listed in *Table 13*.

   A reset circuit with longer RC is used to ensure enough time for the address lines to settle to the final values.
3. In system-controlled idle state, all the keypad pins are to be configured as hotkey with interrupt function enabled. If any key is pressed, the system initiates the keypad controller for scanning operation.

Table 13. Recommended pull up/down resistors on the I²C lines

Pull up/down resistor	V_{IO}			Reset RC or pulse width(1)	Note
	1.8 V	2.5 V	3.3 V		
R_{PU}/R_{PD}	1.5 MΩ	1.2 MΩ	1 MΩ	270 kΩ/0.47 µF 120 ms	All 3 address lines are used for keypad controller
R_{PU}/R_{PD}	1.0 MΩ	800 kΩ	660 kΩ	180 kΩ/0.47 µF 80 ms	2 address lines are used for keypad controller
R_{PU}/R_{PD}	500 kΩ	400 kΩ	330 kΩ	90kΩ/0.47 µF 40 ms	1 address line is used for keypad controller

1. Recommended values are chosen to minimize leakage current.

6.2 Start condition

A Start condition is identified by a falling edge of SDATA while SCLK is stable at high state. A Start condition must precede any data/command transfer. The device continuously monitors for a Start condition and does not respond to any transaction unless one is encountered.

6.3 Stop condition

A Stop condition is identified by a rising edge of SDATA while SCLK is stable at high state. A Stop condition terminates the communication between the slave device and bus master. A read command that is followed by NoAck can be followed by a Stop condition to force the slave device into idle mode. When the slave device is in idle mode, it is ready to receive the next I^2C transaction. A Stop condition at the end of a write command stops the write operation to the registers.

6.4 Acknowledge bit (ACK)

The acknowledge bit is used to indicate a successful byte transfer. The bus transmitter releases the SDATA after sending eight bits of data. During the ninth bit, the receiver pulls the SDATA low to acknowledge the receipt of the eight bits of data. The receiver may leave the SDATA in high state if it would to not acknowledge the receipt of the data.

6.5 Data input

The device samples the data input on SDATA on the rising edge of the SCLK. The SDATA signal must be stable during the rising edge of SCLK and the SDATA signal must change only when SCLK is driven low.

6.6 Slave device address

The slave device address is a 7 or 10-bit address, where the least significant 3-bit are programmable. These 3-bit values will be loaded in once upon reset and after that these 3 pins no longer be needed with the exception during General Call. Up to 8 STMPE1601 devices can be connected on a single I^2C bus.

6.7 Memory addressing

For the bus master to communicate to the slave device, the bus master must initiate a Start condition and followed by the slave device address. Accompanying the slave device address, there is a Read/$\overline{\text{Write}}$ bit (R/$\overline{\text{W}}$). The bit is set to 1 for Read and 0 for Write operation.

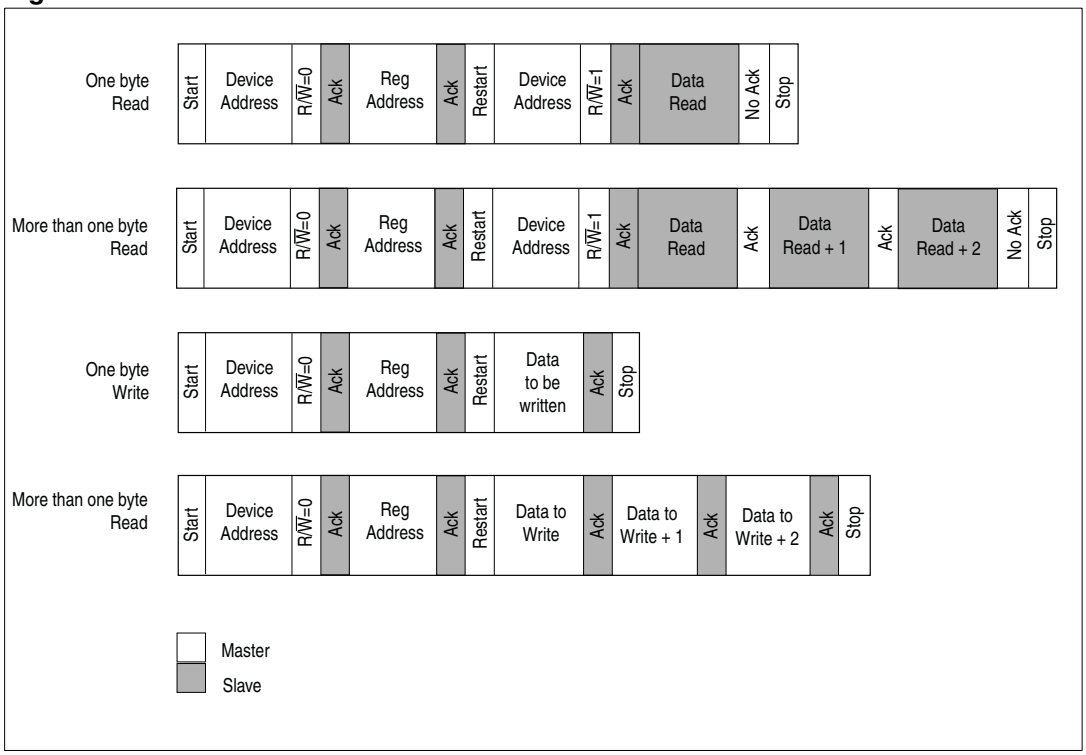
If a match occurs on the slave device address, the corresponding device gives an acknowledgement on the SDA during the 9^{th} bit time. If there is no match, it deselects itself from the bus by not responding to the transaction.

6.8 Operating modes

Table 14. Operating modes

Mode	Bytes	Programming sequence
Read	≥1	START, Device address, R/$\overline{W}$ = 0, Register address to be read
		reSTART, Device address, R/$\overline{W}$ = 1, Data Read, STOP
		If no STOP is issued, the Data Read can be continuously performed. If the register address falls within the range that allows address auto-increment, then register address auto-increments internally after every byte of data being read. For register address that falls within a non-incremental address range, the address will be kept static throughout the entire read operations. Refer to the *Table 11: Register map summary table on page 11* for the address ranges that are auto and non-increment. An example of such a non-increment address is FIFO.
Write	≥1	START, Device address, R/$\overline{W}$ = 0, Register address to be written, Data Write, STOP.
		If no STOP is issued, the Data Write can be continuously performed. If the register address falls within the range that allows address auto-increment, then register address auto-increments internally after every byte of data being written. For those register addresses that fall within a non-incremental address range, the address will be kept static throughout the all write operations. Refer to the memory map table for the address ranges that are auto and non-increment. An example of a non-increment address is Data Port for initializing the PWM commands.

Figure 3. I²C transaction



6.9 General call address

A general call address is a transaction with the slave address of 0x00 and R/$\overline{W}$ = 0. When a general call address is made, the STMPE1601 responds to this transaction with an acknowledgement and behaves as a slave-receiver mode. The meaning of a general call address is defined in the second byte sent by the master-transmitter.

Table 15. General call address

R/$\overline{W}$	Second byte value	Definition
0	0x06	A 2-byte transaction in which the second byte tells the slave device to reset and write (or latch in) the 2-bit programmable part of the slave address.
0	0x04	A 2-byte transaction in which the second byte tells the slave device not to reset and write (or latch in) the 2-bit programmable part of the slave address.
0	0x00	Not allowed as second byte.

Note: All other second byte values will be ignored.

7 System controller

The system controller is the heart of the STMPE1601. It contains the registers for power control and chip identification.

The system registers are:

Table 16. System registers

Address	Register name
0x80	CHIP_ID
0x81	VERSION_ID
0x02	SYS_CTRL
0x03	SYS_CTRL_2

CHIP_ID Chip identification register

7	6	5	4	3	2	1	0
8-bit CHIP_ID							
R	R	R	R	R	R	R	R
0	0	0	0	0	0	1	0

VERSION_ID Version identification register

7	6	5	4	3	2	1	0
8-bit VERSION_ID							
R	R	R	R	R	R	R	R
0	0	0	1	0	0	1	0

SYS_CTRL System control register

7	6	5	4	3	2	1	0
SOFT_RESET	CLOCK SOURCE	DIS_32KHz	SLEEP	EN_GPIO	RESERVED	EN_KPC	EN_SPWM
W	RW	RW	RW	RW	R	RW	RW
0	0	0	0	1	1	1	1

Address: 0x02

Type: R/W

Reset: 0x0F

Description: System control register.

[7] **SOFT_RESET**
Writing a ‘1’ to this bit will do a soft reset of the device. Once the reset is done, this bit will be cleared to ‘0’ by the HW.

[6] **CLOCK_SOURCE**
Set to ‘1’ if external 32 kHz clock were to be used. ‘0’ by default.

[5] **DIS_32 kHz**:
Set this bit to disable the 32 kHz OSC, thus putting the device in hibernate mode.

[4] **SLEEP**:
Writing a ‘1’ to this bit will put the device in sleep mode. On going to sleep mode, this mode is reset internally. When in sleep mode, the internal RC oscillator will output a slower sleep clock which will be used in the device.

[3] **EN_GPIO**:
Writing a ‘0’ to this bit will gate off the clock to the GPIO module, thus stopping its operation

[2] **RESERVED**

[1] **EN_KPC**:
Writing a ‘0’ to this bit will gate off the clock to the keypad controller module, thus stopping its operation

[0] **EN_SPWM**
Writing a ‘0’ to this bit will gate off the clock to the simple PWM controller module, thus stopping its operation

SYS_CTRL_2 System control register 2

7	6	5	4	3	2	1	0
RESERVED			VIO_OFF	AUTOSLEEP_EN	SLEEP_2	SLEEP_1	SLEEP_0
R			R	RW	RW	RW	RW
0			0	0	0	0	0

Address: 0x03

Type: R/W

Reset: 0x00

Description: System control register.

[7] **RESERVED**

[6] **RESERVED**

[5] **RESERVED**

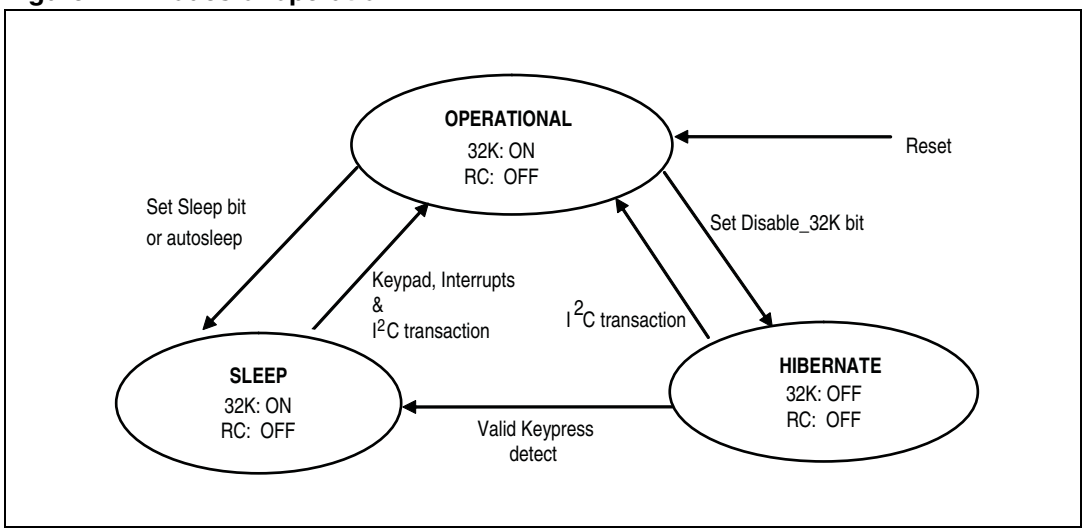
[4] **VIO_OFF**:
Writing a '1' to this bit is mandatory before shutting off the V_{IO} supply while maintaining the V_{CC} supply.
This ensure that the level shifters for GPIOs 15-8 are properly powered down so as not to induce high current and also not to affect the integrity of any external signals that are on the bus where these GPIOs are connected.

[3] **AUTOSLEEP_EN**:
"1" to enable auto-sleep feature. "0" to disable auto-sleep.

[2:0] **SLEEP**:
000 for 4 ms delay
001 for 16 ms delay
010 for 32 ms delay
011: for 64 ms delay
100: for 128 ms delay
101: for 256 ms delay
110: for 512 ms delay
111: for 1024 ms delay

7.1 States of operation

Figure 4. Modes of operation



The device has three main modes of operation:

- **Operational mode**: This is the mode, whereby normal operation of the device takes place. In this mode, the RC clock is available and the main FSM unit routes this clock and the 32 kHz clock to all the device blocks that are enabled. In this mode, individual blocks that need not to be working can be turned off by the master by programming the bits 3 to 0 of the SYS_CTRL register.
- **Sleep mode**: In this low-power mode, the RC oscillator is powered down. All the blocks which need clocks derived from the 32 kHz clock will continue getting a 32 kHz clock. In this mode also, iindividual blocks can be turned off by the master by programming the bits 3 to 0 of the SYS_CTRL register. However, the master needs to program the SYS_CTRL register before coming into this mode, as in the sleep mode, the I^2C interface is not active except to detect traffic for wakeup. Any activity on the I^2C port (intended I^2C transaction for the device) or Wakeup pin or Hotkey activity will cause the device to leave this mode and go into the Operational mode. When leaving this mode, the I^2C will need to hold the SCLK till the RC clock is ready.
- **Hibernate mode:** This mode is entered when the system writes a '1' to bit 5 of the SYS_CTRL register. In this mode, the device is completely inactive as there is absolutely no clock. Only a Reset or a wakeup on I^2C will bring back the system to operational mode. A keypress detect will bring the system to Sleep mode, in which the debounce of the key will take place.

Note: The 32 kHz clock mentioned in this section can be (1) an externally fed 32 kHz clock, or (2) an internally generated (from RC OSC) clock. In case the internal clock is used, the clock has a range of 25 to 45 kHz.

7.2 Autosleep

The host system may configure the STMPE1601 to go into sleep mode automatically whenever there is a period of inactivity following a complete I^2C transaction with the STMPE1601. This inactivity means there is no intended I^2C transaction for the device. For example, if there is an I^2C transaction sent by the host to other slave devices, the STMPE1601 device will still be counting down for the auto-sleep. The STMPE1601 device resets the autosleep time-out counter only when it receives an I^2C transaction meant for the device itself. This autosleep feature is controlled by the SYS_CTRL_2 (system control register 2).

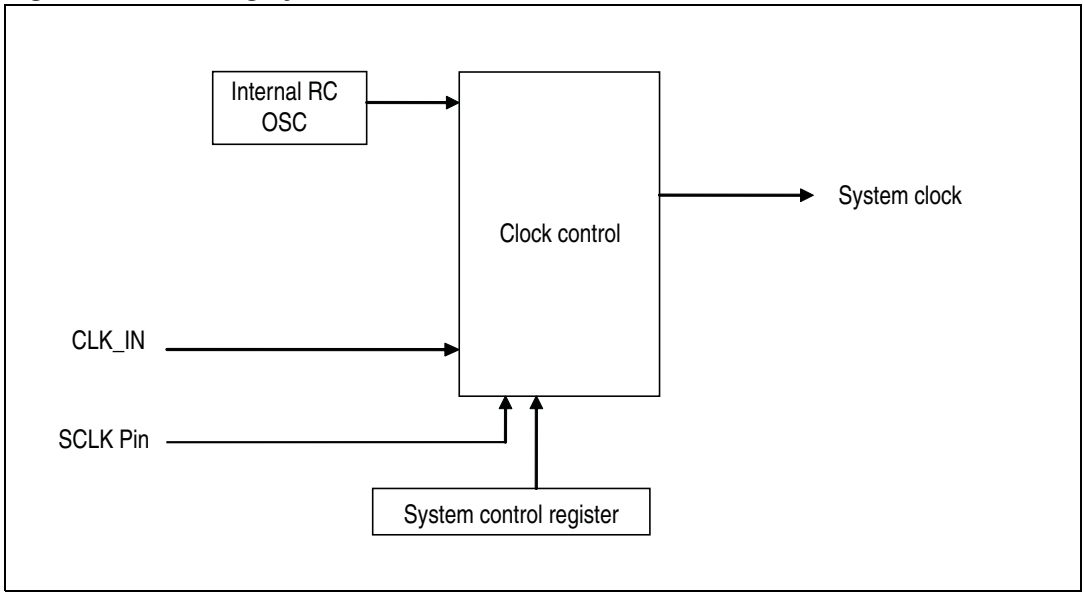
All those events that trigger an interrupt (KPC, hot-key) would result in a transition from Sleep state to Operational state automatically. The wakeup can also be performed through the I^2C transaction intended for the device.

7.3 Keypress detect in the hibernate mode

When in Hibernate mode, a keypress detect causes the system to go into sleep mode. The sleep clock (32 kHz) is then used to debounce the key to detect a valid key. If the keypress is detected to be valid, the system stays in sleep mode. If the key is detected to be invalid, the system goes back into Hibernate mode.

8 Clocking system

Figure 5. Clocking system



The decision on clocks is based on the bits written into the SYS_CTRL registers. Bits 0 to 3 of the SYS_CTRL register allow to control the gating of clocks to the keypad controller, PWM and GPIO in the operational mode.

8.1 Clock source

By default, when the STMPE1601 powers up, it derives a 32 kHz clock from the internal RC oscillator for its operation. If an external clock source is available, it must be configured to accept an external clock through the SYS_CTRL register.

There are 4 sources of reset:

- Reset_N pin
- Low voltage detect (LVD) reset
- Soft reset bit of the SYS_CTRL register
- I^2C reset from the I^2C block.

8.2 Power mode programming sequence

To put the device in sleep mode, the following needs to be done by the host:

– Write a '1' to bit 4 of the SYS_CTRL register.

To wake up the device, the host is required to:

– Assert a wakeup routine on the I^2C bus by sending the Start bit, followed by the device address and the Write bit. Subsequently, proceed with sending the Base Register address and continue with a normal I^2C transaction. The device wakes up upon receiving the correct device address and in Write direction. In other words, the procedure of waking up the device is performed by just sending an I^2C transaction to the device. This procedure can be extended to wake up the device that is in hibernate mode.

To do a soft reset to the device, the host needs to do the following:

– Write a '1' to bit 7 of the SYS_CTRL register. This bit is automatically cleared upon reset.

To go into Hibernate mode, the following needs to be done by the host:

– Set the Disable_32K bit to '1'

To come out of the Hibernate mode, the following needs to be done by the host:

– Assert a system reset

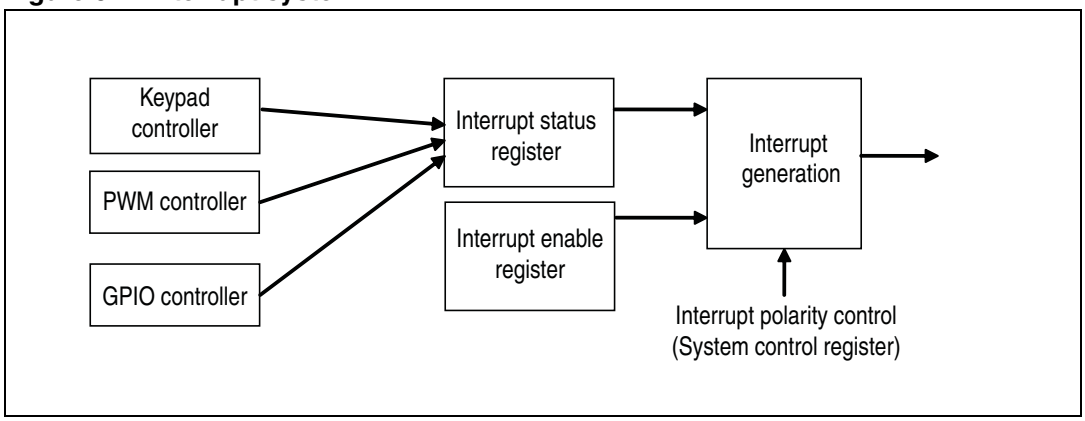
– or put a wakeup on the I^2C

9 Interrupt system

The STMPE1601 uses a highly flexible interrupt system. It allows the host system to configure the type of system events that should result in an interrupt, and pinpoints the source of interrupt by status register. The INT pin can be configured as ACTIVE HIGH, or ACTIVE LOW.

Once asserted, the INT pin would de-assert only if the corresponding bit in the interrupt status register is cleared.

Figure 6. Interrupt system



9.1 Interrupt system register map

Table 17. Register map

Address	Register name	Description	Auto-increment (during sequential R/W)
0x10	INT_CTRL_MSB	Interrupt control register	Yes
0x11	INT_CTRL_LSB		Yes
0x12	INT_EN_MASK_MSB	Interrupt enable mask register	Yes
0x13	INT_EN_MASK_LSB		Yes
0x14	INT_STA_MSB	Interrupt status register	Yes
0x15	INT_STA_LSB		Yes
0x16	INT_EN_GPIO_MASK_MSB	Interrupt enable GPIO mask register	Yes
0x17	INT_EN_GPIO_MASK_LSB		Yes
0x18	INT_STA_GPIO_MSB	Interrupt status GPIO register	Yes
0x19	INT_STA_GPIO_LSB		Yes

9.1.1 Interrupt latency

When the generation of interrupts by the GPIO as input is enabled, the latency (time taken from actual transition at GPIO to time of INT pin assertion) is shown in the following table:

Table 18. Interrupt latency

State of operation	Interrupt latency
Hibernation	10 µs max
Sleep	5 µs max
Active	2 µs max

INT_CTRL Interrupt control register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INT_CTRL_msb								INT_CTRL_lsb							
Reserved													IC2	IC1	IC0
R	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW	RW
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Address: 0x10, 0x11

Type: R, R/W

Reset: 0x00

Description: The interrupt control register is used to configure the interrupt controller. It has a global enable interrupt mask bit that controls the interruption to the host.

[15:3] RESERVED

[2] **IC2:** Output Interrupt polarity
'0' = Active low/falling edge
'1' = Active high/rising edge

[1] **IC1**: Output Interrupt Type
'0' = Level interrupt
'1' = Edge interrupt

[0] **IC0**: Global Interrupt Mask bit
When this bit is written a '1', it will allow interruption to the host. If it is written with a '0', then, it disables all interruption to the host. Writing to this bit does not affect the INT_EN_MASK value.