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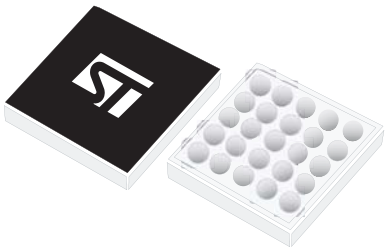
STMPE1801

Xpander Logic™
18-bit enhanced port expander with keypad controller

Features

- 18 GPIOs configurable as GPI, GPO, keypad matrix, special key or dedicated key function
- Operating voltage: 1.65 - 3.6 V
- Hardware keypad controller (KPC) (10 x 8 matrix with 4 optional dedicated keys maximum)
- Keypad controller capable of detecting keypress in hibernation mode
- Interrupt output (open drain) pin
- Advanced power management system
- Ultra-low standby mode current
- Programmable pull-up resistors for all GPIO pins
- ESD performance on GPIO pins:
  - ± 8 kV human body model (JESD22 A114-C)
- ESD performance on V_{CC}, GND, INT_B, R_{STB}, SCL, SDA pins:
  - ± 3 kV human body model (JESD22 A114-C)



Flip-chip CSP 25 (2.03 x 2.03 mm)

Description

The STMPE1801 is a GPIO (general purpose input/output) port expander capable of interfacing a main digital ASIC via the two-line bidirectional bus (I^2C). A separate GPIO expander IC is often used in mobile multimedia platforms to resolve the problem of the limited number of GPIOs typically available on digital engines.
The STMPE1801 offers high flexibility, as each I/O can be configured as input, output, special key, keypad matrix or dedicated key function. This device is designed to include very low quiescent current, and a wakeup feature for each I/O, to optimize the power consumption of the device.
Potential applications for the STMPE1801 include portable media players, game consoles, mobile and smart phones.

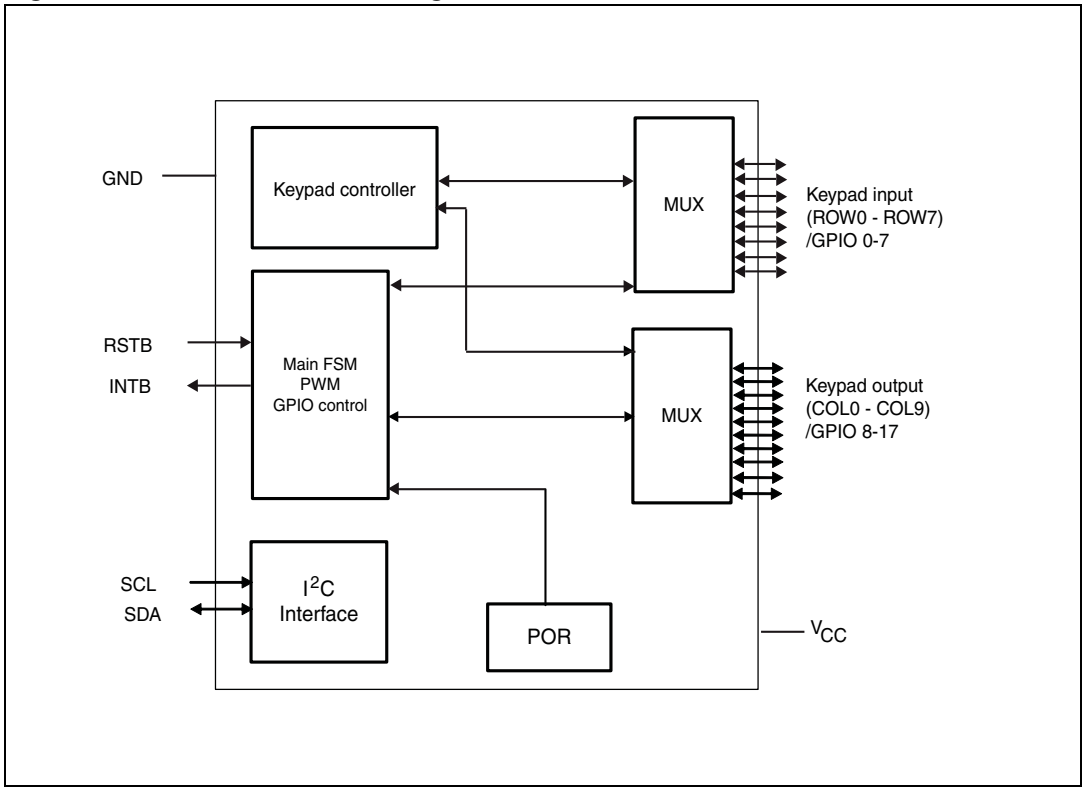
Table 1. Device summary

Order code	Package	Packaging
STMPE1801BJR	Flip-chip CSP 25 (2.03 x 2.03 mm) 0.4 mm pitch	Tape and reel

Contents

1 Block diagram

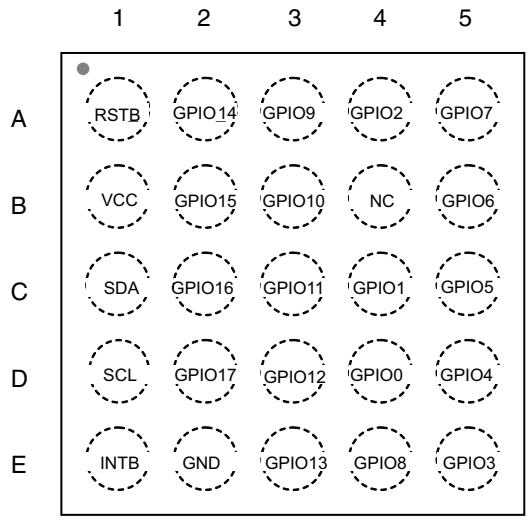
Figure 1. STMPE1801 block diagram



2 Pin settings

2.1 Pin connection

Figure 2. Pin connection (top-through view)



Flip-chip CSP 25

AM04174V1

2.2 Pin description

Table 2. Pin description

Pin number	Type	Symbol	Name and function
D4	I/O	GPIO0	GPIO0/ROW0
C4	I/O	GPIO1	GPIO1/ROW1
A4	I/O	GPIO2	GPIO2/ROW2
E5	I/O	GPIO3	GPIO3/ROW3
D5	I/O	GPIO4	GPIO4/ROW4
C5	I/O	GPIO5	GPIO5/ROW5
B5	I/O	GPIO6	GPIO6/ROW6
A5	I/O	GPIO7	GPIO7/ROW7
E4	I/O	GPIO8	GPIO8/COL0
A3	I/O	GPIO9	GPIO9/COL1
B3	I/O	GPIO10	GPIO10/COL2

Table 2. Pin description (continued)

Pin number	Type	Symbol	Name and function
C3	I/O	GPIO11	GPIO11/COL3
D3	I/O	GPIO12	GPIO12/COL4
E3	I/O	GPIO13	GPIO13/COL5
A2	I/O	GPIO14	GPIO14/COL6
B2	I/O	GPIO15	GPIO15/COL7
C2	I/O	GPIO16	GPIO16/COL8
D2	I/O	GPIO17	GPIO17/COL9
E1	O	INTB	Open drain interrupt output pin. Programmable active low (a pull-up resistor is required) or active high (a pull-down resistor is required). Fail safe. Pull to V_{CC} if not in use.
A1	I	RSTB	External reset input. Active low. Fail safe. Reset pulse width must be more than 500 µs to be valid.
C1	A	SDA	I^2C data. Fail safe
D1	A	SCL	I^2C clock. Fail safe
B4	-	NC	No connect
B1	-	V_{CC}	Power supply
E2	-	GND	Ground

2.3 GPIO pin functions

Table 3. GPIO pin function

Name	Primary function	Alternate function
GPIO0	GPIO	Keypad row 0
GPIO1	GPIO	Keypad row 1
GPIO2	GPIO	Keypad row 2
GPIO3	GPIO	Keypad row 3
GPIO4	GPIO	Keypad row 4
GPIO5	GPIO	Keypad row 5
GPIO6	GPIO	Keypad row 6
GPIO7	GPIO	Keypad row 7
GPIO8	GPIO	Keypad column 0
GPIO9	GPIO	Keypad column 1
GPIO10	GPIO	Keypad column 2
GPIO11	GPIO	Keypad column 3
GPIO12	GPIO	Keypad column 4

Table 3. GPIO pin function

Name	Primary function	Alternate function
GPIO13	GPIO	Keypad column 5
GPIO14	GPIO	Keypad column 6
GPIO15	GPIO	Keypad column 7
GPIO16	GPIO	Keypad column 8
GPIO17	GPIO	Keypad column 9

The default function is always GPIO. As soon as the key scanning is enabled through the keypad registers, the function is then switched to the key function and then any configuration made in the GPIO registers is ignored.

3 Maximum ratings

Stressing the device above the rating listed in the “absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3.1 Absolute maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	4.5	V
V_{IN}	Input voltage on GPIO pin	4.5	V
V_{ESD}	Minimum ESD protection on each GPIO pin (HBM model - JESD22 A114-C)	±8	kV
V_{ESD}	ESD protection on other pins (HBM model - JESD22 A114-C)	±3	kV

3.2 Thermal data

Table 5. Thermal data

Symbol	Parameter	Min	Typ	Max	Unit
R_{thJA}	Thermal resistance junction-ambient	–	100	–	°C/W
T_A	Operating ambient temperature	-40	25	85	°C
T_J	Operating junction temperature	-40	25	125	°C

4 Electrical specification

4.1 DC electrical characteristics

Table 6. DC electrical characteristics

Symbol	Parameter	Test conditions		Value			Unit
				Min	Typ	Max	
V_{CC}	Supply voltage	-		1.65	–	3.6	V
I_{CC}	Active current (core and analog) - 1 key press	1.8 V		–	28	55	µA
		3.3 V		–	90	140	µA
$I_{HIBERNATE}$	Hibernate current	1.8 V	25 °C	–	–	0.5	µA
			85 °C	–	–	1	
		3.3 V	25 °C	–	–	0.5	µA
			85 °C	–	–	1	
I_{NTB}	Open drain output current	$V_{OL(max)}$=0.45 V at V_{CC}=1.8 V $V_{OL(max)}$=0.83 V at V_{CC}=3.3 V		–	4	–	mA

4.2 Input/Output DC electrical characteristics

Table 7. I/O DC electrical characteristics

Symbol	Parameter	Test conditions	Value			Unit
			Min	Typ	Max	
V_{IL}	Low level input voltage	V_{CC} = 1.8 V	–	–	0.2 V_{CC}	V
		V_{CC} = 3.3 V	–	–	0.2 V_{CC}	
V_{IH}	High level input voltage	V_{CC} = 1.8 V	0.8 V_{CC}	–	–	V
		V_{CC} = 3.3 V	0.8 V_{CC}	–	–	
V_{HYST}	Schmitt trigger hysteresis	V_{CC} = 1.8 V	–	0.10	–	V
		V_{CC} = 3.3 V	–	0.20	–	
V_{OL}	Low level output voltage	I_{OL} = 4 mA, V_{CC} = 1.8 V	–	–	0.45	V
		I_{OL} = 4 mA, V_{CC} = 3.3 V	–	–	0.45	
V_{OH}	High level output voltage	I_{OH} = -4 mA, V_{CC} = 1.8 V	1.35	–	–	V
		I_{OH} = -4 mA, V_{CC} = 3.3 V	2.48	–	–	
R_{UP}	Equivalent pull-up resistance	V_{CC} = 3.3 V. Active implementation, R value is determined by the current measured at 0 V	30	60	90	kΩ
		V_{CC} = 1.8 V. Active implementation, R value is determined by the current measured at 0 V	50	100	150	

5 Register address

Table 8. STMPE1801 register summary table

Address	Register name	Description	Auto-increment	7	6	5	4	3	2	1	0
00	CHIP_ID	Chip identification	No	8-bit CHIP ID							
01	VERSION_ID	Version identification	No	8-bit VERSION ID							
02	SYS_CTRL	System control	No	SF_RST	RESERVED				GPI_DB1	GPI_DB0	RSVD
04	INT_CTRL_LOW	Interrupt control	Yes	RESERVED					IC2	IC1	IC0
05	INT_CTRL_HIGH			RESERVED							
06	INT_EN_MASK_LOW	Interrupt enable mask	Yes	RESERVED			IE4	IE3	IE2	IE1	IE0
07	INT_EN_MASK_HIGH			RESERVED							
08	INT_STA_LOW	Interrupt status	Yes	RESERVED			IE4	IE3	IE2	IE1	IE0
09	INT_STA_HIGH			RESERVED							
0A	INT_EN_GPIO_MASK_LOW	Interrupt enable GPIO mask	Yes	IEG7	IEG6	IEG5	IEG4	IEG3	IEG2	IEG1	IEG0
0B	INT_EN_GPIO_MASK_MID			IEG15	IEG14	IEG13	IEG12	IEG11	IEG10	IEG9	IEG8
0C	INT_EN_GPIO_MASK_HIGH			RESERVED						IEG17	IEG16
0D	INT_STA_GPIO_LOW	Interrupt status GPIO	Yes	ISG7	ISG6	ISG5	ISG4	ISG3	ISG2	ISG1	ISG0
0E	INT_STA_GPIO_MID			ISG15	ISG14	ISG13	ISG12	ISG11	ISG10	ISG9	ISG8
0F	INT_STA_GPIO_HIGH			RESERVED						ISG17	ISG16
10	GPIO_SET_LOW	GPIO set pin state	Yes	IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0
11	GPIO_SET_MID			IO15	IO14	IO13	IO12	IO11	IO10	IO9	IO8
12	GPIO_SET_HIGH			RESERVED						IO17	IO16
13	GPIO_CLR_LOW	GPIO clear pin state	Yes	IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0
14	GPIO_CLR_MID			IO15	IO14	IO13	IO12	IO11	IO10	IO9	IO8
15	GPIO_CLR_HIGH			RESERVED						IO17	IO16
16	GPIO_MP_LOW	GPIO monitor pin state	Yes	IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0
17	GPIO_MP_MID			IO15	IO14	IO13	IO12	IO11	IO10	IO9	IO8
18	GPIO_MP_HIGH			RESERVED						IO17	IO16

Table 8. STMPE1801 register summary table

Address	Register name	Description	Auto-increment	7	6	5	4	3	2	1	0
19	GPIO_SET_DIR_LOW	GPIO set pin direction register	Yes	IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0
1A	GPIO_SET_DIR_MID			IO15	IO14	IO13	IO12	IO11	IO10	IO9	IO8
1B	GPIO_SET_DIR_HIGH			RESERVED						IO17	IO16
1C	GPIO_RE_LOW	GPIO rising edge	Yes	IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0
1D	GPIO_RE_MID			IO15	IO14	IO13	IO12	IO11	IO10	IO9	IO8
1E	GPIO_RE_HIGH			RESERVED						IO17	IO16
1F	GPIO_FE_LOW	GPIO falling edge	Yes	IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0
20	GPIO_FE_MID			IO15	IO14	IO13	IO12	IO11	IO10	IO9	IO8
21	GPIO_FE_HIGH			RESERVED						IO17	IO16
22	GPIO_PULL_UP_LOW	GPIO pull up	Yes	IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0
23	GPIO_PULL_UP_MID			IO15	IO14	IO13	IO12	IO11	IO10	IO9	IO8
24	GPIO_PULL_UP_HIGH			RESERVED						IO17	IO16
30	KPC_ROW	Keypad row scanning	Yes	ROW7	ROW6	ROW5	ROW4	ROW3	ROW2	ROW1	ROW0
31	KPC_COL_LOW	Keypad column scanning	Yes	COL7	COL6	COL5	COL4	COL3	COL2	COL1	COL0
32	KPC_COL_HIGH			RESERVED						COL9	COL8
33	KPC_CTRL_LOW	Key config: Scan count and dedicated key	Yes	SCAN_COUNT 0-3				DKEY 0-3			
34	KPC_CTRL_MID			DB6	DB5	DB4	DB3	DB2	DB1	DB0	Rsvd
35	KPC_CTRL_HIGH			Rsvd	CMB_KEY	RESERVED				SCAN_FREQ	
36	KPC_CMD	Keypad command	Yes	RESERVED						KPC_LCK	SCAN
37	KPC_COMB_KEY_0	Keypad combination key mask	Yes	C4	C3	C2	C1	C0	R2	R1	R0
38	KPC_COMB_KEY_1			C4	C3	C2	C1	C0	R2	R1	R0
39	KPC_COMB_KEY_2			C4	C3	C2	C1	C0	R2	R1	R0

Table 8. STMPE1801 register summary table

Address	Register name	Description	Auto-increment	7	6	5	4	3	2	1	0
3A	KPC_DATA_BYTE0	Keypad data	Yes	UP/DWN	C3	C2	C1	C0	R2	R1	R0
3B	KPC_DATA_BYTE1			UP/DWN	C3	C2	C1	C0	R2	R1	R0
3C	KPC_DATA_BYTE2			UP/DWN	C3	C2	C1	C0	R2	R1	R0
3D	KPC_DATA_BYTE3			SF7	SF6	SF5	SF4	SF3	SF2	SF1	SF0
3E	KPC_DATA_BYTE4			RESERVED				Dedicated Key 0 - 3			

6 I²C specification

The features supported by the I²C interface are listed below:

- I²C slave device
- Operates at V_{CC} (1.8 - 3.6 V)
- Compliant to Philips I²C specification version 2.1
- Supports standard (up to 100 kbps) and fast (up to 400 kbps) modes
- 7-bit device addressing modes
- General call
- Start/Restart/Stop

6.1 I²C related pins

- SCL
- SDA

The device supports both 1.8 V I²C and 3.3 V I²C operations. It is recommended that Vpullup at SCL and SDA externally is greater or equal to V_{CC}.

6.2 I²C addressing

The STMPE1801 7-bit addressing is set to 40h.

6.3 Start condition

A Start condition is identified by a falling edge of SDA while SCL is stable at high state. A Start condition must precede any data/command transfer. The device continuously monitors for a Start condition and does not respond to any transaction unless one is encountered.

The first byte is scanned after the START command is detected to check for device ID. Ensure that all state machines are flushed when START instruction is issued.

6.4 Stop condition

A Stop condition is identified by a rising edge of SDA while SCL is stable at high state. A Stop condition terminates the communication between the slave device and bus master. A read command that is followed by NoAck can be followed by a Stop condition to force the slave device into idle mode. When the slave device is in idle mode, it is ready to receive the next I²C transaction. A Stop condition at the end of a write command stops the write operation to the registers.

Once the Stop condition is detected, the device should release the bus and go to Hibernate mode if there is no more activity.

An I²C transaction with a START bit followed immediately by a STOP condition should not cause any I²C lock-up.

6.5 Acknowledge bit (ACK)

The acknowledge bit is used to indicate a successful byte transfer. The bus transmitter releases the SDA after sending eight bits of data. During the ninth bit, the receiver pulls the SDA low to acknowledge the receipt of the eight bits of data. The receiver may leave the SDA in high state if it does not acknowledge the receipt of the data.

6.6 Data input

The device samples the data input on SDA on the rising edge of the SCL. The SDA signal must be stable during the rising edge of SCL and the SDA signal must change only when SCL is driven low.

6.7 Memory addressing

For the bus master to communicate to the slave device, the bus master must initiate a Start condition and be followed by the slave device address. Accompanying the slave device address, there is a Read/Write bit (R/$\overline{W}$). The bit is set to 1 for Read and 0 for Write operation.

If a match occurs on the slave device address, the corresponding device gives an acknowledgement on the SDA during the 9th bit time. If there is no match, it deselects itself from the bus by not responding to the transaction.

6.8 Operation modes

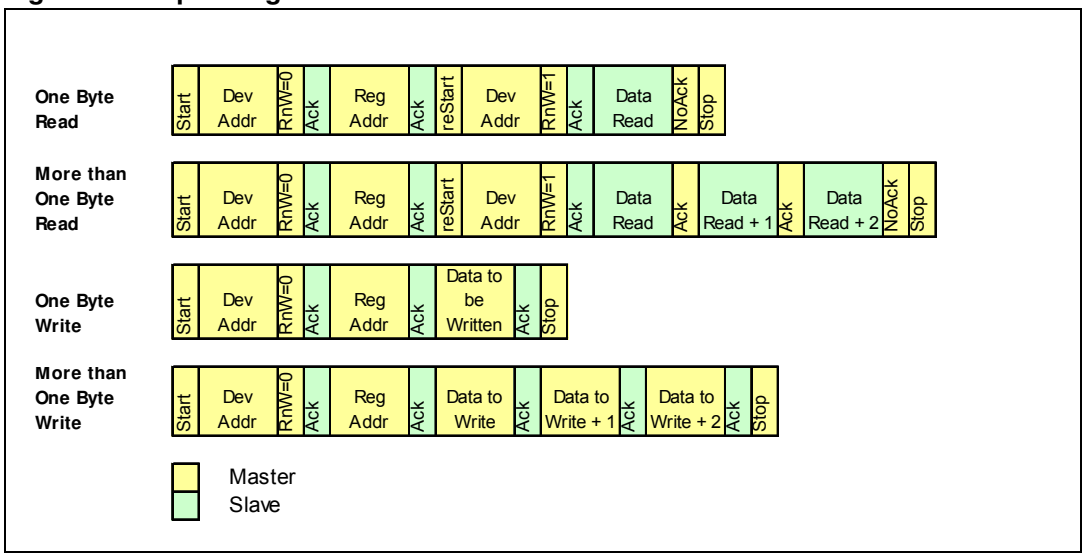
Table 9. Operating modes

Mode	Byte	Programming sequence
Read	≥1	START, Device address, R/$\overline{W}$ =0, Register Address to be read
		RESTART, Device Address, R/$\overline{W}$ =1, Data Read, STOP
		If no STOP is issued, the Data Read can be continuously performed. If the register address falls within the range that allows address auto-increment, then register address auto-increments internally after every byte of data being read. For register address that fails within a non-incremental address range, the address is kept static throughout the entire read operation. Refer to *Table 8.: STMPE1801 register summary table* for the address ranges that are auto-increment and non-increment. An example of such a non-increment address is FIFO.

Table 9. Operating modes

Mode	Byte	Programming sequence
Write	≥1	START, Device Address, R/$\overline{W}$ =0, Register Address to be written, Data Write, STOP
		If no STOP is issued, the Data Write can be continuously performed. If the register address falls within the range that allows address auto-increment, then register address auto-increment internally after every byte of data being written. For those register addresses that fall within a non-incremental address range, the address will be kept static throughout the entire write operation. Refer to *Table 8.: STMPE1801 register summary table* for the address ranges that are auto-increment and non-increment. An example of a non-increment address is Data Port for initializing the PWM.

Figure 3. Operating modes



6.9 General call address

A general call address is a transaction with the slave address of 0x00 and R/$\overline{W}$ =0. When a general call address is asserted, the STMPE1801 responds to this transaction with an acknowledgement and behaves as a slave-receiver mode. The meaning of a general call address is defined in the second byte sent by the master-transmitter.

Table 10. General call address

R/$\overline{W}$	Second byte value	Definition
0	0x06	A 2-byte transaction in which the second byte tells the slave device to reset and write (or latch in) the 2-bit programmable part of the slave address.
0	0x00	Not allowed as second byte.

Note: All other second byte values are ignored.

7 System controller

7.1 System level registers

The system controller is the heart of the STMPE1801. It contains the registers for power control and chip identification.

The system registers are:

Address	Register name
00	CHIP_ID
01	VERSION_ID
02	SYS_CTRL

CHIP_ID — Chip identification register

7	6	5	4	3	2	1	0
8-bit CHIP_ID							
R	R	R	R	R	R	R	R
1	1	0	0	0	0	0	1

VERSION_ID — Version identification register

7	6	5	4	3	2	1	0
8-bit VERSION_ID							
R	R	R	R	R	R	R	R
0	0	0	1	0	0	0	0

SYS_CTRL System control register

7	6	5	4	3	2	1	0
SF_RST	RESERVED				GPI_DB1	GPI_DB0	RSVD
W	R	R	R	R	RW	RW	R
0	0	0	0	0	1	1	0

Address: 02

Type: R/W

Reset: 0x06

Description: System control register.

[7] SF_RST: Soft Reset
Writing a ‘1’ to this bit will do a soft reset of the device. Once the reset is done, this bit is cleared to ‘0’ by the HW.

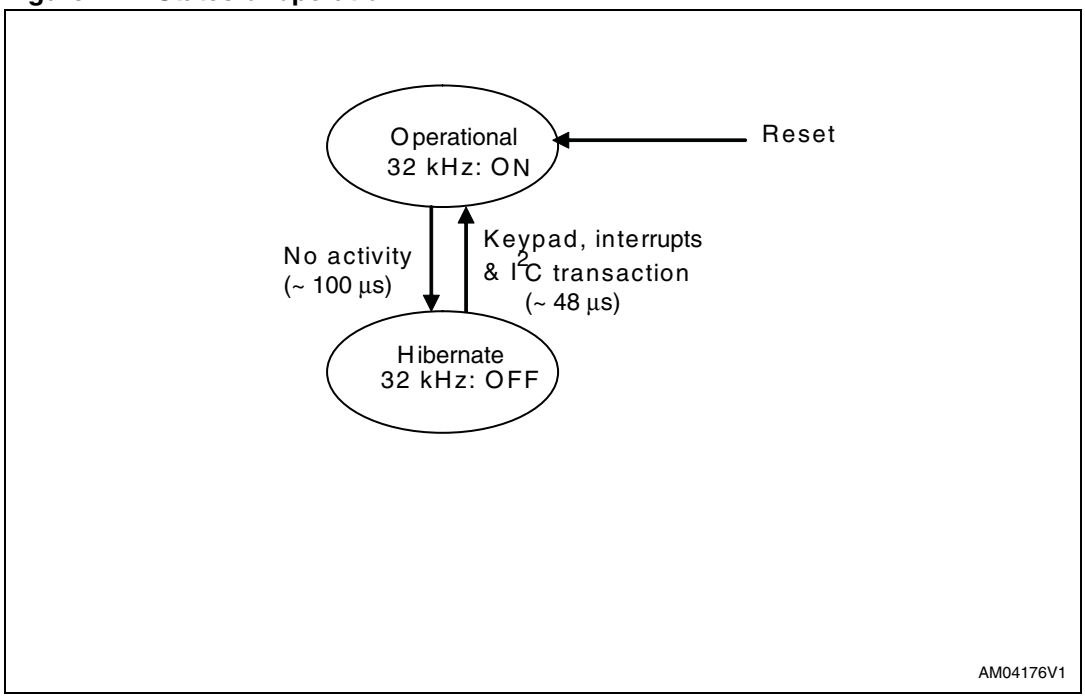
[6:3] RESERVED

[2:1] GPI_DB [1:0]
GPI [17:0] operational mode de-bounce time
‘00’ = 30 µs
‘01’ = 90 µs
‘10’ = 150 µs
‘11’ = 210 µs (default)

[0] RESERVED

7.2 States of operation

Figure 4. States of operation



The device has two main modes of operation:

- Operational mode: This is the mode, whereby normal operation of the device takes place. In this mode, the main finite state machine (FSM) unit routes 32 kHz clock to all the device blocks.
- Hibernate mode: This mode is entered automatically in auto-hibernate mode. When the device is in Hibernate mode, the 32 kHz clock is disabled. If there is a keypad activity, interrupt event, hotkey activity or I^2C transaction, the device switches to operational mode. A reset event brings back the system to operational mode.

7.2.1 Auto-hibernate

The STMPE1801 is set to go into Hibernate mode automatically if there is a period of inactivity (~ 100 µs) following the completion of I^2C transaction with the host. The STMPE1801 will continue counting down for hibernation mode activation even if there is an I^2C transaction sent by the host to other slave devices. Any I^2C transaction from the host to the STMPE1801 resets the hibernate counter.

Auto-hibernate mode occurs only when all the keys are released and FIFO is emptied through reading. This is to prevent any loss of data.

The hibernate mode counter should start when any of the following conditions is detected:

- Once the I^2C transaction is completed or a STOP condition is detected.
- If the device ID in the I^2C transaction is invalid.

When there is a keypad activity, the device should go into Hibernate mode ONLY when all the previously pressed keys are released.

Any keypad activity, interrupt event, hotkey activity or VALID I^2C transaction wakes up the device from Hibernate mode and switches to operational mode automatically.

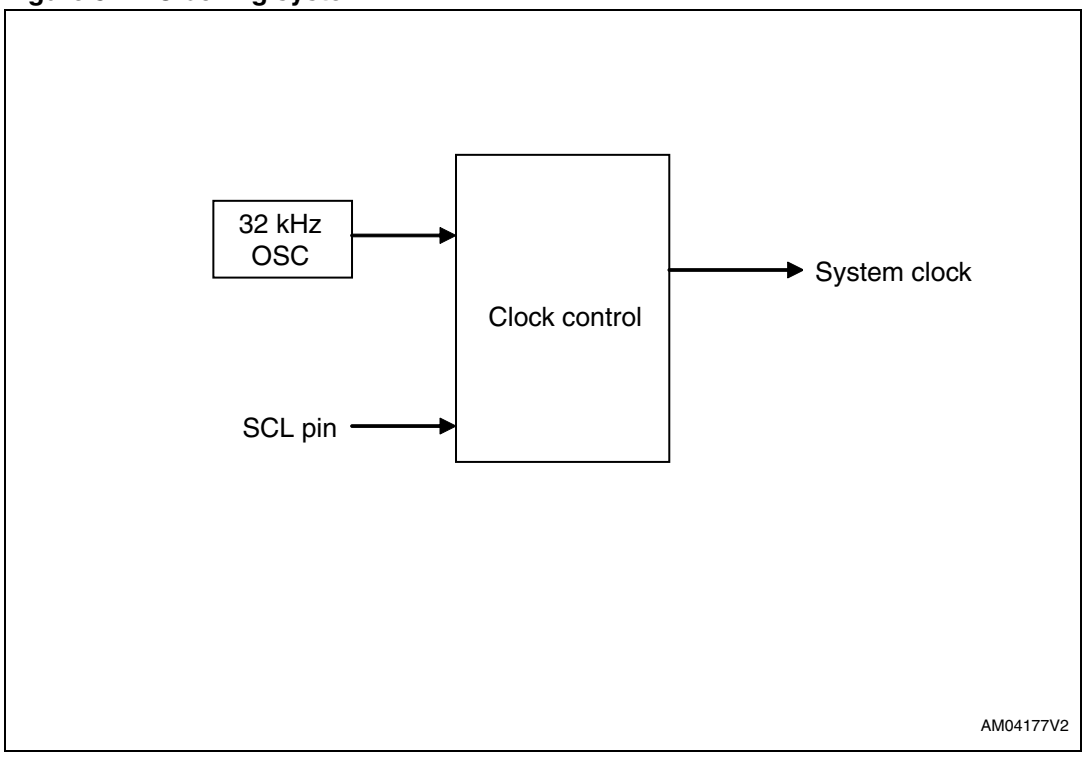
7.2.2 Keypress detect in the Hibernate mode

When in Hibernate mode, any keypress detected causes the system to go into operational mode (~48 µs). The system will then de-bounce the key to detect a valid key. If the keypress detected is valid, the system stays in operation mode. If the key detected is invalid, the system goes back into Hibernate mode.

8 Clocking system

In order to reduce the power consumption, the STMPE1801 turns off the oscillator during Hibernate mode.

Figure 5. Clocking system



8.0.1 Clock source

By default, when the STMPE1801 powers up, it derives a 32 kHz clock from the internal RC oscillator for its operation.

There are 4 sources of reset:

- RSTB pin
- Low voltage detect (LVD) reset
- Soft reset bit of the SYS_CTRL register
- I^2C reset from the I^2C block.

8.0.2 Power mode programming sequence

The device enters auto Hibernate mode when there is inactivity for a fixed period of time.

To wake up the device, the host is required to:

– Send an I^2C transaction to the device.

To do a soft reset to the device, the host needs to do the following:

– Write a '1' to bit 7 of the SYS_CTRL register. This bit is automatically cleared upon reset.

To come out of the Hibernate mode, the following needs to be done by the host:

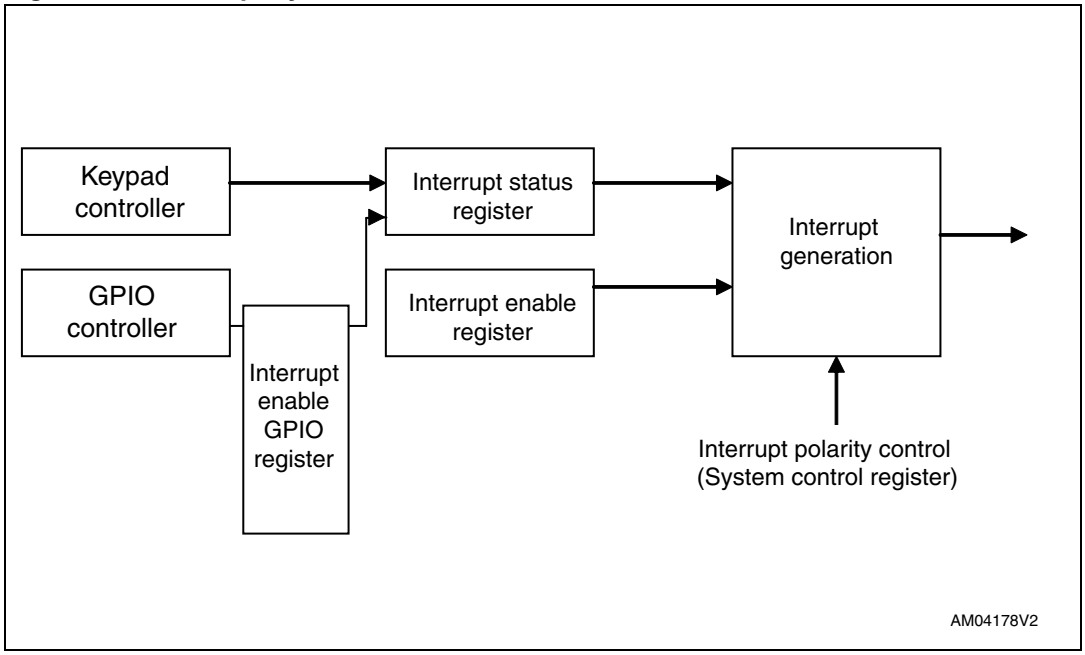
– Assert a system reset
– Or put a wakeup on the I^2C transaction
– Interrupt activity

9 Interrupt system

The STMPE1801 uses a highly flexible interrupt system. It allows the host system to configure the type of system events that should result in an interrupt, and pinpoints the source of interrupt by status registers. The INT pin can be configured as active high (a pull-down resistor is required), or active low (a pull-up resistor is required). If INT pin is not in use, it is necessary to pull INT pin to V_{CC}.

Once asserted, the INT pin would de-assert when a read is done to the corresponding bit either in the INT_STA register or INT_STA_GPIO register.

Figure 6. Interrupt system



9.1 Interrupt system register map

Table 11. Interrupt system register map

Address	Register name	Description	Auto-increment (during sequential R/W)
04	INT_CTRL_LOW	Interrupt control register	Yes
05	INT_CTRL_HIGH		Yes
06	INT_EN_MASK_LOW	Interrupt enable mask register	Yes
07	INT_EN_MASK_HIGH		Yes
08	INT_STA_LOW	Interrupt status register	Yes
09	INT_STA_HIGH		Yes
0A	INT_EN_GPIO_MASK_LOW	Interrupt enable GPIO mask register	Yes
0B	INT_EN_GPIO_MASK_MID		Yes
0C	INT_EN_GPIO_MASK_HIGH		Yes
0D	INT_STA_GPIO_LOW	Interrupt status GPIO register	Yes
0E	INT_STA_GPIO_MID		Yes
0F	INT_STA_GPIO_HIGH		Yes

9.2 Interrupt latency for the GPIO hot keys

When the generation of interrupts by the GPIO as input is enabled for the hot keys, the latency (time taken from actual transition at GPIO to time of INT pin assertion) is shown in the following table:

Table 12. GPIO hot keys interrupt latency

State of operation	Interrupt latency	Comments
Hibernation	>200 µs (default)	Latency can be programmed by the GPI_DB bits of SYS_CTRL register
Active	>200 µs (default)	