Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

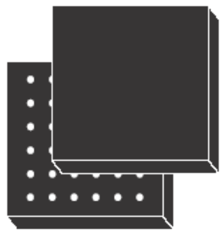
Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

STMPE2401

24-bit Enhanced port expander with Keypad and PWM controller
Xpander logic

Features

- 24 GPIOs
- Operating voltage 1.8V
- Hardware key pad controller (8*12 matrix max)
- 3 PWM (8 bit) output for LED brightness control and blinking
- Interrupt output (open drain) pin
- Configurable hotkey feature on each GPIO
- Ultra-low Standby-mode current
- Package TFBGA - 36 pins 3.6x3.6mm, pitch 0.5mm



TFBGA

Description

The STMPE2401 is a GPIO (General Purpose Input / output) port expander able to interface a Main Digital ASIC via the two-line bidirectional bus (I2C); separate GPIO Expander IC is often used in Mobile-Multimedia platforms to solve the problems of the limited amounts of GPIOs usually available on the Digital Engine.

The STMPE2401 offers great flexibility as each I/Os is configurable as input, output or specific functions; it's able to scan a keyboard, also provides PWM outputs for brightness control in backlight, rotator decoder interface and GPIO. This device has been designed very low quiescent current, and is including a wake up feature for each I/O, to optimize the power consumption of the IC.

Potential application of the STMPE2401 includes portable media player, game console, mobile phone, smart phone

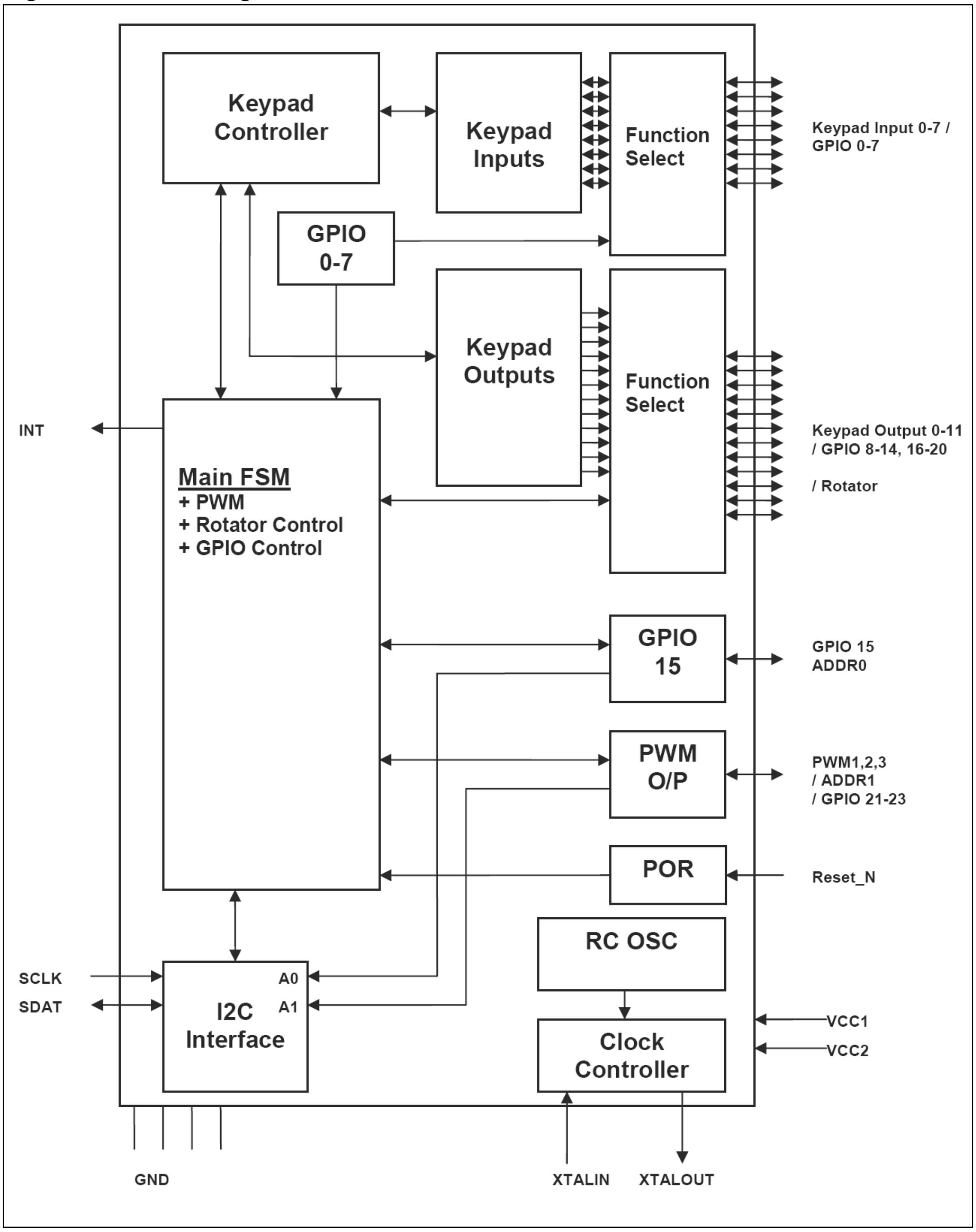
Figure 1. Device summary

Part number	Package	Packaging
STMPE2401TBR	TFBGA36	Tape and reel

Contents

1 Block diagram

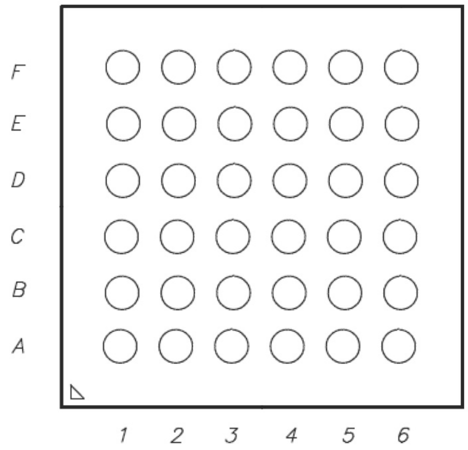
Figure 1. Block diagram



2 Pin settings

2.1 Pin connection

Figure 2. Pin connection



TFBGA

2.2 Pin assignment and TFBGA ball location

Table 1. Pin assignment

Ball	Name	Type	Name and function
C3	GND	-	
C2	KP_X0	IO	GPIO
C1	Reset_N	I	External reset input, active LOW
B1	KP_X1	IO	GPIO
A1	KP_X2	IO	GPIO
B2	KP_X3	IO	GPIO
A2	KP_X4	IO	GPIO
B3	KP_X5	IO	GPIO
A3	KP_X6	IO	GPIO
C4	GND	-	
A4	VCC1	-	1.8V Input

Table 1. Pin assignment

Ball	Name	Type	Name and function
B3	KP_X7	IO	GPIO
A5	KP_Y5	IO	GPIO
A6	KP_Y4	IO	GPIO
B5	KP_Y3	IO	GPIO
B6	KP_Y2	IO	GPIO
C5	KP_Y1	IO	GPIO
C6	KP_Y0	IO	GPIO
D3	GND	-	
D6	ADDR0	IO	GPIO and I2C ADDR 0 (in reset)
D5	KP_Y9	A/IO	GPIO
E6	KP_Y10	A/IO	GPIO
F6	KP_Y11	A/IO	GPIO
E5	PWM3	A/IO	GPIO and I2C ADDR 1 (in reset)
F5	PWM2	A/IO	GPIO
E4	PWM1	A/IO	GPIO
F4	VCC2	-	1.8V Input
D4	GND	-	
F3	INT	O	Open drain interrupt output pin
E3	KP_Y8	IO	GPIO
F2	KP_Y7	IO	GPIO
F1	KP_Y6	IO	GPIO
E2	SDATA	A	I2C DATA
E1	SCLK	A	I2C Clock
D2	XTALIN	A	XTAL Oscillator or External 32KHz input
D1	XTALOUT	A	XTAL Oscillator

2.3 GPIO Pin functions

Table 2. GPIO Pin functions

Pin N°	Name	Primary Function	Alternate Function 1	Alternate Function 2	Alternate Function 3
2	KP_X0	GPIO 0	Keypad input 0		
4	KP_X1	GPIO 1	Keypad input 1		
5	KP_X2	GPIO 2	Keypad input 2		
6	KP_X3	GPIO 3	Keypad input 3		
7	KP_X4	GPIO 4	Keypad input 4		
8	KP_X5	GPIO 5	Keypad input 5		
9	KP_X6	GPIO 6	Keypad input 6		
12	KP_X7	GPIO 7	Keypad input 7		
13	KP_Y5	GPIO 13	Keypad output 5		
14	KP_Y4	GPIO 12	Keypad output 4		
15	KP_Y3	GPIO 11	Keypad output 3		
16	KP_Y2	GPIO 10	Keypad output 2		
17	KP_Y1	GPIO 9	Keypad output 1		
18	KP_Y0	GPIO 8	Keypad output 0		
20	ADDR0	GPIO 15			
21	KP_Y9	GPIO 18	Keypad output 9	Rotator 0	
22	KP_Y10	GPIO 19	Keypad output 10	Rotator 1	
23	KP_Y11	GPIO 20	Keypad output 11	Rotator 2	
24	PWM3	GPIO 23	Channel 3		
25	PWM2	GPIO 22	Channel 2		
26	PWM1	GPIO 21	Channel 1		
30	KP_Y8	GPIO 17	Keypad output 8		ClkOut
31	KP_Y7	GPIO 16	Keypad output 7		
32	KP_Y6	GPIO 14	Keypad output 6		

2.4 Pin mapping to TFBGA (bottom view, balls up)

Table 3. Pin mapping to TFBGA

	A	B	C	D	E	F
1	KP-X2	KP-X1	Reset_N	XTALOUT	SCLK	KP-Y6
2	KP-X4	KP-X3	KP-X0	XTALIN	SDATA	KP-Y7
3	KP-X6	KP-X5	GND	GND	KP-Y8	INT
4	VCC	KP-X7	GND	GND	PWM-1	VCC
5	KP-Y5	KP-Y3	KP-Y1	KP-Y9	PWM-3	PWM-2
6	KP-Y4	KP-Y2	KP-Y0	ADDR0	KP-Y10	KP-Y11

3 Maximum rating

Stressing the device above the rating listed in the “Absolute Maximum Ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

3.1 Absolute maximum rating

Table 4. Absolute maximum rating

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	2.5	V
V_{IN}	Input voltage on GPIO pin	2.5	V
V_{I2C}	Input voltage on I2C pin (SDATA,SCLK, INT)	4.5	V
VESD (HBM)	ESD protection on each GPIO pin	2	KV

3.2 Thermal data

Table 5. Thermal data

Symbol	Parameter	Min	Typ	Max	Unit
R_{thJA}	Thermal resistance junction-ambient		100		°C/W
T_A	Operating ambient temperature	-40	25	85	°C
T_J	Operating junction temperature	-40	25	125	°C

4 Electrical specification

4.1 DC electrical characteristics

Table 6. DC electrical characteristics

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ.	Max.	
VCC1,2	1.8V supply voltage		1.65	1.8	1.95	V
$I_{HIBERNATE}$	HIBERNATE mode current			6	12	uA
I_{SLEEP}	SLEEP mode current			15	50	uA
Icc	Operating current (FSM working – No peripheral activity)			0.5	1.0	mA
I_O_INT	Open drain output current			4		mA
V_INT	Voltage level at INT pin			3.6		V

4.2 I/O DC electrical characteristics

The 1.8V I/O complies to the EIA/JEDEC standard JESD8-7.

Table 7. I/O DC electrical characteristic

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
Vil	Low level input voltage			0.35*Vcc = 0.63	V
Vih	High level input voltage	0.65*Vcc = 1.17			V
Vhyst	Schmitt trigger hysteresis		0.10		V

4.3 DC input specification

($1.55V < V_{DD} < 1.95V$)

Table 8. DC input specification

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ.	Max.	
Vol	Low level output voltage	Iol = 4mA			0.45	V
Voh	High level output voltage	Ioh = 4mA	Vcc - 0.45 = 1.35			V

4.4 DC output specification

(1.55V < vdd < 1.95V)

Table 9. DC output specification

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ.	Max.	
Ipu	Pull-up current	Vi = 0V	15	35	65	µA
Ipd	Pull-down current	Vi = vdd	14	35	60	µA
Rup	Equivalent pull-up resistance	Vi = 0V	30	50	103.3	KΩ
Rpd	Equivalent pull-down resistance	Vi = vdd	32.5	50	110.7	KΩ

Note: Pull-up and Pull-down characteristics

4.5 AC characteristics

Table 10. AC characteristics

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
F_O	Frequency	16		32	kHz
C_L	Load capacitance			27	pF

5 Register map

All registers have the size of 8-bit. Some of the registers are composed of 2-byte to form 16-bit registers. For each of the module, their registers are residing within the given address range.

Table 11. Register map

Address	Module registers	Description	Auto-Increment (during read/write)
0x00 – 0x07 0x80 – 0x81	Clock and Power Manager module	Clock and Power Manager register range.	Yes
0x10 – 0x1F	Interrupt Controller module	Interrupt Controller register range	Yes
0x30 – 0x37	PWM Controller Module	PWM Controller register range	Yes
0x38 – 0x3F		PWM Controller register range	No
0x60 – 0x67	Keypad Controller Module	Keypad Controller register range	Yes
0x68 – 0x6F		Keypad Controller register range	No
0x70 – 0x77	Rotator Controller Module	Rotator Controller register range	Yes
0x82 – 0xBF	GPIO Controller Module	GPIO Controller register range	Yes

6 I^{2}C Interface

The features that are supported by the I^{2}C interface are as below:

- I^{2}C Slave device
- SDAT and SCLK operates from 1.8V to 3.3V
- Compliant to Philip I^{2}C specification version 2.1
- Supports Standard (up to 100kbps) and Fast (up to 400kbps) modes.
- 7-bit device addressing mode
- General Call
- Start/Restart/Stop
- Address up to 4 STMPE2401 devices via I^{2}C

The address is selected by the state of two pins. The state of the pins will be read upon reset and then the pins can be configured for normal operation. The pins will have a pull-up or down to set the address. The I2C interface module allows the connected host system to access the registers in the STMPE2401.

6.1 Start condition

A Start condition is identified by a falling edge of SDATA while SCLK is stable at high state. A Start condition must precede any data/command transfer. The device continuously monitors for a Start condition and will not respond to any transaction unless one is encountered.

6.2 Stop condition

A Stop condition is identified by a rising edge of SDATA while SCLK is stable at high state. A Stop condition terminates communication between the slave device and bus master. A read command that is followed by NoAck can be followed by a Stop condition to force the slave device into idle mode. When the slave device is in idle mode, it is ready to receive the next I^{2}C transaction. A Stop condition at the end of a write command stops the write operation to registers.

6.3 Acknowledge bit (ACK)

The acknowledge bit is used to indicate a successful byte transfer. The bus transmitter releases the SDATA after sending eight bits of data. During the ninth bit, the receiver pulls the SDATA low to acknowledge the receipt of the eight bits of data. The receiver may leave the SDATA in high state if it would to *not* acknowledge the receipt of the data.

6.4 Data input

The device samples the data input on SDATA on the rising edge of the SCLK. The SDATA signal must be stable during the rising edge of SCLK and the SDATA signal must change only when SCLK is driven low.

6.5 Slave device address

The slave device address is a 7 address, where the least significant 2-bit are programmable. These 2-bit values will be loaded in once upon reset and after that these 2 pins no longer be needed with the exception during General Call. Up to 4 STMPE2401 devices can be connected on a single I^2C bus.

Table 12. Slave device address

ADDR 1	ADDR 0	Address
0	0	0x84
0	1	0x86
1	0	0x88
1	1	0x8A

6.6 Memory addressing

For the bus master to communicate to the slave device, the bus master must initiate a Start condition and followed by the slave device address. Accompanying the slave device address, there is a Read/$\overline{\text{Write}}$ bit (R/$\overline{\text{W}}$). The bit is set to 1 for Read and 0 for Write operation.

If a match occurs on the slave device address, the corresponding device gives an acknowledgement on the SDA during the 9th bit time. If there is no match, it deselects itself from the bus by not responding to the transaction.

6.7 Operation modes

Table 13. Operating modes

Mode	Bytes	Programming sequence
Read	≥1	START, Device Address, R/$\overline{W}$ = 0, Register Address to be read
		RESTART, Device Address, R/$\overline{W}$ = 1, Data Read, STOP
		If no STOP is issued, the Data Read can be continuously preformed. If the register address falls within the range that allows address auto-increment, then register address auto-increments internally after every byte of data being read. For register address that falls within a non-incremental address range, the address will be kept static throughout the entire read operations. Refer to the Memory Map table for the address ranges that are auto and non-increment. An example of such a non-increment address is FIFO.
Write	≥1	START, Device Address, R/$\overline{W}$=0, Register Address to be written, Data Write, STOP
		If no STOP is issued, the Data Write can be continuously performed. If the register address falls within the range that allows address auto-increment, then register address auto-increments internally after every byte of data being written in. For register address that falls within a non-incremental address range, the address will be kept static throughout the entire write operations. Refer to the Memory Map table for the address ranges that are auto and non-increment. An example of such a non-increment address is Data Port for initializing the PWM commands.

Figure 3. Master/slave operation modes

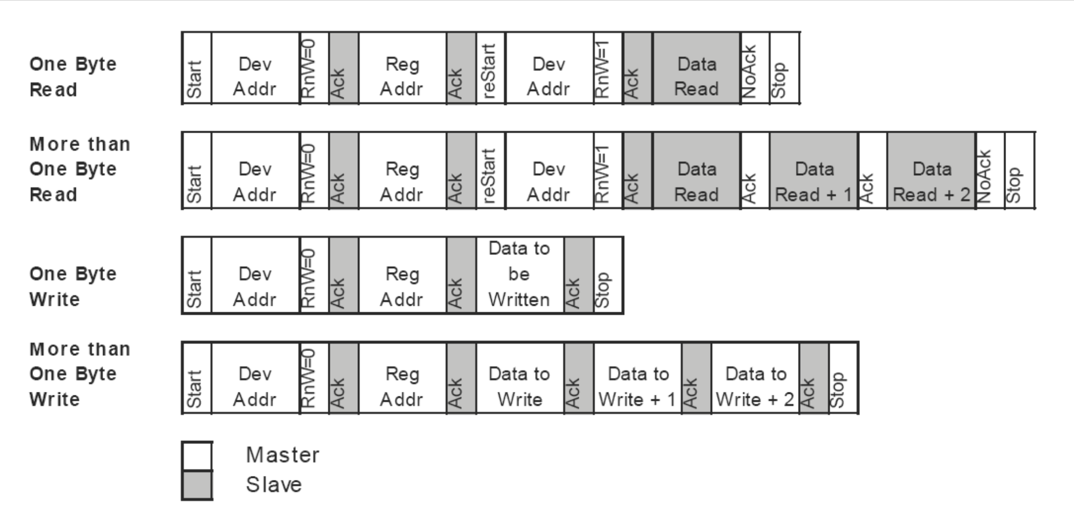


Figure 4. I2C timing

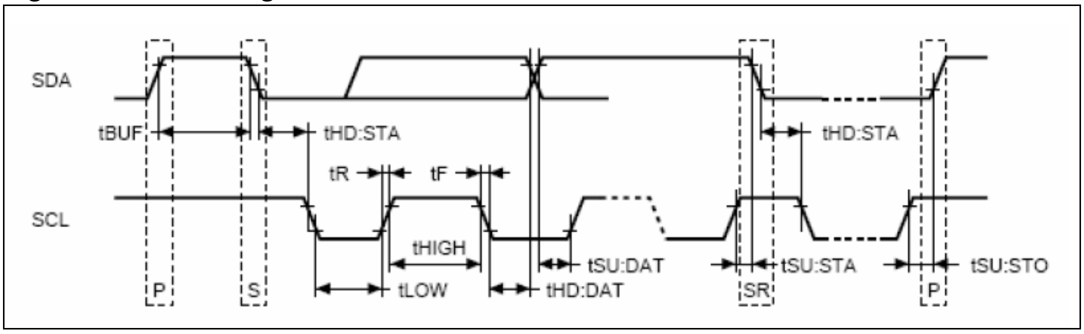


Table 14. I^{2}C address

Symbol	Parameter	Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency	0		400	kHz
t_{LOW}	Clock low period	1.3			µs
t_{HIGH}	Clock high period	600			ns
t_F	SDA and SCL fall time			300	ns
$t_{HD:STA}$	START condition hold time (After this period the first clock is generated)	600			ns
$t_{SU:STA}$	START condition setup time (Only relevant for a repeated start period)	600			ns
$t_{SU:DAT}$	Data setup time	100			ns
$t_{HD:DAT}$	Data hold time	0			µs
$t_{SU:STO}$	STOP condition setup time	600			ns
t_{BUF}	Time the bust must be free before a new trasmission can start	1.3			µs

7 System controller

The system controller is the heart of the STMPE2401. It contains the registers for power control, and the registers for chip identification.

The system registers are:

Table 15. System controller

Address	Register_Name
0x00	Reserved (Reads 0x00)
0x01	Reserved (Reads 0x00)
0x80	CHIP_ID
0x81	VERSION_ID
0x82	Reserved (Reads 0x00)
0x02	SYSCON

7.1 Identification register

Table 16. CHIP_ID

Bit	7	6	5	4	3	2	1	0
8-bit LSB of Chip ID								
Read/Write(IIC)	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	1

Table 17. VERSION_ID

Bit	7	6	5	4	3	2	1	0
8-bit Version ID								
Read/Write(IIC)	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	1

7.2 System control register

Table 18. System control register

Bit	7	6	5	4	3	2	1	0
	Soft_Reset	-	Disable_32KHz	Sleep	Enable_GPIO	Enable_PWM	Enable_KPC	Enable_ROT
Read/Write (IIC)	W		RW	RW	RW	RW	RW	RW
Read/Write(HW)	RW		R	RW	R	R	R	R
Reset Value	0		0	0	1	1	1	1

Table 19. System control register writing

Bits	Name	Description
0	Enable_ROT	Writing a '0' to this bit will gate off the clock to the Rotator module, thus stopping its operation
1	Enable_KPC	Writing a '0' to this bit will gate off the clock to the Keypad Controller module, thus stopping its operation
2	Enable_PWM	Writing a '0' to this bit will gate off the clock to the PWM module, thus stopping its operation
3	Enable_GPIO	Writing a '0' to this bit will gate off the clock to the GPIO module, thus stopping its operation
4	Sleep	Writing a '1' to this bit will put the device in sleep mode. When in sleep mode, all the units which need to work on clocks synchronous to 32KHz will get the clocks derived from the 32K domain. The RC Oscillator will be shut off.
5	Disable_32KHz	Set this bit to disable the 32KHz OSC, thus putting the device in hibernate mode. Only a Reset or a wakeup on IIC will reset this bit
6	-	-
7	Soft_Reset	Writing a '1' to this bit will do a soft reset of the device. Once the reset is done, this bit will be cleared to '0' by the HW.

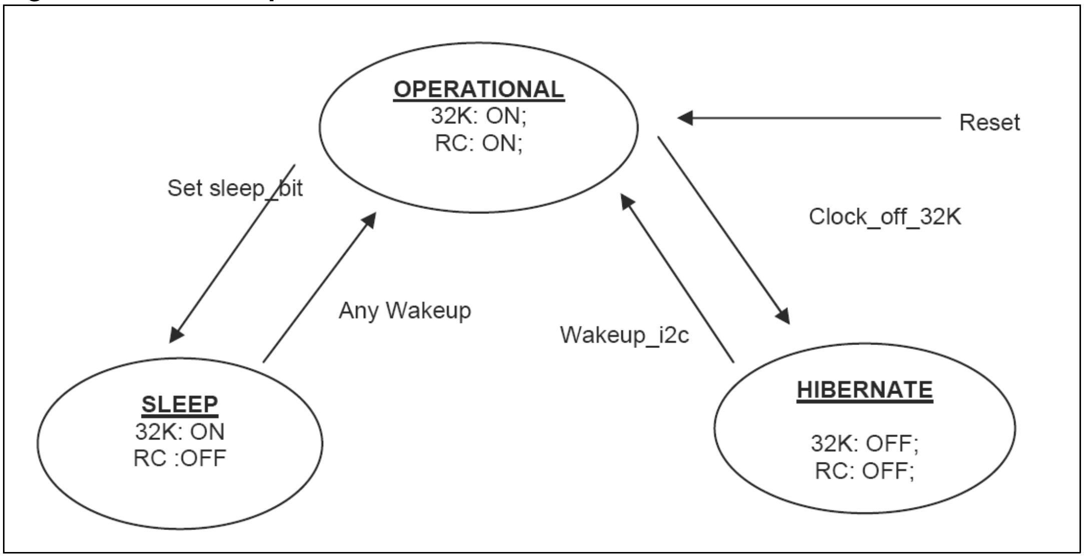
7.3 States of operation

The device has three main modes of operation:

- **Operational Mode**: This is the mode, whereby normal operation of the device takes place. In this mode, the RC clock is available and the Main FSM Unit routes this clock and the 32 KHz clock to all the device blocks that are enabled. In this mode, individual blocks that need not be working can be turned off by the master by programming the bits 3 to 0 of the SYSCON register.
- **Sleep Mode**: In this low-power mode, the RC Oscillator is powered down. All the blocks which need clocks derived from the 32KHz clock will continue getting a 32KHz clock. In this mode also, individual blocks can be turned off by the master by programming the bits 3 to 0 of the SYSCON register. However, the master needs to program the SYSCON register before coming into this mode, as in the sleep mode, the IIC interface is not active except to detect traffic for wakeup. Any activity on the I2C port or Wakeup pin or Hotkey activity will cause the device to leave this mode and go into the Operational mode. When leaving this mode, the I2C will need to hold the SCLK till the RC clock is ready.
- **Hibernate Mode:** This mode is entered when the system writes a '1' to bit 5 of the SYSCON register. In this mode, the device is completely inactive as there is absolutely no clock. Only a Reset or a wakeup on IIC will bring back the System to operational mode. All I2C activities are ignored.

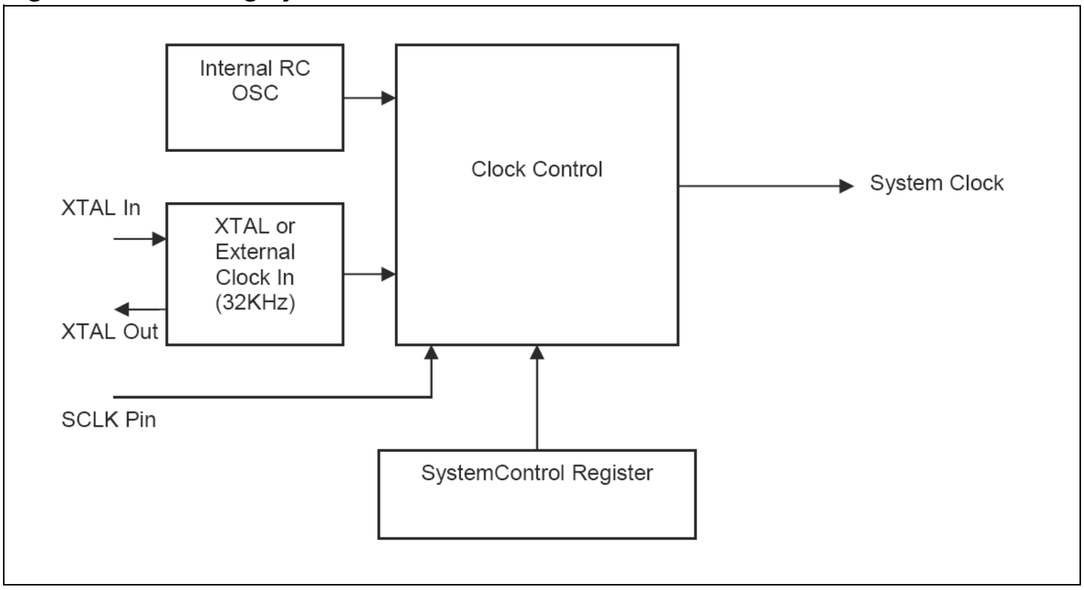
Caution: Hotkey detection is not possible in hibernate mode.

Figure 5. State of operation



8 Clocking system

Figure 6. Clocking system



The decision on clocks is based on the bits written into SYSCON registers. Bits 0 to 4 of the SYSCON register control the gating of clocks to the Rotator, Keypad Controller, PWM and GPIO respectively in the operational mode. When in sleep mode, the operating clock is cut off from every functional blocks (including the I^2C) except Keypad Controller and GPIO.

8.1 Programming sequence

To put the device in sleep mode, the following needs to be done by the host:

1. Write a ‘1’ to bit 4 of the SYSCON register.
2. To wakeup the device, the following needs to be done by the host:
3. Assert a wakeup routine on the I^2C bus by sending the Start Bit, followed by the device address and the R/W bit.
4. If there’s a NOACK, keep sending the wakeup routine till there is an ACK from the slave.
5. To do a soft reset to the device, the host needs to do the following:
6. Write a ‘1’ to bit 7 of the SYSCON register.
7. This bit is automatically cleared upon reset.
8. To go into Hibernate mode, the following needs to be done by the host:
9. Set the Disable_32K bit to ‘1’
10. To come out of the Hibernate mode, the following needs to be done by the host:
11. Assert a system reset or
12. Put a wakeup on the I^2C

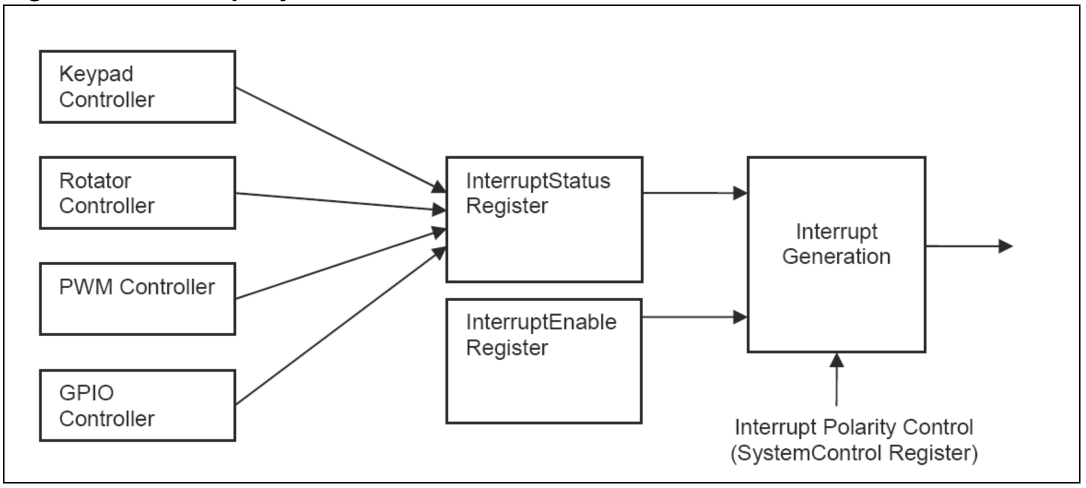
9 Interrupt system

STMPE2401 uses a highly flexible interrupt system. It allows host system to configure the type of system events that should result in an interrupt, and pinpoints the source of interrupt by status register. The INT pin could be configured as ACTIVE HIGH, or ACTIVE LOW. 32KHz clock input or crystal must be available for the interrupt system to be functional.

INT pin is 3.3V tolernat.

Once asserted, the INT pin would de-assert only if the corresponding bit in the InterruptStatus register is cleared.

Figure 7. Interrupt system



9.1 Register map of interrupt system

Table 20. Register map of interrupt system

Address	Register Name	Description	Auto-Increment (during sequential R/W)
0x10	ICR_msb	Interrupt Control Register	Yes
0x11	ICR_lsb		Yes
0x12	IER_msb	Interrupt Enable Mask Register	Yes
0x13	IER_lsb		Yes
0x14	ISR_msb	Interrupt Status Register	Yes
0x15	ISR_lsb		Yes
0x16	IEGPIOR_msb	Interrupt Enable GPIO Mask Register	Yes
0x17	IEGPIOR_mid		Yes
0x18	IEGPIOR_lsb		Yes
0x19	IEGPIOR_msb	Interrupt Status GPIO Register	Yes
0x1A	ISGPIOR_mid		Yes
0x1B	ISGPIOR_lsb		Yes

9.2 Interrupt control register (ICR)

ICR register is used to configure the Interrupt Controller. It has a global enable interrupt mask bit that controls the interruption to the host.

	ICR_msb								ICR_lsb							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved													IC2	IC1	IC0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW	RW
Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 21. ICR

Bits	Name	Description
0	IC[0]	Global Interrupt Mask bit When this bit is written a ‘1’, it will allow interruption to the host. If it is written with a ‘0’, then, it disables all interruption to the host. Writing to this bit does not affect the IER value.
1	IC[1]	output Interrupt Type ‘0’ = Level interrupt ‘1’ = Edge interrupt
2	IC[2]	output Interrupt Polarity ‘0’ = Active Low / Falling Edge ‘1’ = Active High / Rising Edge

9.3 Interrupt enable mask register (IER)

IER register is used to enable the interruption from a particular interrupt source to the host.

	IER_msb								IER_lsb							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved							IE8	IE7	IE6	IE5	IE4	IE3	IE2	IE1	IE0
R/W	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 22. IER

Bits	Name	Description
8:0	IE[x]	Interrupt Enable Mask (where x = 8 to 0) IE0 = Wake-up Interrupt Mask IE1 = Keypad Controller Interrupt Mask IE2 = Keypad Controller FIFO Overflow Interrupt Mask IE3 = Rotator Controller Interrupt Mask IE4 = Rotator Controller Buffer Overflow Interrupt Mask IE5 = PWM Channel 0 Interrupt Mask IE6 = PWM Channel 1 Interrupt Mask IE7 = PWM Channel 2 Interrupt Mask IE8 = GPIO Controller Interrupt Mask Writing a ‘1’ to the IE[x] bit will enable the interruption to the host.

9.4 Interrupt status register (ISR)

ISR register monitors the status of the interruption from a particular interrupt source to the host. Regardless whether the IER bits are enabled or not, the ISR bits are still updated.

	ISR_msb								ISR_lsb							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved							IS8	IS7	IS6	IS5	IS4	IS3	IS2	IS1	IS0
R/W	R	R	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 23. ISR

Bits	Name	Description
8:0	IS[x]	Interrupt Status (where x = 8 to 0) **Read:** IS0 = Wake-up Interrupt Status IS1 = Keypad Controller Interrupt Status IS2 = Keypad Controller FIFO Overflow Interrupt Status IS3 = Rotator Controller Interrupt Status IS4 = Rotator Controller Buffer Overflow Interrupt Status IS5 = PWM Channel 0 Interrupt Status IS6 = PWM Channel 1 Interrupt Status IS7= PWM Channel 2 Interrupt Status IS8 = GPIO Controller Interrupt Status **Write:** A write to a IS[x] bit with a value of ‘1’ will clear the interrupt and a write with a value of ‘0’ has no effect on the IS[x] bit.

9.5 Interrupt enable GPIO mask register (IEGPIOR)

IEGPIOR register is used to enable the interruption from a particular GPIO interrupt source to the host. The IEG[15:0] bits are the interrupt enable mask bits correspond to the GPIO[15:0] pins.

IEGPIOR_msb

Bit	23	22	21	20	19	18	17	16
	IEG 23	IEG 22	IEG 21	IEG 20	IEG 19	IEG 18	IEG 17	IEG 16
R/W	RW	RW	RW	RW	RW	RW	RW	RW
Reset Value	0	0	0	0	0	0	0	0

IEGPIOR _lsb

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IEG 15	IEG 14	IEG 13	IEG 12	IEG 11	IEG 10	IEG 9	IEG 8	IEG 7	IEG 6	IEG 5	IEG 4	IEG 3	IEG 2	IEG 1	IEG 0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 24. GPIO

Bits	Name	Description
23:0	IEG[x]	Interrupt Enable GPIO Mask (where x = 23 to 0) Writing a ‘1’ to the IE[x] bit will enable the interruption to the host.