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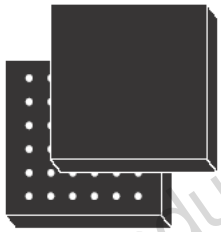
STMPE2403

24-bit Enhanced port expander with Keypad and PWM controller Xpander logic

Features

- 24 GPIOs
- Operating voltage 1.8V
- Hardware key pad controller (8*12 matrix max)
- 8 Special Function Key support
- 3 PWM (8 bit) output for LED brightness control and blinking
- Interrupt output (open drain) pin
- Configurable hotkey feature on each GPIO
- Ultra-low Standby-mode current
- Package TFBGA - 36 pins 3.6x3.6mm, pitch 0.5mm



TFBGA

Description

The STMPE2403 is a GPIO (General Purpose Input / Output) port expander able to interface a Main Digital ASIC via the two-line bidirectional bus (I^2C); separate GPIO Expander IC is often used in Mobile-Multimedia platforms to solve the problems of the limited amounts of GPIOs usually available on the Digital Engine.

The STMPE2403 offers great flexibility as each I/Os is configurable as input, output or specific functions; it's able to scan a keyboard, also provides PWM outputs for brightness control in backlight, rotator decoder interface and GPIO. This device has been designed very low quiescent current, and is including a wake up feature for each I/O, to optimize the power consumption of the IC.

Potential application of the STMPE2403 includes portable media player, game console, mobile phone, smart phone

Table 1. Device summary

Part Number	Package	Packaging
STMPE2403TBR	TFBGA36	Tape and reel

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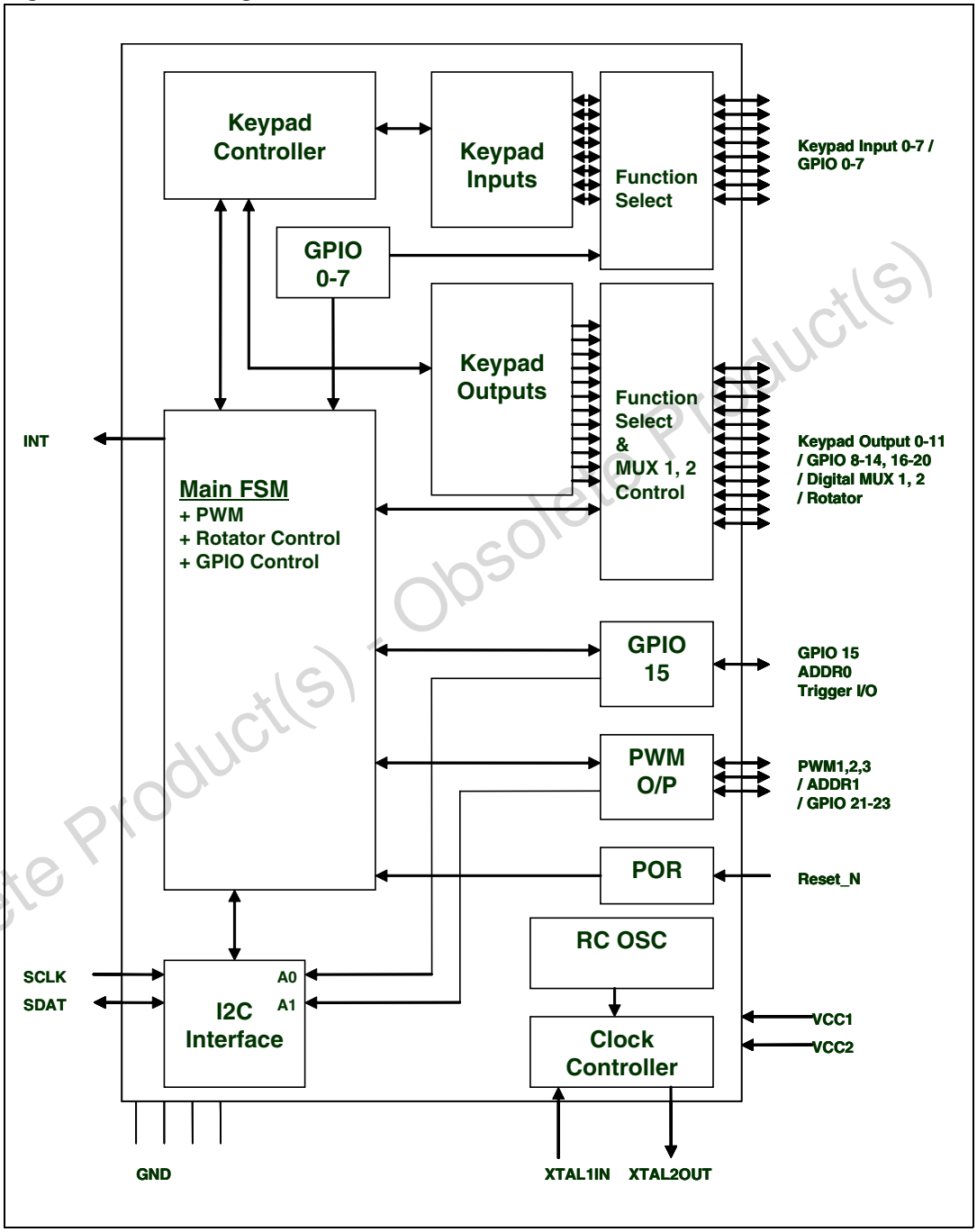
1 Block diagram

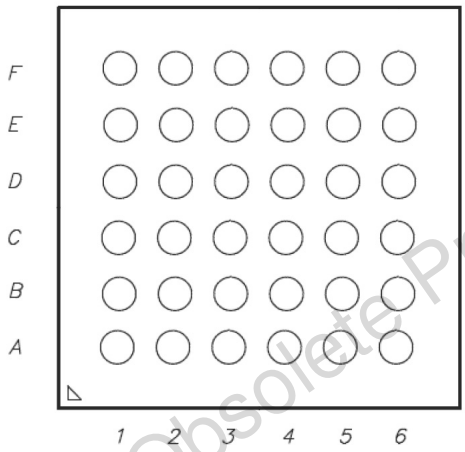
Figure 1. Block diagram



2 Pin settings

2.1 Pin connection

Figure 2. Pin connection



TFBGA

2.2 Pin assignment and TFBGA ball location

Table 2. Pin assignment

Ball	Name	Type	Description
C3	GND1	-	
A6	KP_X0	IO	GPIO
C1	Reset_N	I	External reset input, active LOW
A5	KP_X1	IO	GPIO
F1	KP_X2	IO	GPIO
F2	KP_X3	IO	GPIO
A2	KP_X4	IO	GPIO
B3	KP_X5	IO	GPIO
A3	KP_X6	IO	GPIO
D3	GND2	-	
A4	VCC1	-	1.8V Input

Table 2. Pin assignment (continued)

Ball	Name	Type	Description
B4	KP_X7	IO	GPIO
A1	KP_Y5	IO	GPIO
B2	KP_Y4	IO	GPIO
B5	KP_Y3	IO	GPIO
B6	KP_Y2	IO	GPIO
C5	KP_Y1	IO	GPIO
C6	KP_Y0	IO	GPIO
C4	GND3	-	
D6	ADDR0	IO	GPIO and I2C ADDR 0 (in reset)
D5	KP_Y9	A/IO	GPIO/MUX
E6	KP_Y10	A/IO	GPIO/MUX
F6	KP_Y11	A/IO	GPIO/MUX
E5	PWM3	A/IO	GPIO and I2C ADDR 1 (in reset) /MUX
F5	PWM2	A/IO	GPIO/MUX
E4	PWM1	A/IO	GPIO/MUX
F4	VCC2	-	1.8V Input
D4	GND4	-	
F3	INT	O	Open drain interrupt output pin
E3	KP_Y8	IO	GPIO
C2	KP_Y7	IO	GPIO
B1	KP_Y6	IO	GPIO
E2	SDATA	A	I2C DATA
E1	SCLK	A	I2C Clock
D2	XTALIN	A	XTAL Oscillator or External 32KHz input. be left floating.
D1	XTALOUT	A	XTAL Oscillator

2.3 GPIO Pin functions

Table 3. GPIO Pin functions

Name	Primary Function	Alternate Function 1	Alternate Function 2	Alternate Function 3
KP_X0	GPIO 0	Keypad input 0		
KP_X1	GPIO 1	Keypad input 1		
KP_X2	GPIO 2	Keypad input 2		
KP_X3	GPIO 3	Keypad input 3		
KP_X4	GPIO 4	Keypad input 4		
KP_X5	GPIO 5	Keypad input 5		
KP_X6	GPIO 6	Keypad input 6		
KP_X7	GPIO 7	Keypad input 7		
KP_Y5	GPIO 13	Keypad Output 5		
KP_Y4	GPIO 12	Keypad Output 4		
KP_Y3	GPIO 11	Keypad Output 3		
KP_Y2	GPIO 10	Keypad Output 2		
KP_Y1	GPIO 9	Keypad Output 1		
KP_Y0	GPIO 8	Keypad Output 0		
ADDR0	GPIO 15			
KP_Y9	GPIO 18	Keypad Output 9	Rotator 0	Mux1_In_1
KP_Y10	GPIO 19	Keypad Output 10	Rotator 1	Mux1_In_2
KP_Y11	GPIO 20	Keypad Output 11	Rotator 2	Mux1_Out
PWM3	GPIO 23			Mux2_Out
PWM2	GPIO 22			Mux2_In_2
PWM1	GPIO 21			Mux2_In_1
KP_Y8	GPIO 17	Keypad Output 8		ClkOut
KP_Y7	GPIO 16	Keypad Output 7		
KP_Y6	GPIO 14	Keypad Output 6		

2.4 Pin mapping to TFBGA (bottom view, balls up)

Table 4. Pin mapping to TFBGA (bottom view, balls up)

	A	B	C	D	E	F
1	KP_Y5	KP_Y6	RESET	XTALOUT	SCLK	KP_X2
2	KP_X4	KP_Y4	KP_Y7	XTALIN	SDATA	KP_X3
3	KP_X6	KP_X5	GND1	GND2	KP_Y8	INT
4	VCC1	KP_X7	GND3	GND4	PWM-1	VCC2
5	KP_X1	KP_Y3	KP_Y1	KP_Y9	PWM-3	PWM-2
6	KP_X0	KP_Y2	KP_Y0	ADDR0	KP_Y10	KP_Y11

3 Maximum rating

Stressing the device above the rating listed in the “Absolute Maximum Ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

3.1 Absolute maximum rating

Table 5. Absolute maximum rating

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	2.5	V
V_{IN}	Input voltage on GPIO pin	2.5	V
V_{IN} I2C	Input voltage on I2C pin	4.5	V
VESD (HBM)	ESD protection on each GPIO pin	2	KV

3.2 Thermal data

Table 6. Thermal data

Symbol	Parameter	Min	Typ	Max	Unit
R_{thJA}	Thermal resistance junction-ambient		100		°C/W
T_A	Operating ambient temperature	-40	25	85	°C
T_J	Operating junction temperature	-40	25	125	°C

4 Electrical specification

4.1 DC electrical characteristics

Table 7. DC electrical characteristics

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ.	Max.	
VCC1,2	Supply voltage		1.65	1.8	1.95	V
$I_{HIBERNATE1}$	HIBERNATE mode current	XTALIN not floating		15	20	uA
$I_{HIBERNATE2}$	HIBERNATE mode current	XTALIN floating		35	40	uA
I_{SLEEP1}	SLEEP mode current	XTALIN not floating		55	100	uA
I_{SLEEP2}	SLEEP mode current	XTALIN floating		75	120	uA
Icc	Operating current (FSM working – No peripheral activity)			1.2	1.6	mA
INT	Open drain output current			4		mA

4.2 I/O DC electrical characteristics

The 1.8V I/O complies to the EIA/JEDEC standard JESD8-7.

Table 8. I/O DC electrical characteristic

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
Vil	Low level input voltage			0.35*Vcc = 0.63	V
Vih	High level input voltage	0.65*Vcc = 1.17			V
Vhyst	Schmitt trigger hysteresis		0.10		V

4.3 DC input specification

(1.55V < V_{DD} < 1.95V)

Table 9. DC input specification

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ.	Max.	
Vol	Low level output voltage	Iol = 4mA			0.45	V
Voh	High level output voltage	Ioh = 4mA	Vcc - 0.45 = 1.35			V
Vol_PWM	Low level output voltage	Iol = 16mA			0.45	V
Voh_PWM	High level output voltage	Ioh = 16mA	Vcc - 0.45 = 1.35			V

4.4 DC output specification

(1.55V < vdd < 1.95V)

Table 10. DC output specification

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ.	Max.	
Ipu	Pull-up current	Vi = 0V	15	35	65	uA
Ipd	Pull-down current	Vi = vdd	14	35	60	uA
Rup	Equivalent pull-up resistance	Vi = 0V	30	50	103.3	KΩ
Rpd	Equivalent pull-down resistance	Vi = vdd	32.5	50	110.7	KΩ
Ron_1	Ron when the MUX is ON	Vsignal = 0V		5	10	Ω
Ron_2	Ron when the MUX is ON	Vsignal = 0.9V		5	20	Ω
Ron_3	Ron when the MUX is ON	Vsignal = 1.8V		10	10	Ω
Ron	Ron when the MUX is ON	Vsignal < 1.8V		20	35	Ω

Note: Pull-up and Pull-down characteristics

4.5 AC characteristics

Table 11. AC characteristics

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
Int_32KHz	Internally generated 32KHz clock	22	28	41.6	KHz

5 Register map

All registers have the size of 8-bit. For each of the module, their registers are residing within the given address range.

Table 12. Register map

Address	Module registers	Description	**Auto-Increment** (during read/write)
0x00 – 0x07 0x80 – 0x81	Clock and power Manager module	Clock and Power Manager register range.	Yes
0x10 – 0x1F	Interrupt controller module	Interrupt Controller register range	Yes
0x30 – 0x37	PWM controller module	PWM Controller register range	Yes
0x38 – 0x3F		PWM Controller register range	No
0x60 – 0x6F	Keypad controller module	Keypad Controller register range	Yes
0x70 – 0x77	Rotator controller module	Rotator Controller register range	Yes
0x82 – 0xBF	GPIO Controller Module	GPIO Controller register range	Yes

6 I²C Interface

The features that are supported by the I²C interface are as below:

- I²C Slave device
- Operates at 1.8V
- Compliant to Philip I²C specification version 2.1
- Supports Standard (up to 100kbps) and Fast (up to 400kbps) modes.
- 7-bit and 10-bit device addressing modes
- General Call
- Start/Restart/Stop
- Address up to 4 STMPE2403 devices via I²C

The address is selected by the state of two pins. The state of the pins will be read upon reset and then the pins can be configured for normal operation. The pins will have a pull-up or down to set the address. The I²C interface module allows the connected host system to access the registers in the STMPE2403.

6.1 Start condition

A Start condition is identified by a falling edge of SDATA while SCLK is stable at high state. A Start condition must precede any data/command transfer. The device continuously monitors for a Start condition and will not respond to any transaction unless one is encountered.

6.2 Stop condition

A Stop condition is identified by a rising edge of SDATA while SCLK is stable at high state. A Stop condition terminates communication between the slave device and bus master. A read command that is followed by NoAck can be followed by a Stop condition to force the slave device into idle mode. When the slave device is in idle mode, it is ready to receive the next I²C transaction. A Stop condition at the end of a write command stops the write operation to registers.

6.3 Acknowledge bit (ACK)

The acknowledge bit is used to indicate a successful byte transfer. The bus transmitter releases the SDATA after sending eight bits of data. During the ninth bit, the receiver pulls the SDATA low to acknowledge the receipt of the eight bits of data. The receiver may leave the SDATA in high state if it would to *not* acknowledge the receipt of the data.

6.4 Data input

The device samples the data input on SDATA on the rising edge of the SCLK. The SDATA signal must be stable during the rising edge of SCLK and the SDATA signal must change only when SCLK is driven low.

6.5 Slave device address

The slave device address is a 7 or 10-bit address, where the least significant 2-bit are programmable. These 2-bit values will be loaded in once upon reset and after that these 2 pins no longer be needed with the exception during General Call. Up to 4 STMPE2403 devices can be connected on a single I^2C bus.

Table 13. Slave device address

ADDR 1	ADDR 0	Address
0	0	0x84
0	1	0x86
1	0	0x88
1	1	0x8A

6.6 Memory addressing

For the bus master to communicate to the slave device, the bus master must initiate a Start condition and followed by the slave device address. Accompanying the slave device address, there is a Read/$\overline{\text{Write}}$ bit (R/$\overline{\text{W}}$). The bit is set to 1 for Read and 0 for Write operation.

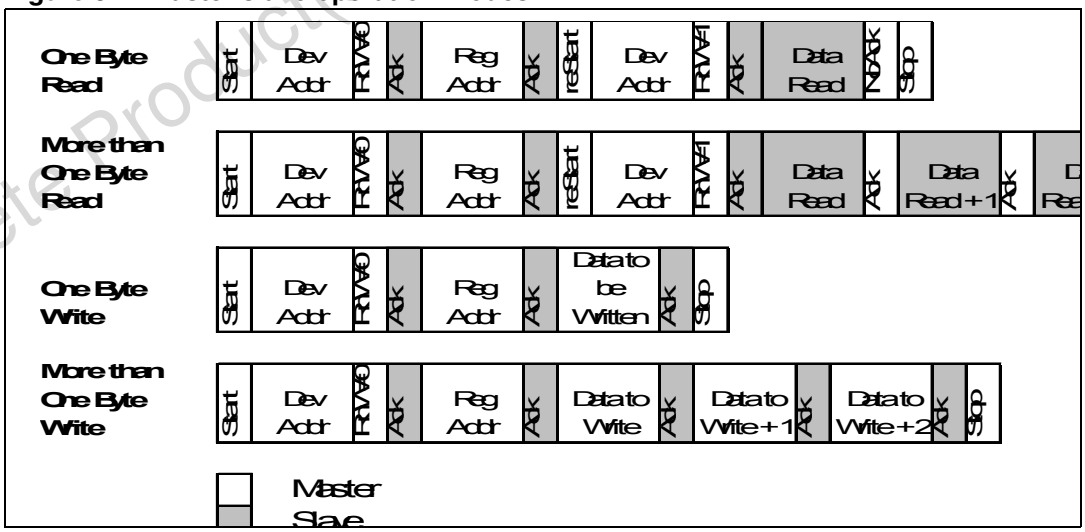
If a match occurs on the slave device address, the corresponding device gives an acknowledgement on the SDA during the 9^{th} bit time. If there is no match, it deselects itself from the bus by not responding to the transaction.

6.7 Operation modes

Table 14. Operation modes

Mode	Bytes	Programming Sequence
Read	≥1	START, Device Address, R/$\overline{W}$ = 0, Register Address to be read
		reSTART, Device Address, R/$\overline{W}$ = 1, Data Read, STOP
		If no STOP is issued, the Data Read can be continuously preformed. If the register address falls within the range that allows address auto-increment, then register address auto-increments internally after every byte of data being read. For register address that falls within a non-incremental address range, the address will be kept static throughout the entire read operations. Refer to the Memory Map table for the address ranges that are auto and non-increment. An example of such a non-increment address is FIFO.
Write	≥1	START, Device Address, R/$\overline{W}$ = 0, Register Address to be written, Data Write, STOP
		If no STOP is issued, the Data Write can be continuously performed. If the register address falls within the range that allows address auto-increment, then register address auto-increments internally after every byte of data being written in. For register address that falls within a non-incremental address range, the address will be kept static throughout the entire write operations. Refer to the Memory Map table for the address ranges that are auto and non-increment. An example of a non-increment address is Data Port for initializing the PWM commands.

Figure 3. Master/slave operation modes



6.8 General call address

A general call address is a transaction with the slave address of 0x00 and R/$\overline{W}$ = 0. When a general call address is made, STMPE2403 responds to this transaction with an acknowledgement and behaves as a slave-receiver mode. The meaning of a general call address is defined in the second byte sent by the master-transmitter.

Table 15.

R/$\overline{W}$	Second byte value	Definition
0	0x06	2-byte transaction in which the second byte tells the slave device to reset and write (or latch in) the 2-bit programmable part of the slave address.
0	0x04	2-byte transaction in which the second byte tells the slave device not to reset and write (or latch in) the 2-bit programmable part of the slave address.
0	0x00	Not allowed as second byte.

Note: All other second byte value will be ignored.

7 System controller

The system controller is the heart of the STMPE2403. It contains the registers for power control, and the registers for chip identification.

The system registers are:

Table 16. System controller

Address	Register_Name
0x00	Reserved (Reads 0x00)
0x01	Reserved (Reads 0x00)
0x02	SYSCON
0x03	SYSCON2
0x80	CHIP_ID
0x81	VERSION_ID
0x82	Reserved (Reads 0x00)

7.1 Identification register

Table 17. CHIP_ID

Bit	7	6	5	4	3	2	1	0
8-bit LSB of Chip ID								
Read/Write(IIC)	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	1

Table 18. VERSION_ID

Bit	7	6	5	4	3	2	1	0
	8-bit Version ID							
Read/Write(IIC)	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	1	0

7.2 System control register

Table 19. System control register

Bit	7	6	5	4	3	2	1	0
	Soft_Reset	Clock_Source	Disable_32KHz	Sleep	Enable_GPIO	Enable_PWM	Enable_KPC	Enable_ROT
Read/ Write (IIC)	W	RW	RW	RW	RW	RW	RW	RW
Reset Value	0	0	0	0	1	1	1	1

Table 20. System control register writing

Bits	Name	Description
0	Enable_ROT	Writing a ‘0’ to this bit will gate off the clock to the Rotator module, thus stopping its operation
1	Enable_KPC	Writing a ‘0’ to this bit will gate off the clock to the Keypad Controller module, thus stopping its operation
2	Enable_PWM	Writing a ‘0’ to this bit will gate off the clock to the PWM module, thus stopping its operation
3	Enable_GPIO	Writing a ‘0’ to this bit will gate off the clock to the GPIO module, thus stopping its operation
4	Sleep	Writing a ‘1’ to this bit will put the device in sleep mode. When in sleep mode, all the units will work on 32KHz (typical) clock frequency.
5	Disable_32KHz	Set this bit to disable the 32KHz OSC, thus putting the device in hibernate mode. Only a Reset or a wakeup on IIC will reset this bit
6	Clock_Source	Set to ‘1’ if external 32KHz clock were to be used. ‘0’ by default.
7	Soft_Reset	Writing a ‘1’ to this bit will do a soft reset of the device. Once the reset is done, this bit will be cleared to ‘0’ by the HW.

7.3 System control register 2

Table 21. System control register 2

Bit	7	6	5	4	3	2	1	0
	Reserved	Reserved	Reserved	Reserved	AutoSleepEN	Sleep_2	Sleep_1	Sleep_0
Read/ Write (IIC)	R	R	R	R	RW	RW	RW	RW
Reset Value	0	0	0	0	0	0	0	0

Table 22. System control register 2

Bits	Name	Description
0	Sleep_0	“000” for 4mS delay “001” for 16mS delay “010” for 32mS delay “011” for 64mS delay “100” for 128mS delay “101” for 256mS delay “110” for 512mS delay “111” for 1024mS delay
1	Sleep_1	
2	Sleep_2	
3	AutoSleepEN	“1” to enable auto-sleep feature. “0” to disable auto-sleep.
4	Reserved	
5	Reserved	
6	Reserved	
7	Reserved	

7.4 States of operation

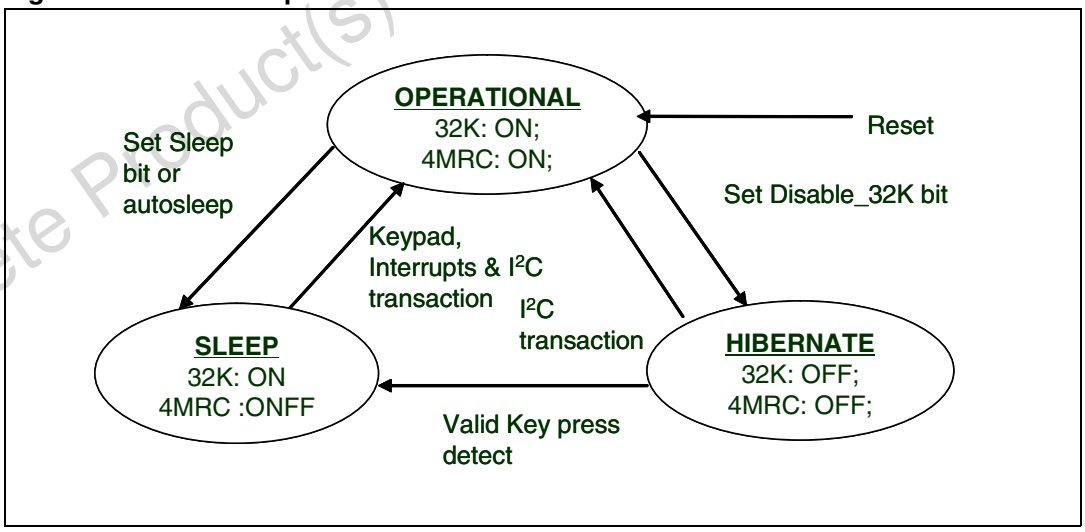
The device has three main modes of operation:

- **Operational Mode**: This is the mode, whereby normal operation of the device takes place. In this mode, the RC clock is available and the Main FSM Unit routes this clock and the 32 KHz clock to all the device blocks that are enabled. In this mode, individual blocks that need not be working can be turned off by the master by programming the bits 3 to 0 of the SYSCON register.
- **Sleep Mode**: In this low-power mode, individual blocks can be turned off by the master by programming the bits 3 to 0 of the SYSCON register. However, the master needs to program the SYSCON register before coming into this mode, as in the sleep mode, the IIC interface is not active except to detect traffic for wakeup. Any activity on the I2C port (intended I2C transaction for the device) or Wakeup pin or Hotkey activity will cause the device to leave this mode and go into the Operational mode. When leaving this mode, the I2C will need to hold the SCLK till the RC clock is ready.
- **Hibernate Mode**: This mode is entered when the system writes a '1' to bit 5 of the SYSCON register. In this mode, the device is completely inactive as there is absolutely no clock. Only a Reset or a wakeup on IIC will bring back the System to operational mode. A keypress detect will bring the system to Sleep mode, in which the debounce of the key will take place.

Note: 32KHz clock mentioned in this section could be (1) External clock from connected XTAL, (2) Externally fed 32KHz clock, or (3) internally generated (from RC OSC) clock. In the case that internal clock is used, it has a range of 25KHz to 45KHz.

Caution: Hotkey detection is not possible in hibernate mode.

Figure 4. States of operation



7.5 Autosleep

Host system may configure the STMPE2403 to go into sleep mode automatically whenever there is a period of inactivity following a complete I2C transaction with the STMPE2403. This inactivity means there is no intended I2C transaction for the device. For example, if there is I2C transaction sent by the host to other slave devices, the STMPE2403 device will still be counting down for the auto-sleep. The STMPE2403 device resets the autosleep time-out counter only when it receives an I2C transaction meant for the device itself. This autosleep feature is controlled by the System Control Register 2.

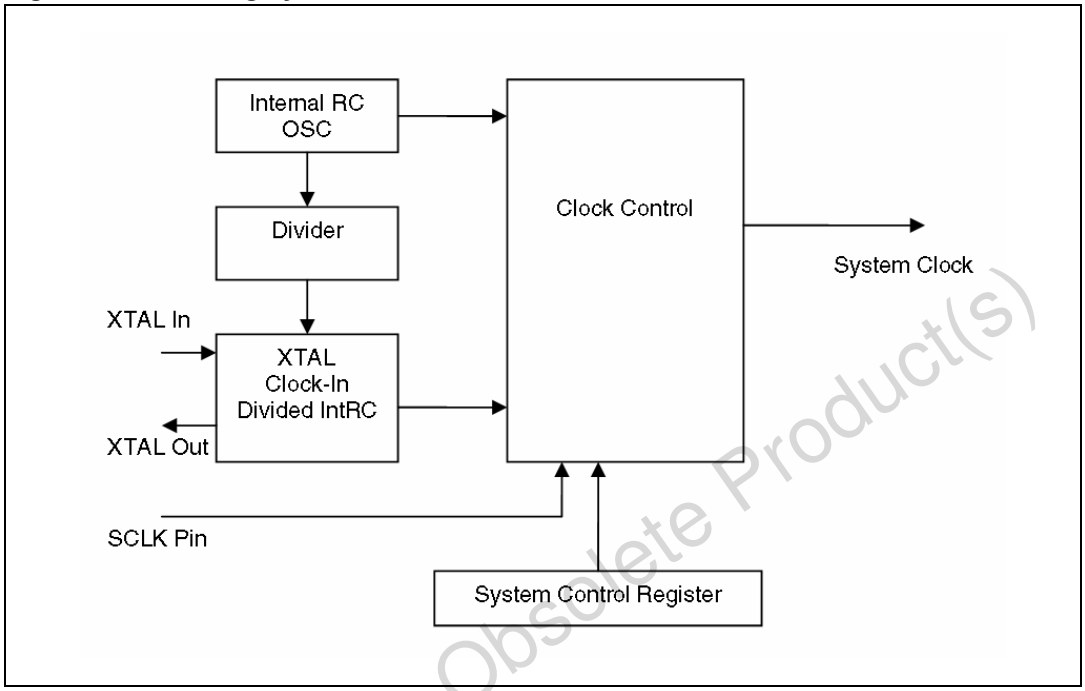
All events that trigger an interrupt (KPC, Rotator controller, Hot-Key) would result in a transition from SLEEP state to OPERATIONAL state automatically. The wake up can also be performed through I2C transaction intended for the device.

7.6 Keypress detect in the hibernate mode

When in hibernate mode, a keypress detect will cause the system to go into sleep mode. The sleep clock (32KHz) will then be used to debounce the key to detect a valid key. If the keypress is detected to be valid, the system staty in the sleep mode. If the key is detected to be invalid, the system will go back into hibernate mode.

8 Clocking system

Figure 5. Clocking system



The decision on clocks is based on the bits written into SYSCON registers. Bits 0 to 4 of the SYSCON register control the gating of clocks to the Rotator, Keypad Controller, PWM and GPIO respectively in the operational mode.

8.1 Clock source

By default, when the STMPE2403 powers up, it derives a 32KHz clock from the internal RC oscillator for it's operation. If external 32KHz crystal or clock source is available, it must be configured to accept external clock through the SYSCON register.

In the case where the STMPE2403 is powered and configured to use external clock, and the XTALIN is left floating, there will be an additional leakage current of approximately 20µA drawn from the V_{CC}.

8.2 Power mode programming sequence

To put the device in sleep mode, the following needs to be done by the host:

Write a '1' to bit 4 of the SYSCON register.

To wakeup the device, the following needs to be done by the host:

Assert a wakeup routine on the I2C bus by sending the Start Bit, followed by the device address and the Write bit. Subsequently, proceed with sending the Base Register address and continue with a normal I2C transaction. The device wakes up upon receiving the correct device address and in Write direction. In other words, the procedure of waking up the device is performed by just sending an I2C transaction to the device. This procedure can be extended to wake up the device that is in hibernate mode.

To do a soft reset to the device, the host needs to do the following:

Write a '1' to bit 7 of the SYSCON register.

This bit is automatically cleared upon reset.

To go into Hibernate mode, the following needs to be done by the host:

Set the Disable_32K bit to '1'

To come out of the Hibernate mode, the following needs to be done by the host:

Assert a system reset or

Put a wakeup on the I2C

9 Interrupt system

STMPE2403 uses a highly flexible interrupt system. It allows host system to configure the type of system events that should result in an interrupt, and pinpoints the source of interrupt by status register. The INT pin could be configured as ACTIVE HIGH, or ACTIVE LOW.

Once asserted, the INT pin would de-assert only if the corresponding bit in the Interrupt Status register is cleared.

Figure 6. Interrupt system