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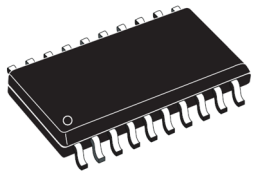
# STNRG011

# Digital combo multi-mode PFC and time-shift LLC resonant controller

**Datasheet - production data**



**SO20**

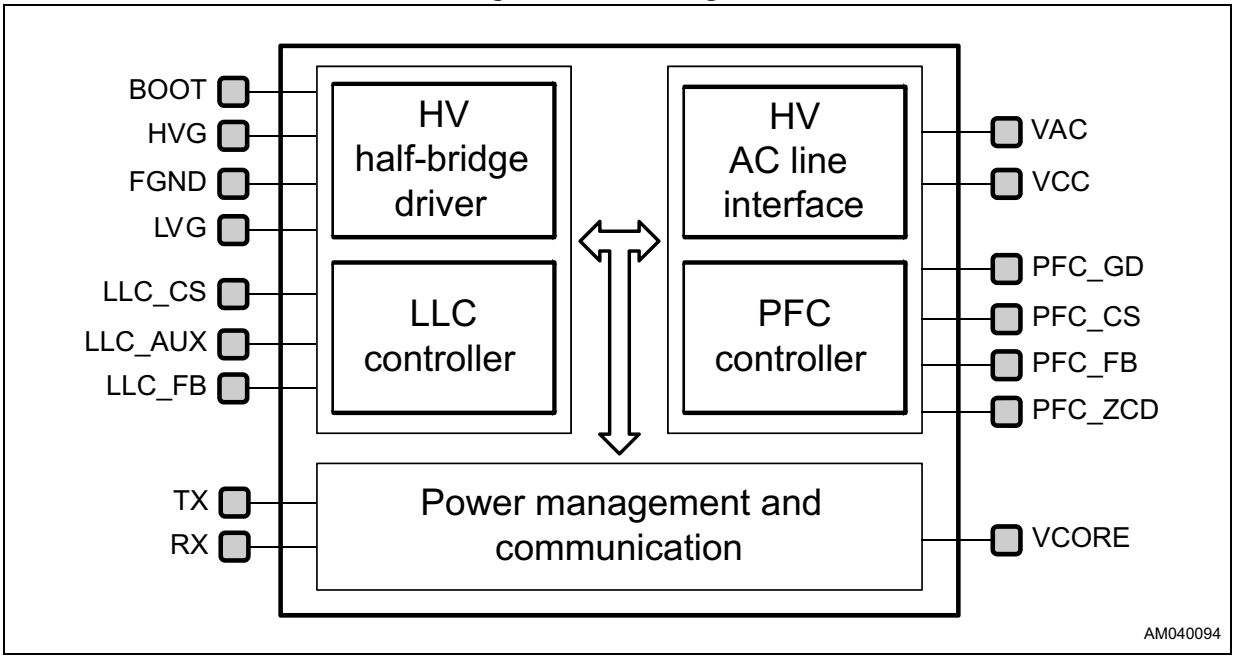
## Features

- Digital combo multi-mode PFC + time-shift LLC resonant half-bridge controller
- Onboard 800 V startup circuit, line sense and X-cap discharge compliant with IEC 62368-1, for reduced standby power
- Enhanced fixed on time multi-mode TM PFC controller with input voltage feedforward, THD optimizer and frequency limitation
- Complete set of PFC protections
- Time-shift control of resonant half-bridge
- Enhanced burst-mode at light load with fast transient response and line adaptive half-bridge brown-out protection
- Complete set of half-bridge protections
- Available in SO20 package

## Applications

- Open frame SMPS
- Flat screen TV SMPS
- ATX power supply
- AC-DC adapter

**Figure 1. Block diagram**






This is information on a product in full production. www.st.com

# Contents

# 1 Description

The STNRG011 embodies a multi-mode (transition-mode and DCM) PFC controller, a high-voltage double-ended controller for the LLC resonant half-bridge, an 800 V-rated startup generator and a sophisticated digital engine, that manage optimal operation of three blocks.

The device comes in a 20-pin SO package and offers an advanced solution for power-factor-corrected high-efficiency converters supposed to comply with the most stringent energy saving regulations.

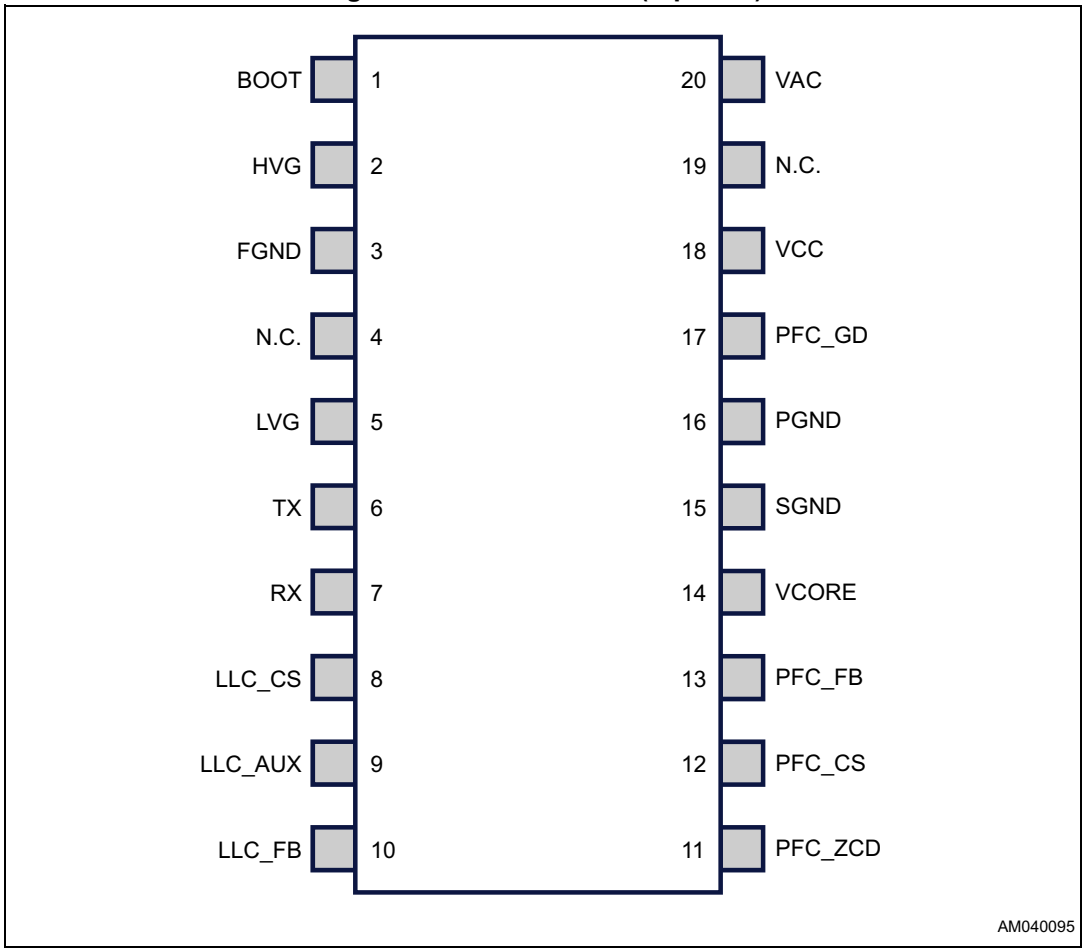
The power system and the control algorithms are managed by an 8-bit core with dedicated fast peripherals (SMED). Optimized digital algorithms together with HW analog IPs are implemented to guarantee a very high performance, BOM optimization and robustness.

The digital algorithms are stored into an internal ROM memory and all key application parameters can be stored into a device's NVM (non-volatile memory) memory during the production phase allowing wide configurability and calibration.

The device can also externally communicate through a 2-pin UART, allowing the monitoring function, the black box storing into an external $E^2$PROM and the software patch upload from the external $E^2$PROM.

# 2 Pin connection

**Figure 2. Pin connection (top view)**



# 3 Absolute maximum ratings and thermal data

**Table 1. Absolute maximum ratings**

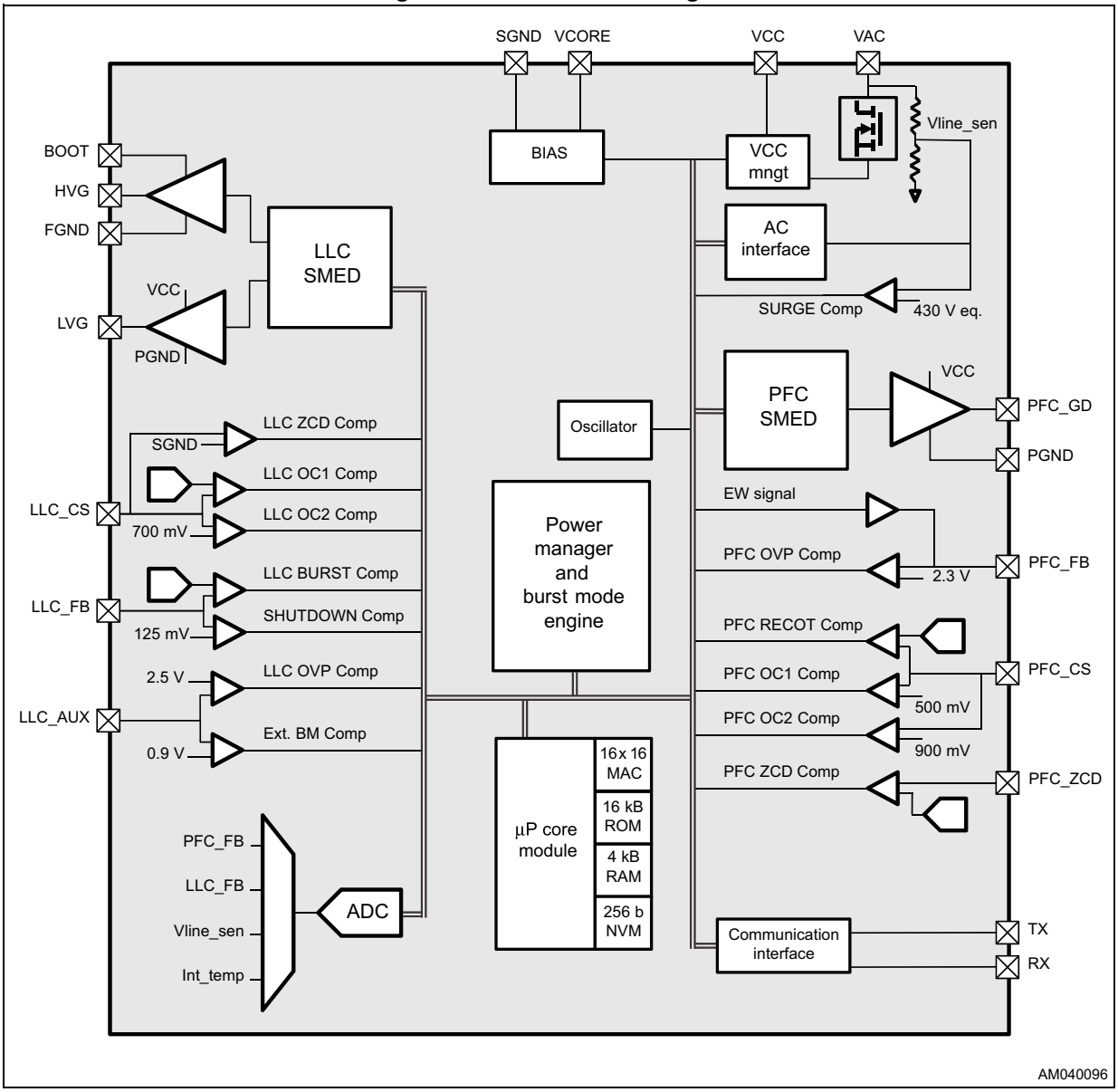
| Symbol | Pin | Parameter | Value | Unit |
|---|---|---|---|---|
| $V_{VAC}$ | VAC | Voltage range | -1 to 800 | V |
| $V_{BOOT}$ | BOOT | Floating supply voltage, referred to GND | -0.3 to 600 + VCC | V |
| $V_{FGND}$ | FGND | Floating ground voltage, connected to the half-bridge node | -3 up to a value included in the range BOOT - VCC and BOOT +0.3 | V |
| $dV_{FGND}$ /dt | FGND | Floating ground max. slew rate | 50 | V/ns |
| $V_{HVG}$ | HVG | HVG voltage | FGND -0.3 to BOOT +0.3 | V |
| $V_{VCC}$ | VCC | IC supply voltage | -0.3 to 19 | V |
| $V_{LVG}$ $V_{PFC\_GD}$ | LVG, PFC_GD | Voltage range | -0.3 to VCC | V |
| $V_{VCORE}$ | VCORE | Voltage range | -0.3 to 5.5 | V |
| $I_{PFC\_CS}$, $I_{LLC\_CS}$, $I_{PFC\_ZCD}$, | PFC_CS, LLC_CS, PFC_ZCD | Clamped source current (pin voltage: < 0 V, self-limited) | 2 | mA |
| $V_{PFC\_CS}$, $V_{LLC\_CS}$, $V_{PFC\_ZCD}$ | PFC_CS, LLC_CS, PFC_ZCD | Positive voltage range | VCORE +0.3 | V |
| $V_{PFC\_FB}$, $V_{LLC\_FB}$ | PFC_FB. LLC_FB | Voltage range | -0.3 to VCORE +0.3 | V |
| $V_{RX}$ | RX | Voltage range | -0.3 to VCORE +0.3 | V |
| $V_{TX}$ | TX | Voltage range | -0.3 to VCORE+ 0.3 | V |

**Table 2. Thermal data**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{th\ j\text{-}amb}$ | Max. thermal resistance, junction to ambient | 120 | °C/W |
| $T_j$ | Junction temperature operating range | -40 to 150 | °C |
| $T_{stg}$ | Storage temperature | -55 to 150 | °C |

# 4 Detailed block diagram

**Figure 3. Detailed block diagram**



# 5 Pin function

**Table 3. Pin function detailed description**

| No. | Name | Function |
|---|---|---|
| 1 | BOOT | High-side gate-drive floating supply voltage.<br>The bootstrap capacitor is connected between this pin and FGND.<br>A fast diode has to be connected from this pin and VCC to guarantee recharge of the bootstrap capacitor. |
| 2 | HVG | High-side gate-drive output.<br>The driver is capable of 0.5 A source and 0.75 A sink peak current (minimum values) to drive the upper MOSFET of the half-bridge leg.<br>A resistor internally connected to FGND ensures that the pin is never floating. |
| 3 | FGND | High-side gate-drive floating ground.<br>It is the return path for the high-side gate-drive current.<br>Layout carefully the connection of this pin to avoid too large spikes below ground. |
| 4 | N.C. | High-voltage spacer.<br>The pin is not internally connected to isolate the high-voltage section and ease compliance with safety regulations (creepage distance) on the PCB. |
| 5 | LVG | Low-side gate-drive output.<br>The driver is capable of 0.5 A source and 0.75 A sink peak current (minimum values) to drive the lower MOSFET of the half-bridge leg.<br>The pin is actively pulled to GND during UVLO. |
| 6 | TX | TX pin for UART/SDA pin for $I^2C$ interface |
| 7 | RX | RX pin for UART/SCL pin for $I^2C$ interface |
| 8 | LLC_CS | LLC tank current sensing input. A voltage proportional to the tank current (usually obtained with a capacitive divider) has to be applied to this pin.<br>The information is used for zero-crossing detection (required by time-shift algorithm), the first and second level OCP. |
| 9 | LLC_AUX | LLC_AUX is connected to a divider sensing the auxiliary voltage from the LLC transformer.<br>The LLC OVP detection is active on this pin. |
| 10 | LLC_FB | The voltage from this pin is used as the LLC feedback voltage. It has to be connected to the feedback phototransistor collector and a pull-up resistor to VCORE. |
| 11 | PFC_ZCD | PFC ZCD input, connected to the PFC AUX winding through a resistor divider detecting the PFC inductor demagnetization. |
| 12 | PFC_CS | Current sense input for PFC.<br>The current flowing in the MOSFET is sensed through a resistor, and the resulting voltage is applied to this pin.<br>After GD turns on, a first voltage threshold cross allows enhanced COT control implementation.<br>A second level can be detected for overcurrent protection. |
| 13 | PFC_FB | Input for PFC output voltage. It is used for closing the PFC loop and OVP protection. It has to be connected with a voltage divider to the bulk capacitor. If the early warning feature is enabled this pin is brought to 5 V when the EW pulse is released. |
| 14 | VCORE | Internal VCORE bypass capacitor connection. |

**Table 3. Pin function detailed description (continued)**

| No. | Name | Function |
|---|---|---|
| 15 | SGND | Signal ground. Reference ground for analog signals. |
| 16 | PGND | Power ground. Current return for the PFC gate-driver and the low-side gate-driver of the half-bridge. Keep the PCB trace that goes from this pin to the sources of the PFC and the low-side MOSFETs separate from the trace that collects the grounding of the bias components. |
| 17 | PFC_GD | PFC gate-driver output.<br>The output stage is able to drive power MOSFETs, it is capable of 0.7 A source current and 0.8 A sink current (minimum values). |
| 18 | VCC | Supply voltage of both the signal part of the IC and the gate-drivers. A bypass capacitor to GND is necessary to sustain the IC during startup and low power modes.<br>The voltage on the pin is internally clamped to protect the internal circuits from temporary excessive supply voltages. |
| 19 | N.C. | The pin is not internally connected to isolate the high-voltage section and ease compliance with safety regulations (creepage distance) on the PCB. |
| 20 | VAC | High-voltage startup generator input.<br>The pin has to be connected directly to the mains voltage through two dedicated diodes.<br>If the voltage on the pin is higher than 50 V, an internal current source charges the capacitor connected between the pin VCC and GND until the voltage on the VCC pin reaches the startup threshold.<br>Normally, the generator is re-enabled when the voltage on the VCC pin falls below the UVLO threshold.<br>The pin is also used as the line voltage sensing input.<br>This pin is internally connected to a 20 MΩ resistor divider. It is used for all line sense related functions: the AC brown-out, surge detection, line disconnection, input voltage feedforward, line synchronization.<br>When a line disconnection is detected, the internal current source is activated to discharge the X-capacitor. |

# 6 Electrical characteristics

$T_j$ = 0 to +125 °C, $V_{CC}$ = $V_{BOOT}$ = 15 V[a], $C_{HVG}$ = $C_{LVG}$ = $C_{PFC\_GD}$ = 1 nF; unless otherwise specified.

**Table 4. Electrical characteristics**

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Supply voltage** | | | | | | |
| Vccz | Vcc clamp voltage | - | 19 | - | - | V |
| Vcc | Operating range | After turn-on | 9.5 | - | 19 | V |
| $Vcc_{On}$ | Processing turn-on threshold | (1)Voltage rising | 16 | 17 | 18 | V |
| $Vcc_{Off}$ | Processing turn-off threshold | (1)Voltage falling | 8 | 8.7 | 9.4 | V |
| Hys | Hysteresis | - | - | 8.3 | - | V |
| $Vcc_{CoreOn}$ | VCC threshold for VCore turn-on | (1)Voltage rising | - | 8 | - | V |
| $Vcc_{CoreOff}$ | VCC threshold for VCore turn-off | (1)Voltage falling | - | 7 | - | V |
| VCore | Operating range | $I_{source}$ 0 to 1 mA | 4.75 | - | 5.25 | V |
| **Supply current** | | | | | | |
| $I_{Vccs}$ | Quiescent current during sleep (BM) | T 25 °C | - | 0.5 | - | mA |
| $I_{Vccop}$ | Operating supply current at $f_{sw}$ = 50 kHz, C = 1 nF, VCC = 12 V | PFC and LLC off | - | 18 | - | mA |
| | | PFC driver only (during PFC SS) | - | 20 | - | |
| | | All drivers | - | 22 | - | |
| **High-voltage startup generator** | | | | | | |
| $V_{VAC\_BR}$ | Breakdown voltage | $I_{HV}$ < 50 µA<br>$V_{CC}$ > $Vcc_{On}$ | 800 | - | - | V |
| $I_{VAC\_on}$ | ON-state VAC input current | $V_{VAC}$ > 40 V<br>$V_{CC}$ < 0.8 V | - | 1 | - | mA |
| | | $V_{VAC}$ > 40 V<br>0.8 V < $V_{CC}$ < $Vcc_{CoreOn}$ | - | 6 | - | |
| | | $V_{VAC}$ > 100 V<br>$Vcc_{CoreOn}$ < $V_{CC}$ < 14 V | - | 6 | - | |
| | | $V_{VAC}$ > 100 V<br>14 V < $V_{CC}$ < $Vcc_{On}$ | - | 4 | - | |
| | | 40 V < $V_{VAC}$ < 100 V<br>$Vcc_{CoreOn}$ < $V_{CC}$ < 14 V | - | 20 | - | |
| | | 40 V < $V_{VAC}$ < 100 V<br>14 V < $V_{CC}$ < $Vcc_{On}$ | - | 10 | - | |

a. Adjust $V_{CC}$ above $Vcc_{On}$ before setting at 15 V.

**Table 4. Electrical characteristics (continued)**

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{Vcc\_charge}$ | ON-state VCC charge current | $V_{VAC}$ > 40 V<br>$V_{CC}$ < 0.8 V | -0.5 | -0.75 | -1 | mA |
| | | $V_{VAC}$ > 40 V<br>0.8 V < $V_{CC}$ < $Vcc_{CoreOn}$ | -3.5 | -5 | -7 | |
| | | $V_{VAC}$ > 100 V<br>$Vcc_{CoreOn}$ < $V_{CC}$ < 14 V | - | -5 | - | |
| | | $V_{VAC}$ > 100 V<br>14 V < $V_{CC}$ < $Vcc_{On}$ | - | -3.5 | - | |
| | | 40 V < $V_{VAC}$ < 100 V<br>$Vcc_{CoreOn}$ < $V_{CC}$ < 14 V | - | -18 | - | |
| | | 40 V < $V_{VAC}$ < 100 V<br>14 V < $V_{CC}$ < $Vcc_{On}$ | - | -8 | - | |
| $I_{VAC\_off}$ | OFF-state VAC input current | $V_{VAC}$ = 400 V, $V_{CC}$ > $Vcc_{On}$ | - | 20 | 40 | µA |
| $I_{VAC\_HV\_SINK}$ | VAC reading improvement current | $V_{VAC}$ = 100 V | - | 100 | - | µA |
| **PFC - gate-driver** | | | | | | |
| $V_{OL}$ | Output low voltage | $I_{sink}$ = 100 mA | - | - | 0.7 | V |
| $V_{OH}$ | Output high voltage | $I_{source}$ = -10 mA<br>$V_{CC}$ = 10 V,<br><br>$V_{CC}$ = 18 V | 9.85<br><br>17.9 | 9.95<br><br>17.95 | -<br><br>- | V |
| $I_{srcpk}$ | Peak source current | Cgate = 4.7 nF(2) | -0.7 | -1.1 | - | A |
| $I_{snkpk}$ | Peak sink current | Cgate = 4.7 nF(2) | 0.8 | 1.3 | - | A |
| $t_f$ | Voltage fall time | - | - | 25 | - | ns |
| $t_r$ | Voltage rise time | - | - | 30 | - | ns |
| PFC_GD_uvlo | UVLO saturation | $V_{CC}$ = 0 to $Vcc_{On}$, $I_{sink}$ = 1 mA | - | 0.9 | 1.15 | V |
| **Low-side gate-driver** (voltages referred to GND) | | | | | | |
| $V_{OL}$ | Output low voltage | $I_{sink}$ = 100 mA | - | - | 0.7 | V |
| $V_{OH}$ | Output high voltage | $I_{source}$ = -10 mA<br>$V_{CC}$ = 10 V<br><br>$V_{CC}$ = 18 V | 9.85<br><br>17.85 | 9.9<br><br>17.9 | -<br><br>- | V |
| $I_{srcpk}$ | Peak source current | Cgate = 4.7 nF(2) | -0.5 | -0.8 | - | A |
| $I_{snkpk}$ | Peak sink current | Cgate = 4.7 nF(2) | 0.75 | 1.2 | - | A |
| $t_f$ | Voltage fall time | - | - | 25 | - | ns |
| $t_r$ | Voltage rise time | - | - | 40 | - | ns |
| LVG_uvlo | UVLO saturation | $V_{CC}$ = 0 to $Vcc_{On}$, $I_{sink}$ = 1 mA | - | 0.9 | 1.1 | V |

**Table 4. Electrical characteristics (continued)**

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **High-side gate-driver** (voltages referred to FGND) | | | | | | |
| $V_{OL}$ | Output low voltage | $I_{sink}$ = 100 mA | - | - | 0.7 | V |
| $V_{OH}$ | Output high voltage | $I_{source}$ = -10 mA<br>$V_{BOOT}$= 10 V,<br><br>$V_{BOOT}$ = 18 V | 9.85<br><br>17.85 | 9.9<br><br>17.9 | -<br><br>- | V |
| $I_{srcpk}$ | Peak source current | Cgate = 4.7 nF(2) | -0.5 | -0.8 | - | A |
| $I_{snkpk}$ | Peak sink current | Cgate = 4.7 nF(2) | 0.75 | 1.2 | - | A |
| $t_f$ | Voltage fall time | - | - | 25 | - | ns |
| $t_r$ | Voltage rise time | - | - | 40 | - | ns |
| HVG_pdw | HVG-FGND pull-down resistor | - | - | 25 | - | kΩ |
| $I_{FGND}$ | Current from $V_{BOOT}$ to FGND | $V_{BOOT}$ = 200 V | - | 1.5 | - | µA |
| **X-CAP discharge** | | | | | | |
| XCD_inact_time | Inactivity detection time | - | - | 50 | - | ms |
| $I_{XCD}$ | Discharge current | - | 4 | - | - | mA |
| **Brown-in/out** | | | | | | |
| BI | TH | Vline rising | 112 | 114 | 116 | V |
| BO | | Vline falling | - | 108 | - | V |
| BIBO_H | HYST | - | 5.25 | 6 | 6.75 | V |
| BO_mask | Brown-out time | - | - | 45 | - | ms |
| **Overtemperature** (by design) | | | | | | |
| OTP | TH | T rising | 130 | 140 | 150 | °C |
| | HYST | T falling | - | -30 | - | °C |
| **CK** | | | | | | |
| Fck | System clock in run mode | - | 57 | 60 | 63 | MHz |
| **ADC** | | | | | | |
| ADC_res | Resolution | Vin ADC > 50 mV | - | 10 | - | bit |
| FSR_L | Conversion range | CS | 0 | - | 1.5 | V |
| FSR_H | | Other | 0 | - | 2.5 | V |
| DNL | Differential non linearity | Vin ADC > 50 mV | - | ±1.5 | - | lsb |
| Fck_ADC | Clock frequency | Vin ADC > 50 mV | - | 15 | - | MHz |
| Ts | Sampling time | Vin ADC > 50 mV | - | 7 | - | ADC Ck cycles |

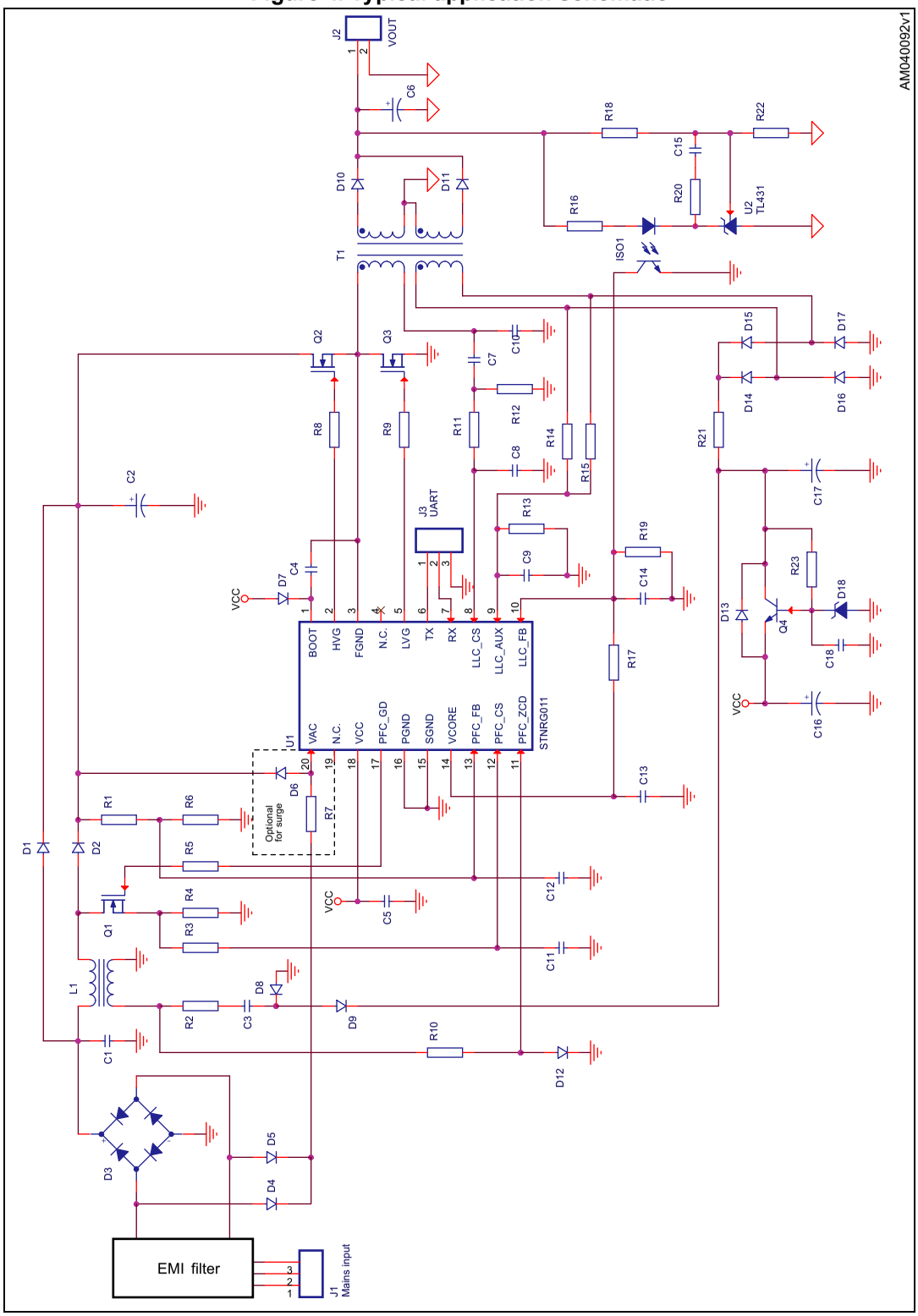
**Table 4. Electrical characteristics (continued)**

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Tc | Total conversion time (sampling included) | Vin ADC > 50 mV | - | 18 | - | ADC Ck cycles |
| **Comparators** | | | | | | |
| PFC_CS RECOT(3) | TH RISING (DAC 6 bits) | Input pin PFC_CS | FSR = 125 STEP = 1.95 | | | mV |
| | HYST | | 5 | | | |
| PFC_CS OC1 | TH RISING | Input pin PFC_CS | - | 500 | - | mV |
| | TH FALLING | | - | 450 | - | |
| PFC_CS OC2 | TH RISING | Input pin PFC_CS | - | 900 | - | mV |
| | TH FALLING | | - | 850 | - | |
| PFC_ZCD ZCD(3) | TH FALLING (TH_F) | Input pin PFC_ZCD | 0/50/100/200 | | | mV |
| | TH RISING (TH_R) | | 210/110(4)/310/ TH_F +10 | | | |
| PFC_FB OVP | TH RISING | Input pin PFC_FB | - | 2.33 | - | V |
| | HYST | | - | 75 | - | mV |
| LLC_FB(3) BURST | TH RISING | Input pin LLC_FB | 0.75/1/1.25 | | | V |
| | HYST | | 5/10 | | | mV |
| LLC_FB SHUTDOWN | TH RISING | Input pin LLC_FB | - | 145 | - | mV |
| | TH FALLING | | - | 125 | - | |
| LLC_AUX OVP | TH RISING | Input pin LLC_AUX | - | 2.5 | - | V |
| | TH FALLING | | - | 2.4 | - | |
| LLC_AUX Ext. BM | TH RISING | Input pin LLC_AUX | - | 0.9 | - | V |
| | TH FALLING | | - | 0.8 | - | |
| LINE SURGE | TH RISING | Input pin VAC | - | 430 | - | V |
| | TH FALLING | | - | 410 | - | |
| LLC_CS OC1(3) | TH RISING | Input pin LLC_CS | FSR = 500 STEP = 15.6 | | | mV |
| | HYST | | 20 | | | |
| LLC_CS OC2 | TH RISING | Input pin LLC_CS | - | 700 | - | mV |
| | TH FALLING | | - | 650 | - | |

1. Parameters tracking each other.
2. Guarantee by design, not production tested.
3. Thresholds and hysteresis are programmed by the software in use.
4. The selection for TH_R = 110 mV is not allowed if TH_F = 200 mV.

# 7 Application schematics

**Figure 4. Typical application schematic**



# 8 Architecture

The PFC and LLC external MOSFETs gates are managed by the “State Machine Event Driven” (SMEDs): 2 for PFC (PFC SMEDs) and 2 for LLC (LLC SMEDs).

The SMEDs are programmable state machine driven by events:

- External events
  - Analog comparators outputs
  - Power manager generated events (protections)
- Internal events
  - Timers events

**PFC SMEDs**

- Inputs events: PFC RECOT, PFC OC1, PFC ZCD
- Outputs: PFC_GD

**LLC SMEDs**

- Inputs events: LLC ZCD
- Outputs: LVG, HVG

The **µP subsystem** manages dynamically the control loop.

- Analog comparators thresholds setting
- SMED configuration
- SMED timers
- ADC scheduler
- Interrupt management

The multichannel **ADC** is controlled by a programmable event driven scheduler: sampling sequence can be configured and every sample can be triggered by a specific SMED state occurrence and an internal timer value. Different priorities can be programmed to allow fast sampling for real time control and slow sampling for state control (i.e. temperature).

The scheduler can be programmed to generate interrupts after completion of selectable conversions.

A dedicated **AC line monitor** easily follows the AC line providing system triggers.

The µP reads data from the ADC and performs the loop calculation with the support of a dedicated 16-b x 16-b multiplier and a 32-b accumulator unit.

A **Power management and burst-mode machine** manages the system power state in order to have very low idle consumption and fast activity restart during the burst-mode operation.

Hard protections are managed with a very low propagation delay; the protection enable and the latched/not latched response are programmable.

The power manager controls also the brown-in/out, VCC charge/discharge, AC monitor and X-cap discharge.

A **Watchdog** resets the system in case of missed µP signal for a long time.

A **communication peripheral** allows serial communication at startup and during the normal operation for:

- External memory communication for
  - Black box external recording
  - Patch SW upload
- Monitoring
- Internal memory R/W and OTP management
- Test mode

# 9 Functional description

The main functions are:

- HV startup and VCC management
- Line monitor and protection
- Drivers
- PFC control and fault management
- Resonant LLC HB control and fault management
- Power management
- Communication and configuration

## 9.1 HV startup and VCC management

The VAC pin voltage is a rectified sine wave at 100 Hz/120 Hz, connected to the mains AC line (Vline) through two dedicated diodes. The VAC pin is the device supply at the startup.

The VAC pin voltage is different from the PFC power path (Vin) where big caps are connected: the VAC pin partially follows the Vline also at no load condition while the Vin could be very close to a DC; this assumption allows to detect the AC line disconnection to implement the X-cap discharge function.

At the VAC pin a HV DMOS is internally connected to charge the capacitor connected to the VCC pin.

From the VCC pin an internal LDO provides the 5 V VCore for analog and digital circuitry; the digital section is supplied by the internal LDO from the VCORE pin.

At startup, from the HV DMOS the capacitor connected to the VCC pin is charged to provide the power supply to the whole device; then the HV DMOS is turned off.

The VCC pin starts sourcing current to the connected capacitor after a minimum 15 V VAC pin voltage.

The VCC capacitor charge current is limited to 0.75 mA during the first charge phase to limit the temperature increase in case the VCC pin is short-circuited at startup. After the VCC pin voltage is above 0.8 V, the charging current rises to 5 mA.

VCORE pin voltage rises when the VCC pin crosses 8 V ($Vcc_{CoreOn}$). There is a VCORE overload protection that limits the VCC charging current below 1 mA in case the VCORE pin is short-circuited at startup. Then the VCC capacitor charge continues with an average current higher than 6 mA: the current is increased during the time the VAC pin voltage is below 100 V.

Once the VCC pin crosses the 17 V $Vcc_{On}$ rising threshold the HV DMOS turns off and the whole device starts working: the µP boots.

If the VCC pin goes below the 9 V $Vcc_{Off}$ falling threshold (UVLO threshold) the µP stops working and the HV DMOS turns on again.

If the VCC pin falls below 7 V ($Vcc_{CoreOff}$) the device stops working and the capacitor connected to the VCORE pin discharges. The VCC pin can rise again only after the voltage on the VCORE pin falls below 1 V.

The worst case average charging current from the 0.8 V to the $Vcc_{on}$ threshold is estimated in 4.63 mA and 4.11 mA, in case the mains voltage is 115 Vac - 60 Hz and 230 Vac - 50 Hz respectively.

## 9.2 AC line monitor and protection

A HV voltage divider is internally connected to the VAC pin to generate Vline_sense for the AC line monitoring and protection:

- Brown-in/out
- Line synchronization
- Line disconnection and X-cap discharge
- Surge detection and stop
- Line monitor for PFC control

### 9.2.1 Brown-in/out

Brown-in and -out functions are implemented based on the Vline_sense information.

The peak VAC voltage is monitored to enable and disable the PFC.

The PFC is enabled when the AC line crosses the brown-in threshold. The PFC is disabled after 45 ms the AC line is below the brown-out threshold.

In order to improve AC line reading and avoid false brown-in, the HV DMOS is turned on sinking $I_{XCD}$ current for 100 ms in case of brown-out or line disconnection events. This function can be enabled / disabled through the dedicated NVM bit.

### 9.2.2 Line synchronization

A dedicated digital peripheral manages the PFC synchronization with the AC line sine wave.

In order to improve AC line reading and synchronization, the HV DMOS is turned on sinking $I_{VAC\_HV\_SINK}$ current at startup. This function can be enabled / disabled through the dedicated NVM bit.

### 9.2.3 Line disconnection and X-cap discharge

The Vline_sense is monitored to detect the AC line disconnection in order to discharge the X-cap through the internal HV DMOS.

The detection is based on AC activity absence on the VAC pin (the X-cap discharge function is triggered if there is no line activity for more than 50 ms). To discharge the X-cap, the HV DMOS turns on sinking a current of 4 mA minimum.

In order to improve AC line reading and avoid false brown-in, the HV DMOS is turned on sinking $I_{XCD}$ current for 100 ms in case of brown-out or line disconnection events. This function can be enabled / disabled through the dedicated NVM bit.

The discharge current stays on until the VAC pin is discharged or the AC line activity is detected again.

### 9.2.4 Vline surge stop

A surge can be detected on the VAC pin (430 V).

During the surge the PFC activity is stopped for one half-cycle.

If a line surge is detected during the PFC soft-start, the system shuts down with a not latched fault.

### 9.2.5 Line monitor for PFC control

A 20 MΩ voltage divider for the AC line monitor is internally connected from the VAC pin to GND.

### 9.2.6 Early warning signal

In case a brown-out or another stopping event (early warning managed faults) is detected then the STNRG011:

- Stops the PFC
- LLC continues switching for about 5 ms, trying to keep the LLC output voltage regulated
- PFC_FB pin is pulled up to VCore voltage for about 5 msec (early warning signal)

The early warning managed faults are

- Brown-out
- X-cap
- PFC UVP
- LLC OLP

If any other faults/events will occur, the STNRG011 will stop both PFC and LLC and will generate an early warning signal for about 250 μsec.

The early warning signal generation is active as soon as the device starts driving the PFC MOSFET.

This function can be enabled / disabled through the dedicated NVM bit.

## 9.3 Gate-drivers

The HVG and LVG are matched drivers. Deadtimes are programmable by the user.

During the burst-mode sleep phase, the HS BOOT capacitor discharges. The burst packets always start with a LVG pulse to recharge the bootstrap capacitor. A fast external bootstrap diode is necessary.

## 9.4 PFC control and fault management

### 9.4.1 PFC resources

**Table 5. Related pins**

| Pin name | Description | Level | Function |
|---|---|---|---|
| PFC_CS | PFC MOSFET current sense | 0 - 125 mV | 6-bit ramp enhanced COT feature |
| | | 500 mV | OCP1 |
| | | 900 mV | OCP2 fault |
| PFC_ZCD | PFC auxiliary connection for ZCD detection | - | - |
| PFC_FB | Reading for PFC Vout estimation | ADC, 10 bits | - |
| VAC | Mains line voltage reading | ADC, 10 bits | - |
| PFC_GD | PFC MOSFET gate-driver | - | - |

### 9.4.2 Vin reading

Input line voltage peak (Vin) reading on the VAC pin by the ADC at the AC line peak.

### 9.4.3 PFC output voltage feedback reading

PFC output voltage reading on the PFC_FB pin by the ADC.

### 9.4.4 PFC OVP comparator

The PFC OVP comparator sets the limit for the PFC output voltage.

It monitors the PFC_FB pin with respect to a fixed 2.3 V threshold.

### 9.4.5 PFC RECOT comparator

The PFC RECOT comparator implements the $T_{ON}$ adjustment for the ramp enhanced constant on-time (RECOT) control.

It monitors the PFC_CS pin with respect to a programmable threshold.

Its output communicates to the PFC SMED.

### 9.4.6 PFC OC1 comparator

The PFC OC1 comparator sets the limit for the operational maximum allowed peak current into the PFC MOSFET. If the OC1 threshold is hit the PFC_GD is turned off. This protection works cycle by cycle.

It monitors the PFC_CS pin with respect to a fixed 500 mV threshold.

Its output communicates to the PFC SMED.

### 9.4.7 PFC OC2 comparator

The PFC OC2 comparator sets an HW limit for the current flowing into the PFC MOSFET: it triggers the OCP fault.

It monitors the PFC_CS pin with respect to a fixed 900 mV threshold.

### 9.4.8 PFC ZCD

The PFC ZCD comparator performs the zero cross detection to implement the soft switching of the PFC MOSFET.

It monitors the PFC_ZCD pin with respect to two programmable rising and falling thresholds.

Its output communicates to the PFC SMED.

### 9.4.9 PFC state machine event driven (SMED)

The PFC high frequency operations are managed by a programmable 8-state ”State Machine Event Driven” (2 coupled 4-state SMEDs).

The SMED controls the PFC MOSFET based on the PFC comparators output and internally controlled counters.

It generates also the comparators' enable signals.

It works at 60 MHz.

## 9.5 PFC algorithm

The PFC operates based on a multi-mode scheme.

A constant on-time (COT) control is implemented; $T_{ON}$ is calculated from the PFC feedback and the measured Vin peak.

$T_{ON}$ is calculated and updated at the line cycle valley.

Based on the working PFC's operating state variables the working mode is changed to optimize the overall efficiency.

### 9.5.1 Ramp enhanced COT improved (patented)

The PFC control is based on the constant on-time scheme, with a proprietary improved algorithm: the calculated $T_{ON}$ is applied only after the PFC RECOT comparator is triggered to balance the recovery diode energy and the EMI capacitor current.

The PFC RECOT comparator threshold is adjusted by the core with a 6-bit DAC and allows to apply the programmed base and ramp (defined by user into NVM).

This feature allows improving the total harmonic distortion (THD) and the power factor (PF) of the application.

### 9.5.2 Operating modes

The PFC manager changes the operating modes by dynamically reconfiguring the SMEDs, obtaining optimal performances in term of both efficiency and THD/PF.

- Transition mode (TM mode)
- Valley skipping
- Discontinuous mode (DCM)

## 9.6 PFC protections

### 9.6.1 PFC OVP

In case the bulk voltage triggers the PFC OVP comparator, the system enters the fault state; the overvoltage protection can be programmed as latched or not latched.

The device implements also software overvoltage protection (SW OVP) that allows turning off the PFC until the next line valley in case the SW OVP threshold is reached. The SW OVP threshold is a NVM parameter.

### 9.6.2 PFC OCP2

If the PFC OC2 comparator is triggered, the PFC gate is truncated and remains off until the beginning of a new line half cycle. In case the PFC OC2 comparator is triggered for more than a programmable number of consecutives half line cycles the device enters the OCP2 fault and it is turned off.

The OCP2 fault can be programmed as latched or not latched.

### 9.6.3 Surge

When the surge comparator signal is high the PFC MOSFET is turned off and an interrupt is generated. The device will turn on the PFC MOSFET at the new line half cycle if the surge comparator output is low.

### 9.6.4 PFC soft-start timeout

If the PFC soft-start is not finished after 1 s the system enters the PFC soft-start timeout fault state and it is turned off. The fault is not latched.

### 9.6.5 PFC UVP

If the PFC_FB pin is below a threshold set by the user the device enters the PFC UVP fault and it is shut down. The system provides two different times of intervention configurable by NVM: adaptive and slow.

The slow intervention allows to shut off the system in case the UVP threshold is confirmed for at least 100 ms. The adaptive one allows to shut off the device immediately in case also the mains AC line is sensed below the brownout threshold for at least 1 half line cycle. On the contrary, the shut off will be delayed as if the intervention is set to slow, until the UVP and the mains conditions remain.

### 9.6.6 PFC_FB disconnection

If the PFC_FB is stuck low the system enters the PFC_FB disconnection fault state (latched) and it is turned off if the disconnection faults detection is enabled in NVM.

### 9.6.7 PFC_CS disconnection

If the PFC_CS pin is stuck low (or high) during the the PFC soft-start the system enters the PFC_CS disconnection fault state (latched) and it is shut down if the disconnection faults detection is enabled in NVM. In case the PFC_CS is stuck high during the operative mode the system enters the PFC_CS disconnection fault state and it is turned off if the disconnection faults detection is enabled in NVM.

### 9.6.8 PFC_ZCD disconnection

If the PFC_ZCD pin is stuck low or high during the the PFC soft-start the system enters the PFC_ZCD disconnection fault (latched) and it is turned off if the disconnection faults detection is enabled in NVM.

## 9.7 LLC control and fault management

### 9.7.1 LLC related resources

**Table 6. Pin**

| Pin name | Description | Level | Function |
|---|---|---|---|
| LLC_CS | Low-side current sense | 0 - 500 mV | 5-bit OLP |
| | | 700 mV | OCP2 fault |
| LLC_AUX | LLC auxiliary winding voltage sense | 0.9 V | External burst-mode |
| | | 2.5 V | LLC output OVP |
| LLC_FB | LLC OPTO feedback sense, burst comparator and SHUTDOWN comparator | ADC, 10 bits | Feedback sense |
| | | Programmable | Burst comparator |
| | | 125 mV | Shutdown comparator |
| HVG | High-side gate driving | - | - |
| LVG | Low-side gate driving | - | - |

### 9.7.2 LLC OC1 comparator

The LLC OC1 comparator implements the overload protection (OLP). It monitors the LLC_CS pin with respect to a programmable threshold. If the LLC_CS pin goes every cycle over the OC1 threshold for a programmable time, the IC shuts down and enters the OLP fault.

Both threshold and duration are programmable trough NVM parameters.

### 9.7.3 LLC OC2 comparator

The LLC OC2 comparator sets an HW limit for the current flowing into the LLC resonant tank: it triggers the OCP2 fault.

It monitors the LLC_CS pin with respect to a fixed 700 mV threshold. If this threshold is triggered for a programmable consecutive number of cycles, the OCP2 fault is triggered and the system shuts down.

### 9.7.4 LLC ZCD comparator

The LLC ZCD comparator detects the LLC current zero-crossing during the normal operation to implement the time-shift control and the anti capacitive protection.

Its output communicates to the LLC SMED.

The comparator's hysteresis is programmable by NVM choosing between the available values 5 mV or 10 mV.

### 9.7.5 LLC_FB voltage reading: OPTO feedback loop error

The LLC_FB pin is connected to the optocoupler and its voltage is the error signal of the LLC loop.

The LLC_FB voltage is sampled by the ADC to calculate the time-shift.

### 9.7.6 Shutdown feature

If the LLC_FB pin is forced below 125 mV, the device shuts down. If the voltage returns over such threshold the system restarts performing the soft-start.

This feature can be enabled / disabled using a NVM bit.

### 9.7.7 SMEDs

HVG and LVG are driven by an event driven 60 MHz state machine (2 coupled 4-state SMEDs).

Driving events are the ZCD event and the elapsing of the programmable time which sets the high-side and low-side time-shift values and drivers deadtime.

### 9.7.8 Algorithm

The LLC operation is based on "Symmetric Time-Shift Control" (STSC), an improved version of time-shift control that guarantees 50% of the HB duty cycle. The time-shift value is calculated from the LLC_FB pin.

### 9.7.9 Time-shift (patented)

The TSC methodology consists in controlling the amount of time elapsing from a zero-crossing of the tank current to the switch-off of the MOSFET currently on.

Conceptually, with TSC an inner loop is closed and the outer loop that regulates the output voltage provides the reference for the inner loop. This inner loop is completely managed by SMEDs using the zero current detection information.