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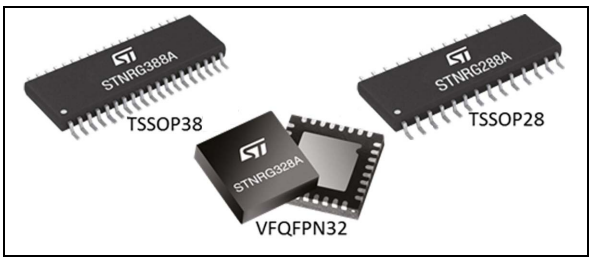
STNRGxxxA

Digital controller for power conversion applications with up to 6 programmable PWM generators, 96 MHz PLL

Datasheet - production data



Features

- Up to 6 programmable PWM generators (SMED - “State Machine Event Driven”)
  - 10 ns event detection and reaction
  - Max.1.3 ns PWM resolution
  - Single, coupled and two coupled operational modes
  - Up to 3 internal/external events per SMED
- 4 analog comparators
  - 4 internal 4-bit references
  - Up to 4 external references
  - Less than 50 ns propagation time
  - Continuous comparison cycle
  - Configurable hysteresis voltage levels
- ADCs (up to 8 channels)
  - 10-bit precision, with operational amplifier to extend resolution to 12-bit equivalent
  - Sequencer functionality
  - Input impedance: 1 MΩ
  - Configurable gain value: x1 and x4
- Integrated microcontroller
  - Advanced STM8® core with Harvard architecture and 3-stage pipeline
  - Max. f_{CPU}: 16 MHz
- Memories
  - Flash and E^{2}PROM with read while write (RWW) and error correction code (ECC)
  - Program memory: 32 Kbytes Flash; data retention 15 years at 85 °C after 10 kcycles at 25 °C
  - Data memory: 1 Kbyte true data E^{2}PROM; data retention:15 years at 85 °C after 100 kcycles at 85 °C
  - RAM: 6 Kbytes
- Clock management
  - Internal 96 MHz PLL
  - Low power oscillator circuit for external crystal resonator or direct clock input
  - Internal, user-trimmable 16 MHz RC and low power 153.6 kHz RC oscillators
  - Clock security system with clock monitor
- Basic peripherals
  - System, auxiliary and basic timers
  - IWDG/WWDG watchdog, AWU, ITC
- Reset and supply management
  - Multiple low power modes (wait, slow, auto-wakeup, Halt) with user definable clock gating
  - Low consumption power-on and power-down reset
- I/O
  - Multifunction bidirectional GPIO with highly robust design, immune against current injection
  - Fast digital input DIGIN, with configurable pull-up
- Communication interfaces
  - UART asynchronous with SW flow control and bootloader support
  - I^{2}C master/slave fast-slow speed rate
- Operating temperature: -40 °C up to 105 °C.

Table 1. Device summary

Part number	Package
STNRG388A	TSSOP38
STNRG328A	VFQFPN32
STNRG288A	TSSOP28

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1 Description

STNRG devices are a part of the STNRG family of STMicroelectronics® digital devices designed for advanced power conversion applications.

The STNRG improves the design of the successful STLUX™ family, now integrated in a wide range of LED driver architectures, to support industrial power conversion applications such as PFC+LLC, interleaved LC DC/DC, interleaved PFC for smart power supplies as well as the full bridge for pilot line drivers for electric vehicles.

2 STNRG family features list

All devices of the STNRG family provide the following features:

Table 2. STNRG family features list

Feature list		Device		
		STNRG388A	STNRG328A	STNRG288A
Package		TSSOP38	VFQFPN32	TSSOP28
Pin count		38	32	28
SMED numbers		6	6	6
SMED PWM output pins		6	5	4
Fast digital inputs pins		6	5(1)	3(2)
Positive comparator input pin		4	4	4(3)
Negative comparator input pins		3(4)	1	1(3)
Comparator hysteresis		Yes	Yes	Yes
Internal DACs		4	4	4
ADC input pins		8	6	6
ADC gain		x1 - x4	x1	x1
ADC hardware trigger		Yes	Yes	Yes
GPIO Port 0 pins		6	4	4
Communication	UART peripheral	Yes	Yes	Yes
	I^2C peripheral	Yes	Yes	Yes
	DALI peripheral	Yes	Yes	Yes
HSE function		Yes	Yes	Yes
Timers	System timer	1	1	1
	Auxiliary timer	1	1	1
	Basic timer	2	2	2
Auto-wakeup timer		1	1	1
Watchdog	Window watchdog timer	1	1	1
	Independent watchdog timer	1	1	1
Flash program memory		32 Kbytes	32 Kbytes	32 Kbytes
EEPROM data memory		1 Kbytes	1 Kbytes	1 Kbytes
RAM		6 Kbytes	6 Kbytes	6 Kbytes
SWIM pin		Mixed	Mixed	Mixed

1. DIGIN2 - DIGIN3 are connected to the same pin.
2. DIGIN0 - DIGIN1, DIGIN2 - DIGIN3 and DIGIN4 - DIGIN5 are connected to the same pin.
3. CPP2 and CPM3are connected to the same pin.
4. Some CPM pin is shared with other signals.

3 Introducing SMED

The heart of the STNRG controller family is the SMED (state machine event driven) technology which allows the device to pilot six independently configurable PWM clocks with a maximum resolution of 1.3 ns. A SMED is a powerful autonomous state machine, which is programmed to react to both external and internal events and may evolve without any software intervention. The SMED reaction time can be as low as 10.4 ns, giving the STNRG the ability of operating in time critical applications. The SMEDs offer superior performances when compared to traditional, timer based, PWM generators.

Each SMED is configured via the STNRG internal microcontroller. The integrated controller extends the STNRG reliability and guarantees more than 15 years of both operating lifetime and memory data retention for program and data memory after cycling.

A set of dedicated peripherals complete the STNRG device:

- 4 analog comparators with configurable references and 50 ns max. propagation delay. It is ideal to implement zero current detection algorithms or detect current peaks.
- 10-bit ADC with configurable op amp and 8-channel sequencer.
- 96 MHz PLL for high output signal resolution.

Documentation

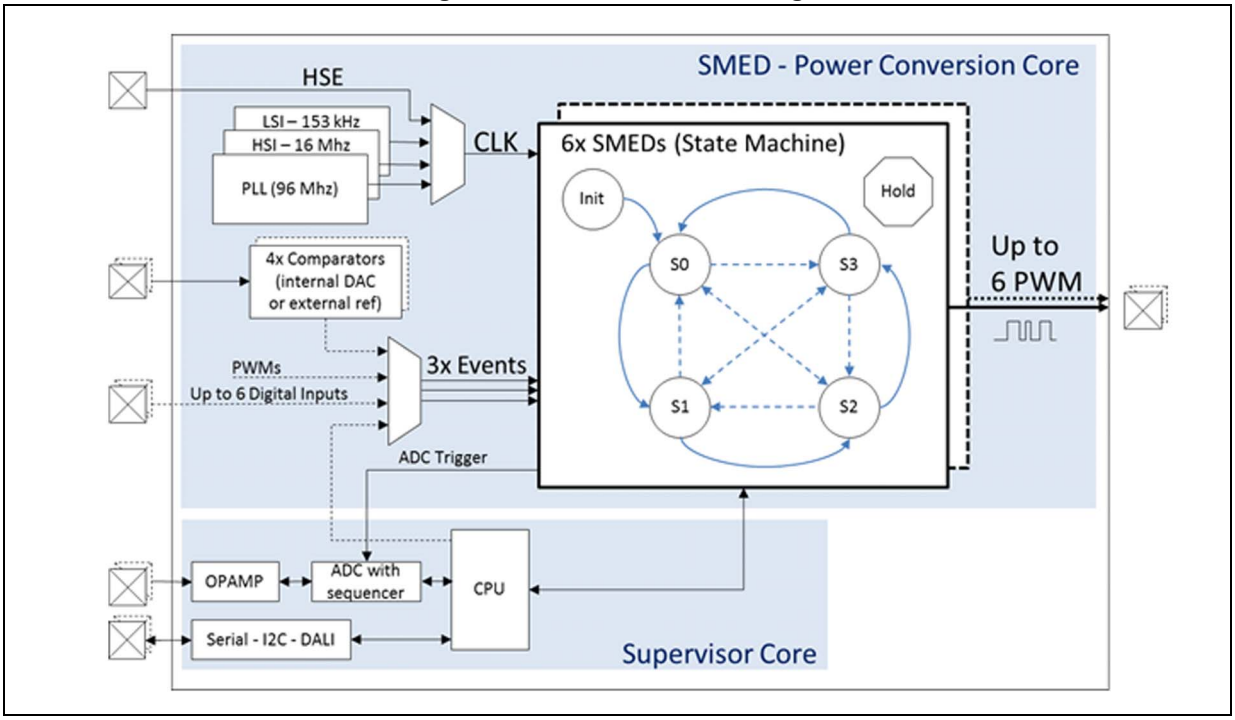
This datasheet contains the description of features, pinout, pin assignment, electrical characteristics, mechanical data and ordering information.

- For information on programming, erasing and protection of the internal Flash memory, please refer to the STM8S reference in the programming manual “How to program STM8S and STM8A Flash program memory and data EEPROM” (PM0051).
- For information on the debug and SWIM (single wire interface module) interface refer to the “STM8 SWIM communication protocol and debug module” user manual (UM0470).
- For information on the STM8 core, please refer to the “STM8 CPU programming manual” (PM0044).

4 System architecture

The STNRG device generates and controls PWM signals by means of a state machine, called SMED (state machine event driven). *Figure 1* gives an overview of the internal architecture.

Figure 1. STNRG internal design



The core of the device is the SMED unit: a hardware state machine driven by system events. The SMED includes 4 states (S0, S1, S2 and S3) available during running operations. A special HOLD state is provided as well. The SMED allows the user to configure, for every state, which system events will trigger a transaction to a new state. During a transaction from one state to the other, the PWM output signal level can be updated.

Once a SMED is configured and running, it becomes an autonomous unit, so no interaction is required since the SMED automatically reacts to system events.

Thanks to the SMED's 96 MHz operating frequency and their automatic dithering function, the PWM maximum resolution is 1.3 ns.

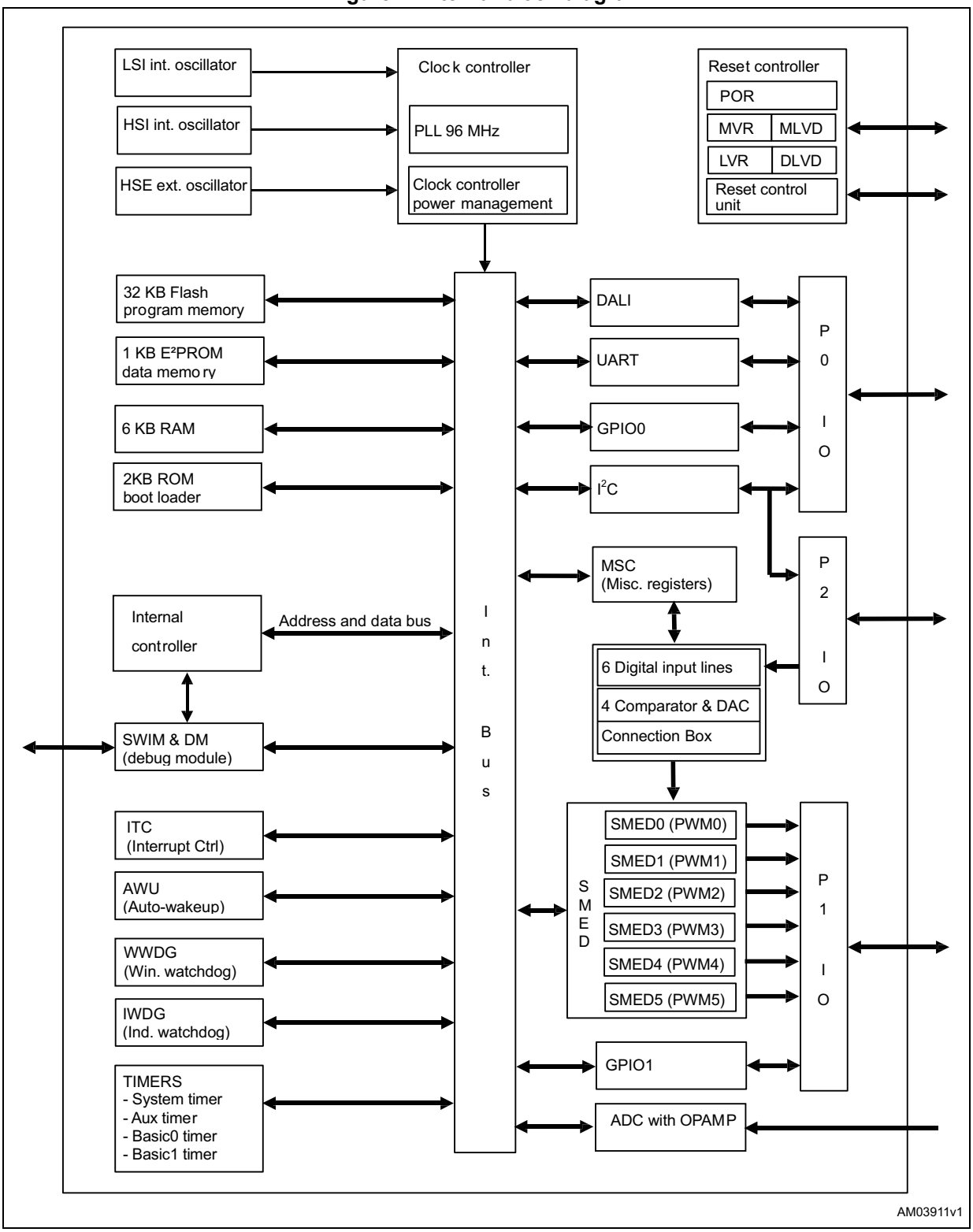
The STNRG family has 6 SMEDs available. Multiple SMEDs can operate independently from each other or they can be grouped together to form a more powerful state machine.

The STNRG also integrates a low power STM8 microcontroller which is used to configure and monitor the SMED activity and to supply external communication such as the UART, I^2C or DALI. The STM8 controller has full access to all the STNRG subsystems, including the SMEDs. The STNRG family also features a sequential ADC, which can be configured to continuously sample up to 8 channels.

Section : Block diagram illustrates the overall system block and shows how SMEDs have been implemented in the STNRG architecture.

Block diagram

Figure 2. Internal block diagram



5 Product overview

Section 5.1 describes the features implemented in the product device.

5.1 SMED (state machine event driven): configurable PWM generator

The SMED is an advanced programmable PWM generator signal. The SMED (state machine event driven) is a state machine device controllable by both external events (primary I/O signals) and internal events (counter timers), which generate an output signal (PWM) depending on the evolution of the internal state machine.

The PWM signal generated by the SMED is therefore shaped by external events and not only by a simple timer. This mechanism allows to generate controlled high frequency PWM signals.

The SMED is also autonomous: once it has been configured by the STNRG internal controller, the SMED can operate without any software interaction.

The STNRG family provides 6 SMED units. Multiple SMEDs can operate independently from each other or they can be grouped together to form a more powerful state machine.

The main features of a SMED are described here below:

- Configurable state machine generating a PWM signal
- More than 10.4 ns PWM native resolution
- Up to 1.3 ns PWM resolution when using SMED dithering
- 6 states available in each SMED: IDLE, S0, S1, S2, S3 plus a special HOLD state
- Transactions triggered by synchronous and asynchronous external events or an internal timer
- Each transaction can generate an interrupt
- Fifteen registers available to configure the state machine behavior
- Four 16-bit configurable time registers, one for each running state (T0, T1, T2, T3)
- Internal resources accessible through the processor interface
- Eight interrupt request lines
- Configurable ADC HW trigger request
- PWM pseudo open drain features configurable through GPIO1 registers

5.1.1 SMED coupling schemes

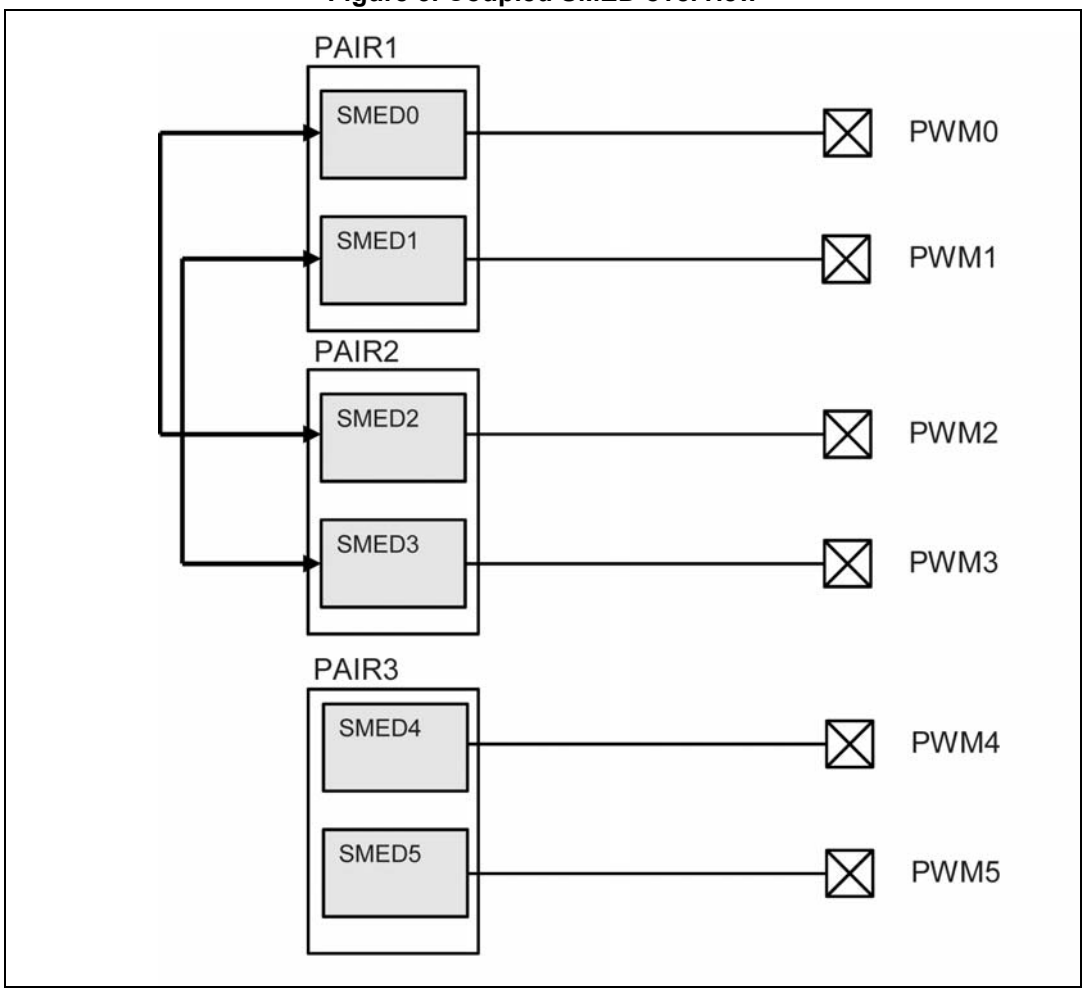
The SMED coupling extends the capability of the single SMED, preserving the independence of each “Finite State Machine” (FSM) programmed state evolution. The coupling scheme allows the SMED pulse signals to be interleaved on their own PWM or on a merged single PWM output. The STNRG supports the following coupled configuration schemes:

- Single SMED configuration
- Synchronous coupled SMED
- Asynchronous coupled SMED
- Synchronous two coupled SMEDs
- Asynchronous two coupled SMEDs
- External controlled SMED

The SMED units may be configured in different coupled schemes through the SMDx_GLBCONF and SMDx_DRVOUT bit fields of MSC_SMEDCFGxy registers.

An outline of the SMED subsystem is shown in *Figure 3*.

Figure 3. Coupled SMED overview



1. The PWM4 and PWM5 output pins are not present on all STNRG devices.

5.1.2 Connection matrix

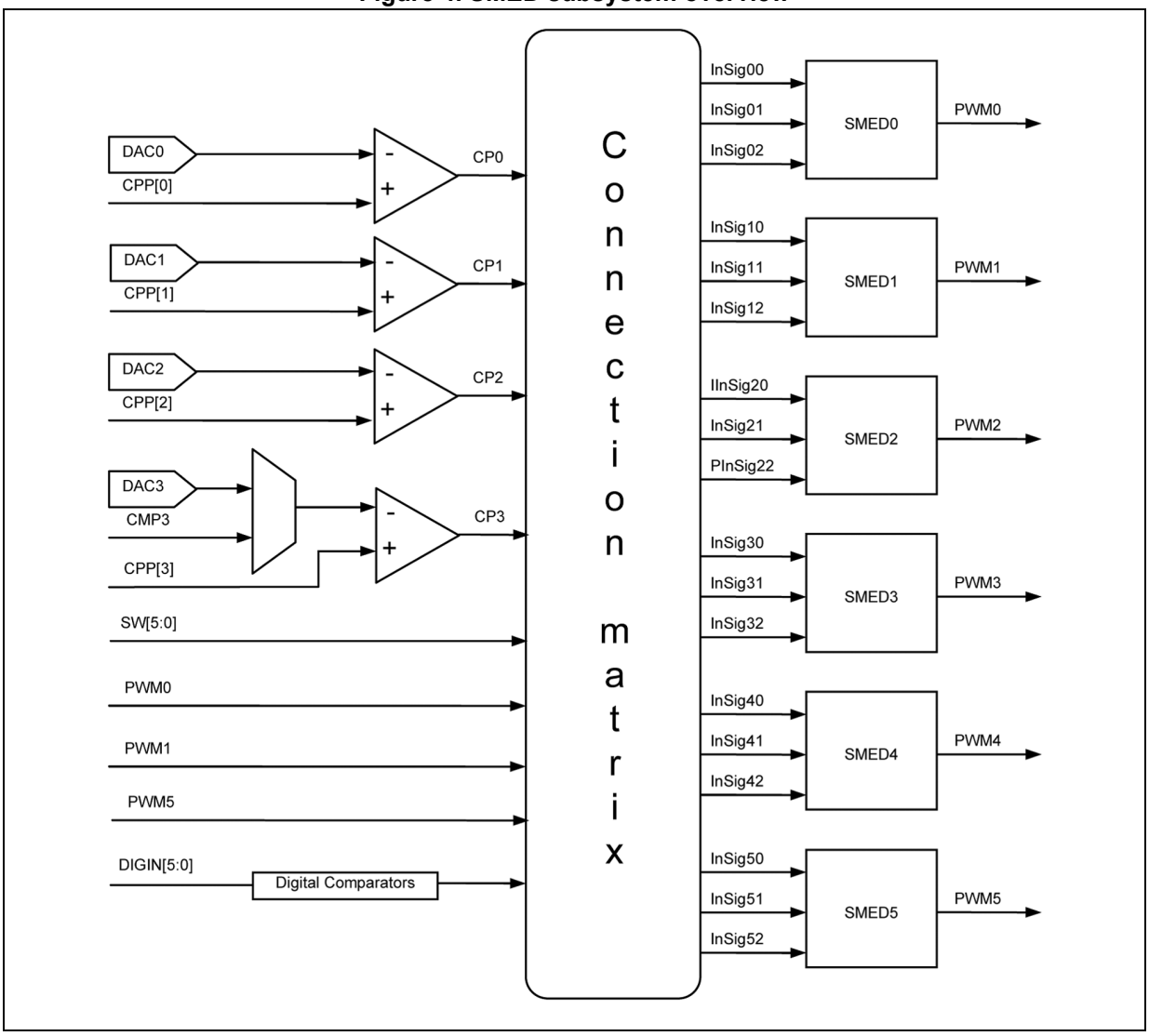
The connection matrix extends the input connectivity of each SMED unit so that a SMED can receive events from a wide range of sources. Through the matrix, it's possible to connect the SMED inputs to various signal families such as digital inputs, comparator output signals, SW events, and three PWM internal feedback signals as shown in *Figure 4*.

The list of the available event sources is the following:

- DIGIN [5:0] digital input lines
- CPM [3:0] analog comparator outputs
- PWM [5:0] output signals of SMEDs (only PWM 0, 1 and 5 are accessible)
- SW [5:0] software events

Figure 4 shows the connection matrix and signal interconnections as they are implemented in the STNRG family.

Figure 4. SMED subsystem overview



1. The CPP2 and CMP3 inputs are connected together in some STNRG devices.

Connection matrix interconnection

Every SMED unit has three input selection lines, one for each In_Sig input, configurable via the MSC_CBOXS (5:0) register. The selection lines choose the interconnection between one of possible four connection matrix signals for each SMED input event In_Sig (Y).

Table 3 shows the layout of the connection matrix interconnection signals as implemented in the STNRG family.

Table 3. Connection matrix interconnection

Conb_s(x)_(y)(z)					
SMED number	**SMED input**	**SMED input signal selection (z)**			
(x)	**(y)**	**00**	**01**	**10**	**11**
0	0	CP0	DIG0	DIG2	DIG5
	1	CP1	DIG0	DIG3	CP3
	2	CP2	DIG1	DIG4	SW0
1	0	CP1	DIG1	DIG3	DIG0
	1	CP2	DIG1	DIG4	CP3
	2	CP0	DIG2	DIG5	SW1
2	0	CP2	DIG2	DIG4	DIG1
	1	CP0	DIG2	DIG5	PWM0
	2	CP1	DIG3	DIG0	SW2
3	0	CP0	DIG3	DIG5	DIG2
	1	CP1	DIG3	DIG0	PWM1
	2	CP2	DIG4	DIG1	SW3
4	0	CP1	DIG4	DIG0	DIG3
	1	CP2	DIG4	DIG1	PWM5
	2	CP0	DIG5	DIG2	SW4
5	0	CP2	DIG5	DIG1	DIG4
	1	CP0	DIG5	DIG2	CP3
	2	CP1	DIG0	DIG3	SW5

Connection matrix legend:

- X represents the SMED [5:0] number
- Y represents the SMED input signal number (In_Sig [2:0])
- Z represents the In_Sig (Y) selection signal

Note: Each SMED input has independent connection matrix selection signals.
The DIG0 and DIG1 signal are interconnected together, the pin DIGIN [1_0] on the STNRG288A.
The DIG2 and DIG3 signals are interconnected together, the pin DIGIN [3_2] on the STNRG328A and STNRG288A.

The DIG4 and DIG5 signal are interconnected together, the pin DIGIN [5_4] on the STNRG288A.

5.2 Internal controller (CPU)

The STNRG family integrates a programmable STM8 controller acting as a device supervisor. The STM8 is a modern CISC core and has been designed for code efficiency and performance. It contains 21 internal registers (six of them directly addressable in each execution context), 20 addressing modes including indexed indirect and relative addressing and 80 instructions.

5.2.1 Architecture and registers

- Harvard architecture with 3-stage pipeline
- 32-bit wide program memory bus with single cycle fetching for most instructions
- X and Y 16-bit index registers, enabling indexed addressing modes with or without offset and read-modify-write type data manipulations
- 8-bit accumulator
- 24-bit program counter with 16 Mbyte linear memory space
- 16-bit stack pointer with access to a 64-Kbyte stack
- 8-bit condition code register with seven condition flags updated with the results of last executed instruction

5.2.2 Addressing

- 20 addressing modes
- Indexed indirect addressing mode for lookup tables located in the entire address space
- Stack pointer relative addressing mode for efficient implementation of local variables and parameter passing

5.2.3 Instruction set

- 80 instructions with 2-byte average instruction size
- Standard data movement and logic/arithmetic functions
- 8-bit by 8-bit multiplication
- 16-bit by 8-bit and 16-bit by 16-bit division
- Bit manipulation
- Data transfer between stack and accumulator (push/pop) with direct stack access
- Data transfer using the X and Y registers or direct memory-to-memory transfers

5.2.4 Single wire interface module (SWIM)

The single wire interface module (SWIM), together with the integrated debug module (DM), allows non-intrusive, real-time in-circuit debugging and fast memory programming. The interface can be activated in all device operation modes and can be connected to a running device (hot plugging).The maximum data transmission speed is 145 byte/ms.

The SWIM pin is a multifunction signal. For further details refer to *Table 7: Port P1 I/O multiplexing signal* in *Section 7.3 on page 40*.

5.2.5 Debug module

The non-intrusive debugging module is fully controllable through the external target emulator. Besides memory and peripheral operation, the CPU operation can also be monitored in real-time by means of shadow registers.

- R/W of RAM and peripheral registers in real-time
- R/W for all resources when the application is stopped
- Breakpoints on all program-memory instructions (software breakpoints), except for the interrupt vector table
- Two advanced breakpoints and 23 predefined breakpoint configurations

5.3 Basic peripherals

Section 5.3.1 and *Section 5.3.2* describe the basic peripherals accessed by the internal CPU controller.

5.3.1 Vectored interrupt controller

- Nested interrupts with three software priority levels
- 21 interrupt vectors with hardware priority
- Two vectors for 12 external maskable or un-maskable interrupt request lines
- Trap and reset interrupts

5.3.2 Timers

The STNRG family provides several timers which are used by software and do not interact directly with the SMED and the PWM generation.

System timers

The system timer consists of a 16-bit autoreload counter driven by a programmable prescaled clock and operating in one shoot or free running operating mode. The timer is used to provide the IC time base system clock, with an interrupt generation on timer overflow events.

Basic timers

The IC device includes two independent 6-bit timers programmable through the miscellaneous indirect register area. The time base frequency is configurable with different source clocks.

The timers have the following functionalities:

- Free running mode
- Timer prescaler 8-bits
- Counter register 6-bits
- Programmable time base clock (HSI, HSE, LSI, PLL)
- Interrupt timer capability:
  - Vectored interrupt
  - Interrupt IRQ/NMI or polling mode

Auxiliary timer

The auxiliary timer is a light timer with elementary functionality. The time base frequency is provided by the CCO clock logic (configurable with a different source clock and prescale division factors), while the interrupt functionality is supplied by an interrupt edge detection logic similarly to the solution adopted for the Port P0/P2.

The timer has the following main features:

- Free running mode
- Up counter
- Timer prescaler 8-bit
- Interrupt timer capability:
  - Vectored interrupt
  - Interrupt IRQ/NMI or Polling mode
- Timer pulse configurable as a clock output signal via the CCO primary pin

Thanks to the great configurability of the CCO frequency, the timer can cover a wide range of interval time to fit better the target application requirements.

Auto-wakeup timer

The AWU timer is used to cyclically wake-up the IC device from the active halt state. The AWU frequency time base f_{AWU} can be selected between the following clock sources: LSI (153.6 kHz) and the external clock HSE scaled down to 128 kHz clock.

By default the f_{AWU} clock is provided by the LSI internal source clock.

Watchdog timers

The watchdog system is based on two independent timers providing a high level of robustness to the applications. The watchdog timer activity is controlled by the application program or by suitable option bytes. Once the watchdog is activated, it cannot be disabled by the user program without going through reset.

Window watchdog timer

The window watchdog is used to detect the occurrence of a software fault, usually generated by external interferences or by unexpected logical conditions, which causes the application program to break the normal operating sequence.

The window function can be used to adjust the watchdog intervention period in order to match the application timing perfectly. The application software must refresh the counter before timeout and during a limited time window. If the counter is refreshed outside this time window, a reset is issued.

Independent watchdog timer

The independent watchdog peripheral can be used to solve malfunctions due to hardware or software failures.

It is clocked by the 153.6 kHz LSI internal RC clock source. By properly setting the hardware watchdog feature associated option bits, the watchdog is automatically enabled at power-on, and generates a reset unless the key register is written by software before the counter reaches the end of the count.

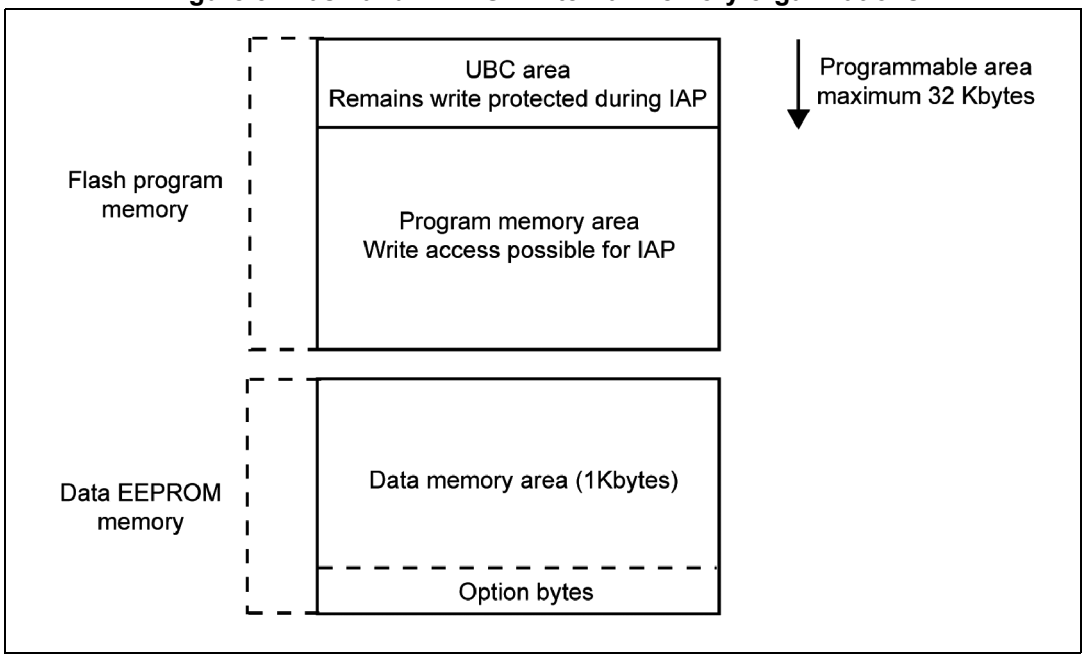
5.3.3 Flash program and data E^{2}PROM

Embedded Flash and E^{2}PROM with the memory ECC code correction and protection mechanism preventing embedded program hacking.

- 32 Kbyte of single voltage program Flash memory
- 1 Kbyte true (not emulated) data E^{2}PROM
- Read while write: writing in the data memory is possible while executing code program memory
- The device setup is stored in a user option area in the non-volatile memory.

5.3.4 Architecture

Figure 5. Flash and E^{2}PROM internal memory organizations



- The memory is organized in blocks of 128 bytes each
- Read granularity: 1 word = 4 bytes
- Write/erase granularity: 1 word (4 bytes) or 1 block (128 bytes) in parallel
- Writing, erasing, word and block management is handled automatically by the memory interface.

5.3.5 Write protection (WP)

Write protection in application mode is intended to avoid unintentional overwriting of the memory. The write protection can be removed temporarily by executing a specific sequence in the user software.

5.3.6 Protection of user boot code (UBC)

In STNRG devices a memory area of 32 Kbyte can be protected from overwriting at a user option level. In addition to the standard write protection, the UBC protection can be modified by the embedded program or via debug interface when the ROP protection is enabled.

The UBC memory area contains the reset and interrupt vectors and its size can be adjusted in increments of 512 bytes by programming the UBC and nUBC option bytes.

Note: If users choose to update the boot code in the application programming (IAP), this has to be protected so to prevent unwanted modification.

5.3.7 Read-out protection (ROP)

The STNRG family provides a read-out protection of the code and data memory which can be activated by an option byte setting.

The read-out protection prevents reading and writing program memory, data memory and option bytes via the debug module and SWIM interface. This protection is active in all device operation modes. Any attempt to remove the protection by overwriting the ROP option byte triggers a global erase of the program and data memory contents.

5.4 Clock controller

The clock controller distributes the system clock provided by different oscillators to the core and the peripherals. It also manages clock gating for low- power modes and ensures clock robustness.

The main clock controller features are:

- Clock sources
- Internal 16 MHz and 153.6 kHz RC oscillators
- External source clock:
  - Crystal/resonator oscillator
  - External clock input
- Internal PLL at 96 MHz (not used as the f_{MASTER} source clock)
- Reset: after the reset the microcontroller restarts by default with the HSI internal clock scaled at 2 MHz (16 MHz/8). The clock source and speed can be changed by the application program as soon as the code execution starts.
- Safe clock switching: clock sources can be changed safely on the fly in run mode through a configuration register. The clock signal is not switched until the new clock source is ready. The design guarantees glitch-free switching.
- Clock management: to reduce power consumption, the clock controller can stop the clock to the core or individual peripherals.
- Wakeup: In in case the device wakes up from low- power modes, the internal RC oscillator (16 MHz/8) is used for a quick startup. After a stabilization time, the device brings back the clock source that was selected before Halt mode was entered.
- Clock security system (CSS): the CSS permits monitoring of external clock sources and automatic switching to the internal RC (16 MHz/8) in case of a clock failure.
- Configurable main clock output (CCO): this feature permits to output an internal clock source signal for application usage.

5.4.1 Internal 16 MHz RC oscillator (HSI)

The high speed internal (HSI) clock is the default master clock line, generated by an internal RC oscillator and with nominal frequency of 16 MHz. It has the following major features:

- RC architecture
- Glitch-free oscillation
- 3-bit user calibration circuit.

5.4.2 Internal 153.6 kHz RC oscillator (LSI)

The low speed internal (LSI) clock is a low speed clock line provided by an internal RC circuit. It drives both the independent watchdog (IWDG) circuit and the auto-wakeup unit (AWU). It can also be used as a low power clock line for the master clock f_{MASTER}.

5.4.3 Internal 96 MHz PLL

The PLL provides a high frequency 96 MHz clock used to generate high frequency and accurate PWM waveforms. The input reference clock must be 16 MHz and may be sourced either by the internal HSI signal or by the external HSE auxiliary input crystal oscillator line.

The internal PLL prescaled clock cannot be selected as f_{MASTER}.

Note: When the application requires a PWM signal with a custom defined long term stability it is suggested to use an external clock source connected to the HSE auxiliary clock line as the PLL input reference clock. In this case, the external clock source accuracy determines the PWM output stability.

5.4.4 External clock input/crystal oscillator (HSE)

The high speed external clock (HSE) allows the connection of an external clock generated, for example, by a highly accurate crystal oscillator. The HSE is interconnected with the f_{MASTER} clock line and to several peripherals. It allows users to provide a custom clock characterized by a high level of precision and stability to meet the application requirements. The HSE supports two possible external clock sources with a maximum of 24 MHz:

- Crystal/ceramic resonator interconnected with the HseOscin/HseOscout signals
- Direct drive clock interconnected with the HseOscin signal

The HseOscin and HseOscout signals are multifunction pins configurable through the I/O multiplex mechanism; for further information refer to Section 6 on page 30.

Note: When the HSE is configured as the f_{MASTER} source clock, the HSE input frequency cannot be higher than 16 MHz.
When the HSE is the PLL input reference clock, then the HSE input frequency must be equal to 16 MHz.
If the HSE is the reference for the SMED or the ADC logic, the input frequency can be configured up to 24 MHz.