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STP1612PW05

16-channel LED driver with 16-bit PWM, 8-bit gain and full LED error detection

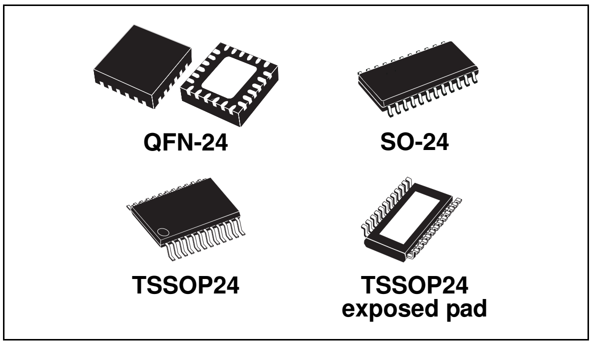
Preliminary data

Features

- 16 constant current output channels
- Supply voltage: 3.3 V or 5 V
- Two PWM selectable counters 12/16-bit of grayscale
- Selectable enhanced PWM for ghost effect reduction
- Open and short LED detection
- 8-bit current gain control by means of 256 steps in two selectable ranges
- Single resistor to set the current from 3 mA to 60 mA
- Programmable progressive output delay
- Thermal protection and thermal flag
- UVLO
- Schmitt trigger input
- Selectable 16-bit or 256-bit serial data-in format
- Max clock frequency: 30 MHz
- ESD protection 2.5 kV HBM, 200 V MM
- Drop-in compatible with STP16CP\S\DP05 series
- Available in high thermal efficiency TSSOP exposed pad

Applications

- Video display LED panels
- RGB backlighting
- Special lighting



Description

The STP1612PW05 is a 16-channel constant current sink LED driver. The maximum output current value for all the 16 channels is set by a single resistor from 3 mA to 60 mA. The device features 8-bit gain (256 steps) for global LED brightness adjustment with two selectable ranges. This function is accessible via a serial interface. The device has an individual adjustable PWM brightness control for each output channel. The PWM counters are selectable via a serial interface with 4096 or 65536 steps (12 or 16 bit). The STP1612PW05 also provides enhanced pulse-width modulation counting algorithms called e-PWM to reduce flickering effects (ghost visual effects) improving the overall image quality. The device has a dual size 16-bit or 256-bit shift register. All the control and the shift register read back data are accessible via serial interface. The STP1612PW05 has the capability to detect open and short LED failure and overtemperature, reporting the status through SPI line. The device guarantees a 20 V output driving capability, allowing the user to connect more LEDs in series.

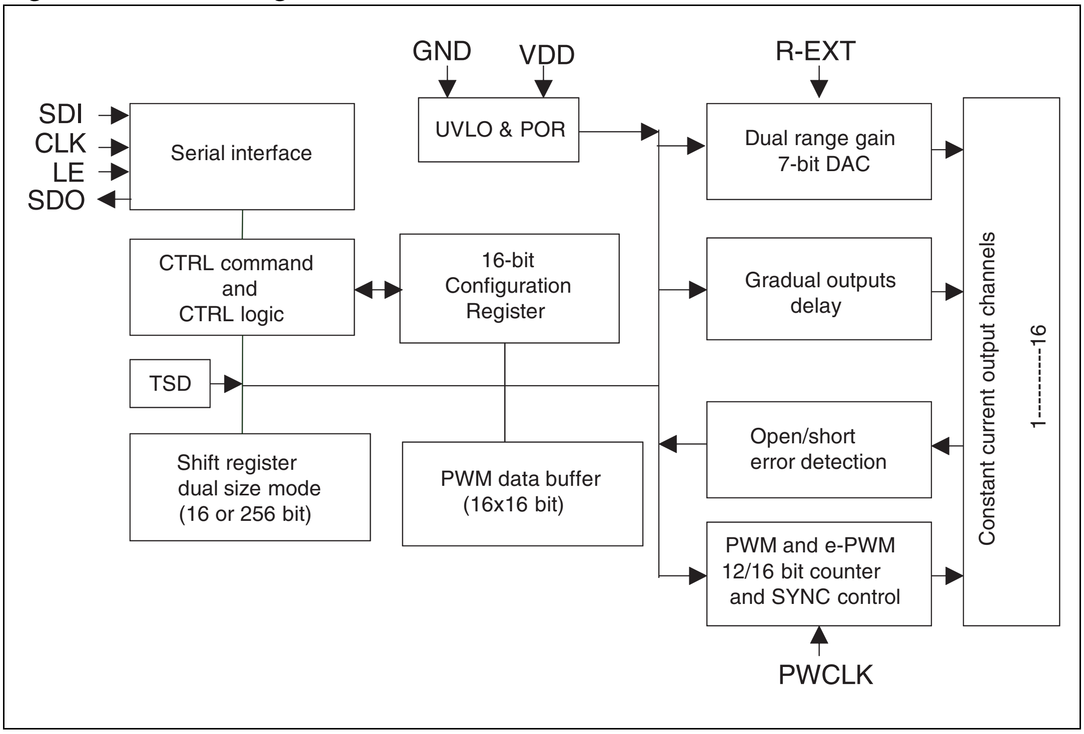
Table 1. Device summary

Order code	Package	Packaging
STP1612PW05QTR	QFN-24	4000 parts per reel
STP1612PW05MTR	SO-24	1000 parts per reel
STP1612PW05TTR	TSSOP24	2500 parts per reel
STP1612PW05XTTR	TSSOP24 exposed pad	2500 parts per reel

Contents

1 Block diagram

Figure 1. Block diagram



2 Summary description

Table 2. Typical current accuracy at 5 V

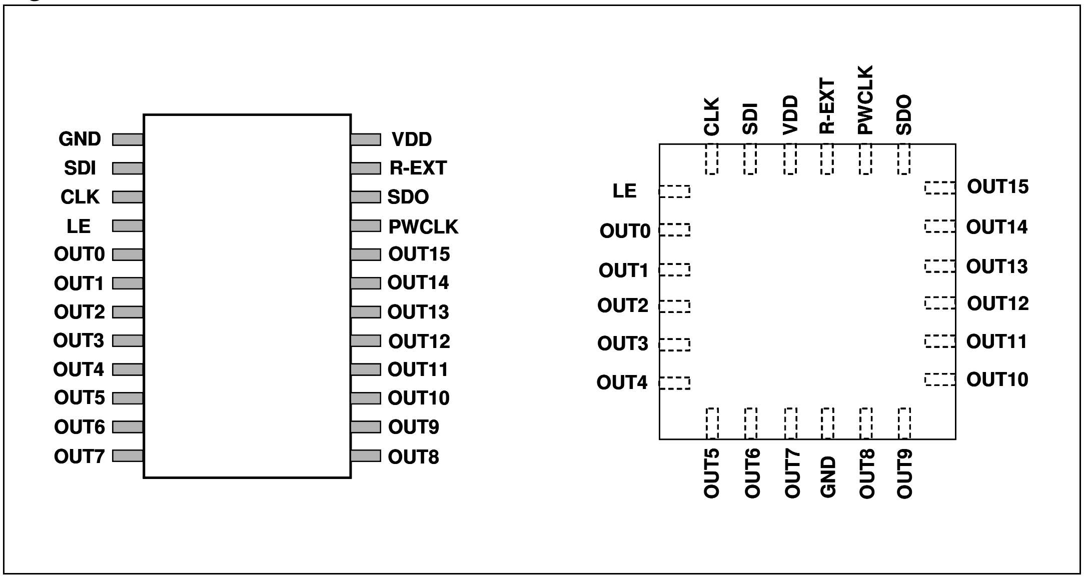
Output voltage	Current accuracy Between ICs	Output current	V_{DD}	temp.
≥ 1.0	± 6%	15 to 60	5 V	25 °C
≥ 0,2	± 6%	3 to 15		

Table 3. Typical current accuracy at 3.3 V

Output voltage	Current accuracy Between ICs	Output current	V_{DD}	temp.
≥ 1.0	± 6%	15 to 60	3.3 V	25 °C
≥ 0,3	± 6%	3 to 15		

2.1 Pin connection and description

Figure 2. Pin connection



Note: The exposed pad should be electrically connected to a metal land electrically isolated or connected to ground

Table 4. Pin description

Pin n°	Symbol	Name and function
1	GND	Ground terminal
2	SDI	Serial data input terminal
3	CLK	Clock input terminal used to shift data on rising edge and carries command information when LE is asserted.
4	LE	Data strobe terminal and controlling command with CLK
5-20	OUT 0-15	Output terminals
21	PWCLK	Gray scale clock terminal. Reference clock for grey scale PWM counter.
22	SDO	Serial data out terminal
23	R-EXT	Input terminal of an external resistor for constant current programing
24	V_{DD}	Supply voltage terminal

3 Electrical ratings

3.1 Absolute maximum ratings

Stressing the device above the rating listed in the *Table 5* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 5. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage	0 to 7	V
V_O	Output voltage	-0.5 to 20	V
I_O	Output current	60	mA
V_I	Input voltage	-0.4 to V_{DD}	V
I_{GND}	GND terminal current	1300	mA
f_{CLK}	Clock frequency	50	MHz
T_J	Junction temperature range (1)	-40 to + 170	°C

1. Such absolute value is based on the thermal shutdown protection.

3.2 Thermal data

Table 6. Thermal data

Symbol	Parameter		Value	Unit
T_A	Operating free-air temperature range		-40 to +125	°C
$T_{J\text{-}OPR}$	Operating thermal junction temperature range		-40 to +150	°C
T_{STG}	Storage temperature range		-55 to +150	°C
R_{thJA}	Thermal resistance junction-ambient (1)	SO-24	42.7	°C/W
		TSSOP24	55	°C/W
		TSSOP24(2) Exposed pad	37.5	°C/W
		QFN-24	55	°C/W

1. According to Jedec standard 51-7B
2. The exposed pad should be soldered directly to the PCB to realize the thermal benefits.

3.3 Recommended operating conditions

Table 7. Recommended operating conditions at 25 °C

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage		3.0	-	5.5	V
V_O	Output voltage			-	20	V
I_O	Output current, OUTn		3	-	60	mA
$I_{OH,SDO}$	Output current, SDO			-	+1	mA
$I_{OL,SDO}$	Output current, SDO			-	-1	mA
V_{IH}	Input voltage		0.7 V_{DD}	-	V_{DD}	V
V_{IL}	Input voltage		GND	-	0.3 V_{DD}	V
t_{wLAT}	LE pulse width	V_{DD} = 3.3 V to 5.0 V	20	-		ns
t_{wCLK}	CLK pulse width		10	-		ns
t_{wEN}	PWCLK pulse width		20	-		ns
$t_{SETUP(D)}$	Setup time for DATA		5	-		ns
$t_{HOLD(D)}$	Hold time for DATA		5	-		ns
$t_{SETUP(L)}$	Setup time for LATCH		5	-		ns
f_{CLK}	Clock frequency	Cascade operation (1)		-	30	MHz

1. If the device is connected in cascade, it may not be possible achieve the maximum data transfer. Please considered the timings carefully.

4 Electrical characteristics

V_{DD} = 3.3 V ± 10%, V_{DD} = 5 V ± 10%, T_A = 25 °C unless otherwise specified

Table 8. Electrical characteristics

Symbol	Characteristics		Test conditions	Min.	Typ.	Max.	Unit
V_O	Maximum output voltage		$\overline{OUT0}$ ~ $\overline{OUT15}$			20	V
I_{OUT}	Output current	OUT0~OUT115	V_O = 2V	3		60	mA
$I_{OH,SDO}$		SDO				-8	
$I_{OL,SDO}$		SDO				8	
V_{IH}	Input voltage “H” level			0.7 * V_{DD}		V_{DD}	V
V_{IL}	Input voltage “L” level			GND		0.3 * V_{DD}	V
I_{OH}	Output leakage current		V_O = 20 V			1	µA
V_{OL}	Output voltage SDO		I_{OL} = +8 mA			0.4	V
V_{OH}			I_{OH} = -8 mA	V_{DD} - 0.4			V
dI_{OUT1}	Current skew (channel)		I_{OUT} = 3mA, V_O = 0.3V, R_{EXT} = 238.2kΩ		±1.5	±3	%
dI_{OUT1}			I_{OUT} = 20mA, V_O = 1V, R_{EXT} = 34.7kΩ				
dI_{OUT2}	Current skew (IC)		I_{OUT} = 3mA, V_O = 0.3V, R_{EXT} = 238.2kΩ		±3	±6	%
dI_{OUT2}			I_{OUT} = 20mA, V_O = 1V, R_{EXT} = 34.7kΩ				
%/dV_O	Output current vs. output voltage regulation		V_O within 1.0 V and 3.0 V, R_{ext} = 34.7 kΩ @ 20 mA		± 0.1	± 0.5	% / V
%/dV_{DD}	Output current vs. supply voltage regulation		V_{DD} within 4.5 V and 5.5 V		± 1.0	± 5.0	% / V
$R_{IN(down)}$	Pull-down resistor		LE	150	200	250	kΩ
$I_{DD(off)\,1}$	Supply current “Off”		R_{ext} = Open, $\overline{OUT0}$ ~ $\overline{OUT15}$ = Off		8	11	mA
$I_{DD(off)\,2}$			I_O = 3 mA, $\overline{OUT0}$ ~ $\overline{OUT15}$ = Off		8.5	11	
$I_{DD(off)\,3}$			I_O = 60 mA, $\overline{OUT0}$ ~ $\overline{OUT15}$ = Off		11	15	
$I_{DD(on)\,1}$	Supply current “On”		I_O = 3 mA, $\overline{OUT0}$ ~ $\overline{OUT15}$ = On		8	11.5	
$I_{DD(on)\,2}$			I_O = 60 mA, $\overline{OUT0}$ ~ $\overline{OUT15}$ = On		11.5	15	

Figure 3. Test circuit for electrical characteristics

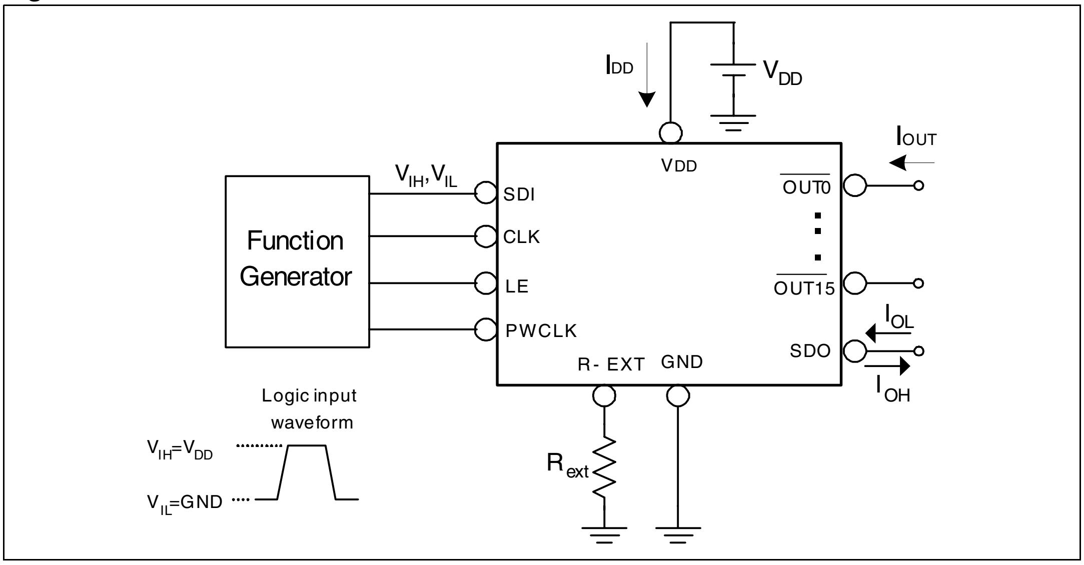


Table 9. Switching characteristics (V_{DD} = 5.0 V) T_A = -40 ~ 125 °C

Symbol	Characteristics	Conditions		Min.	Typ.	Max.	Unit
t_{SU0}	Setup time	SDI - CLK ↑	V_{DD} = 5.0 V V_{IH} = V_{DD} V_{IL} = GND R_{ext} = 460 Ω V_{LED} = 4.5 V R_L = 152 Ω CL = 10 pF C1 = 100 nF C2 = 10 µF I_O = 20 mA	1			ns
t_{SU1}		LE ↑ – DCLK ↑		1			ns
t_{SU2}		LE ↓– DCLK ↑		5			ns
t_{H0}	Hold time	CLK ↑ - SDI		3			ns
t_{H1}		CLK ↑ - LE ↓		7			ns
t_{PD0}	Propagation delay time	CLK - SDO			30	40	ns
t_{PD1}		PWCLK-$\overline{\text{OUTn4}}$ (1)			100		ns
t_{PD2}		LE – SDO(2)			30	40	ns
t_{DL1}	Stagger delay time	$\overline{\text{OUTn4}}$ + 1 (1)			40		ns
t_{DL2}		$\overline{\text{OUTn4}}$ + 2 (1)			80		ns
t_{DL3}		$\overline{\text{OUTn4}}$ +3 (1)			120		ns
$t_{w(L)}$	Pulse width	LE		5			ns
$t_{w(CLK)}$		CLK		20			ns
$t_{w(PWCLK)}$		PWCLK		20			ns
t_{ON}	Output rise time of output ports				10		ns
t_{OFF}	Output fall time of output ports				6		ns
t_{EDD}	Error detection minimum duration (3)				1		µs

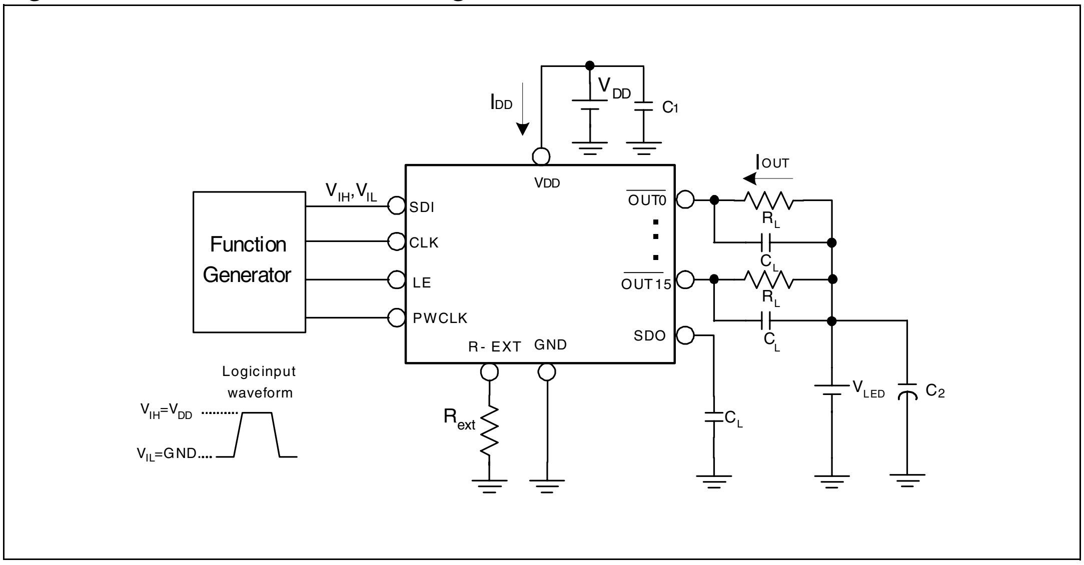
1. Refer to the timing waveform, where n = 0, 1, 2, 3.
2. In timing of “read configuration” and “read error status code”, the next CLK rising edge should be t_{PD2} after the falling edge of LE.
3. Refer to Figure 5 on page 13.

Table 10. Switching characteristics (V_{DD} = 3.3 V)

Symbol	Characteristics	Conditions		Min.	Typ.	Max.	Unit
t_{SU0}	Setup time	SDI - DCLK ↑	V_{DD} = 3.3 V V_{IH} = V_{DD} V_{IL} = GND R_{ext} = 460 Ω V_{LED} = 4.5 V R_L = 152 Ω CL = 10 pF C1 = 100 nF C2 = 10 µF	1			ns
t_{SU1}		LE ↑ – DCLK ↑		1			ns
t_{SU2}		LE ↓– DCLK ↑		5			ns
t_{H0}	Hold time	CLK ↑ - SDI		3			ns
t_{H1}		CLK ↑ - LE ↓		7			ns
t_{PD0}	Propagation delay time	CLK - SDO			45	40	ns
t_{PD1}		PWCLK-$\overline{\text{OUTn4}}$(1)			120		ns
t_{PD2}		LE – SDO(2)			45	40	ns
t_{DL1}	Stagger delay time	$\overline{\text{OUTn4}}$ + 1 (1)			40		ns
t_{DL2}		$\overline{\text{OUTn4}}$ + 2 (1)			80		ns
t_{DL3}		$\overline{\text{OUTn4}}$ +3 (1)			120		ns
$t_{w(L)}$	Pulse width	LE		5			ns
$t_{w(CLK)}$		CLK		20			ns
$t_{w(PWCLK)}$		PWCLK		20			ns
t_{ON}	Output rise time of output ports				11.6		ns
t_{OFF}	Output fall time of output ports				7		ns
t_{DEC}	Error detection duration				0.5	1	µs

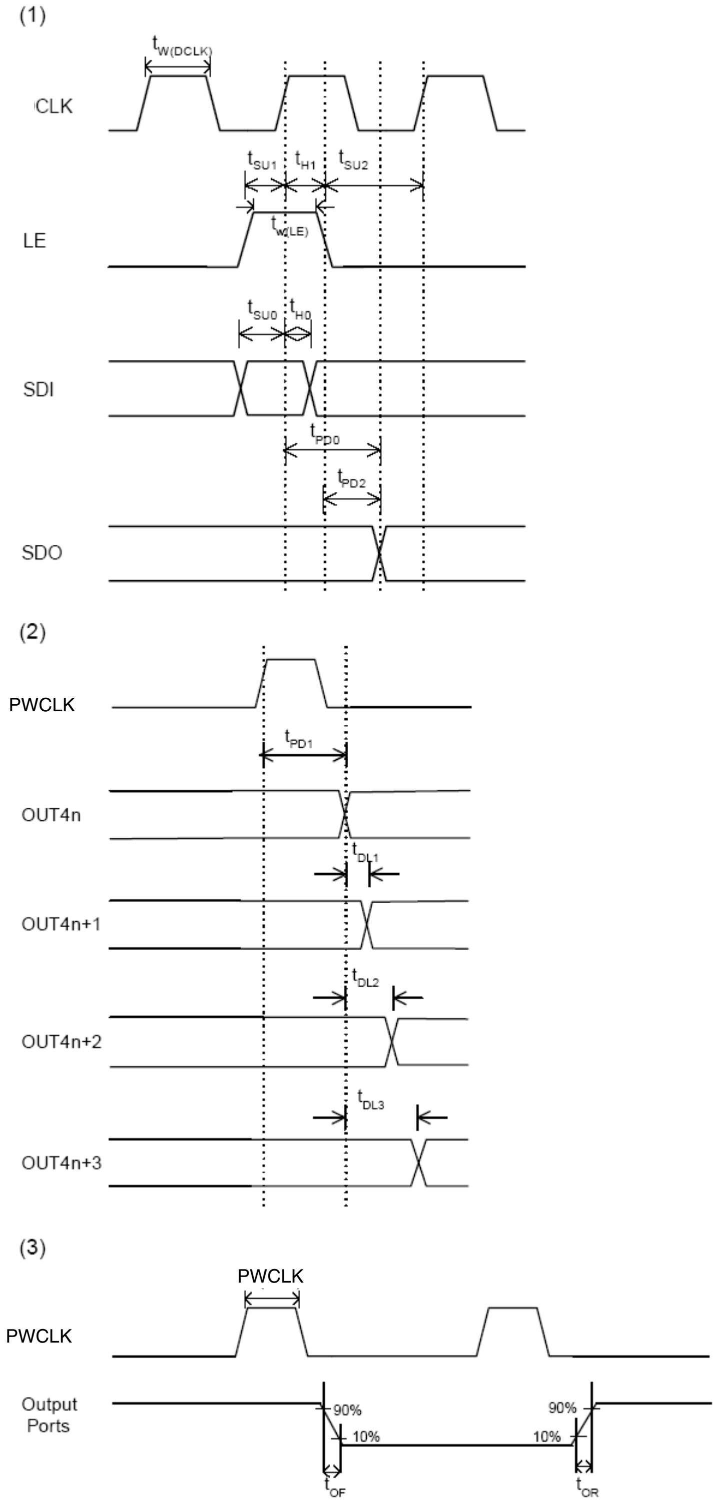
1. Refer to the timing waveform *Figure 4*, where n = 0, 1, 2, 3.
2. In timing of “read configuration” and “read error status code”, the next CLK rising edge should be t_{PD2} after the falling edge of LE.

Figure 4. Test circuit for switching characteristics



5 Timing waveform

Figure 5. Timing waveform

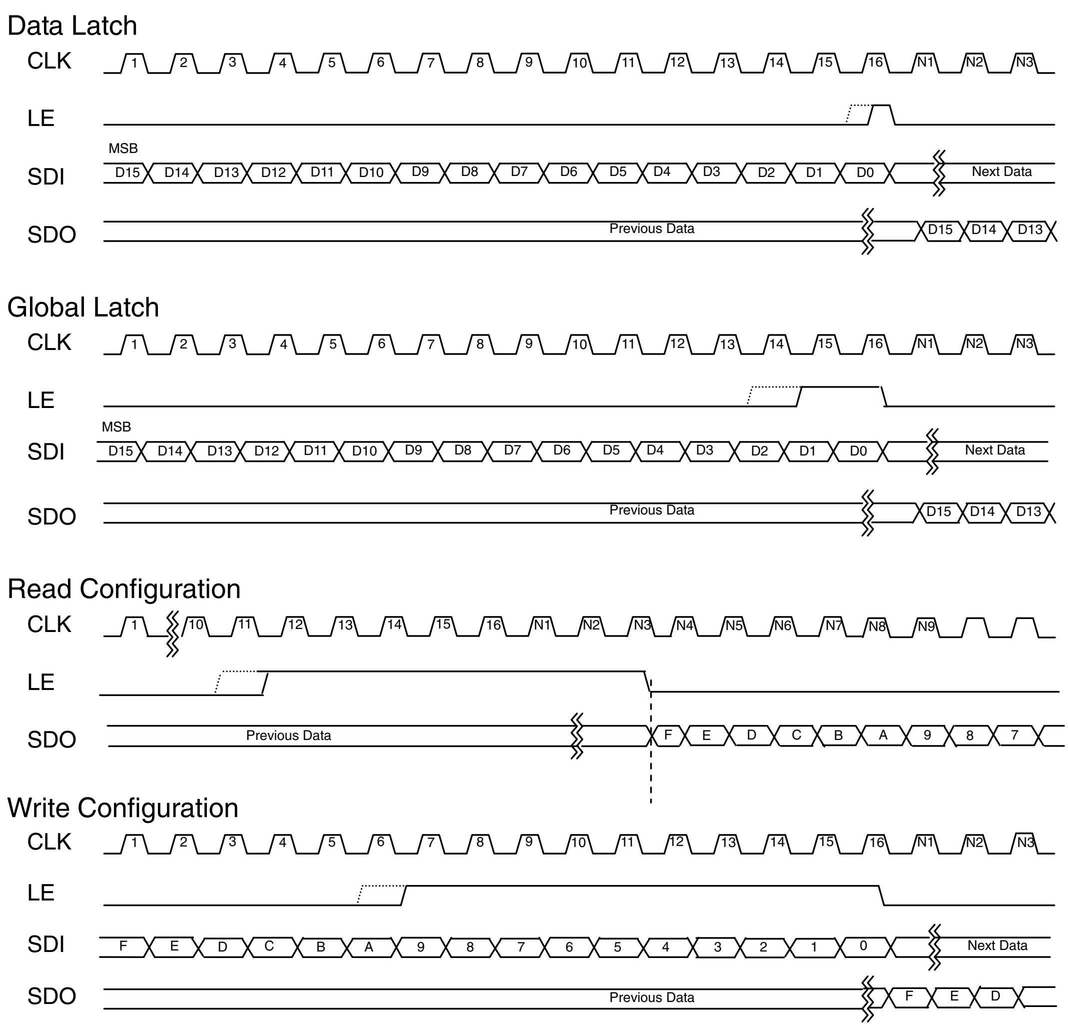


6 Principle of operation

Table 11. Control command

	Signals combination		Description
Command name	LE	Number of CLK rising edge when LE is asserted	The action after a falling edge of LE
Data latch	High	1	Serial data are transferred to the buffers
Global latch	High	2 or 3	Buffer data are transferred to the comparators
Read configuration	High	4 or 5	Move out “configuration register” to the shift register
Enable “error detection”	High	6 or 7	Detect the status of each output’s LED
Read “error status code”	High	8 or 9	Move out “error status code” of 16 outputs to the shift registers
Write configuration	High	10 or 11	Serial data are transferred to the “configuration register”
Reset to 16-bit shift register length	High	12 or 13	Set to 16-bit the shift register length

Figure 6. Timing diagram



7 Configuration register

Table 12. Configuration register

Bit	Attribute	Definition	Value	Function	Default value
15	Read/Write	Shift register length	0	16 bit shift register	0
			1	256 bit shift register	
14	Read	Thermal error flag	0	Temperature OK	0
			1	Over temperature (>150°C typ.)	
13	Read/Write	PWM counter (12/16 bit)	0	12 bit Grayscale PWM counter	0
			1	16 bit Grayscale PWM counter	
12-11	Read/Write	PWM counting mode selection	00	64 times of MSB[1] 6-bit PWM counting plus once of LSB[1] 6-bit PWM	11
			01	16 times of MSB 6-bit PWM counting by 1/4 PWCLK plus once of LSB 6-bit PWM counting	
			10	4 times of MSB 6-bit PWM counting by 1/16 PWCLK plus once of LSB 6-bit PWM counting	
			11	PWM counting	
10	Read/Write	PWM data synchronization mode	0	Auto-synchronization	1
			1	Manual synchronization	
9-2	Read/Write	Current gain adjustment	00000000 ~ 11111111	Adjust the current value set by R-EXT over 256 steps	8b 10101011
1	Read/Write	Thermal Shutdown function	0	Disable	0
			1	Enable [2] (output channels OFF if temperature overcomes 150°C)	
0	Read/Write	Time-out alert for PWCLK disconnection	0	Enable [3]	0
			1	Disable	

1. Please refer to “setting the PWM counting mode” section.
2. Please refer to “TSD” thermal error flag and thermal shutdown “section.
3. Please refer to “time-out alert of PWCLK disconnection” section.

8 Grey scales data loading

The STP1612PW05 is able to manage a gray-scale depth of 12 or 16 bits for each output, exploiting an e-PWM algorithm.

The bit D of the configuration register is used to select the grey-scale loading. Its value can be set to “0” for 12 bits or “1” for 16 bits. By default, D is set to “0”.

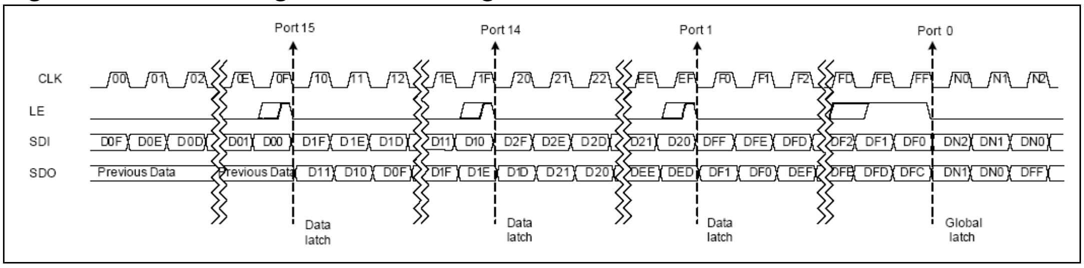
Loading of the data is performed through the serial input on a dedicated buffer and two different methods can be used.

With both methods, the first incoming data packet is relative to the output 15; the following packet is relative to the output 14 and so on up to the output 0.

If F=”0”, when a data packet has been loaded, the latch signal (LE) must become active for one CLK cycle (data latch). When the last data packet, relative to the output 0, has been loaded, the latch signal must be active for two CLK cycles (global latch) and all the data will be transferred to the e-PWM registers starting from the MSB.

If F=”1” all data packets (12 or 16 bits x16) are loaded and then the global latch signal must be active and all the data will be transferred to the e-PWM registers starting from the MSB.

Figure 7. Full timing for data loading



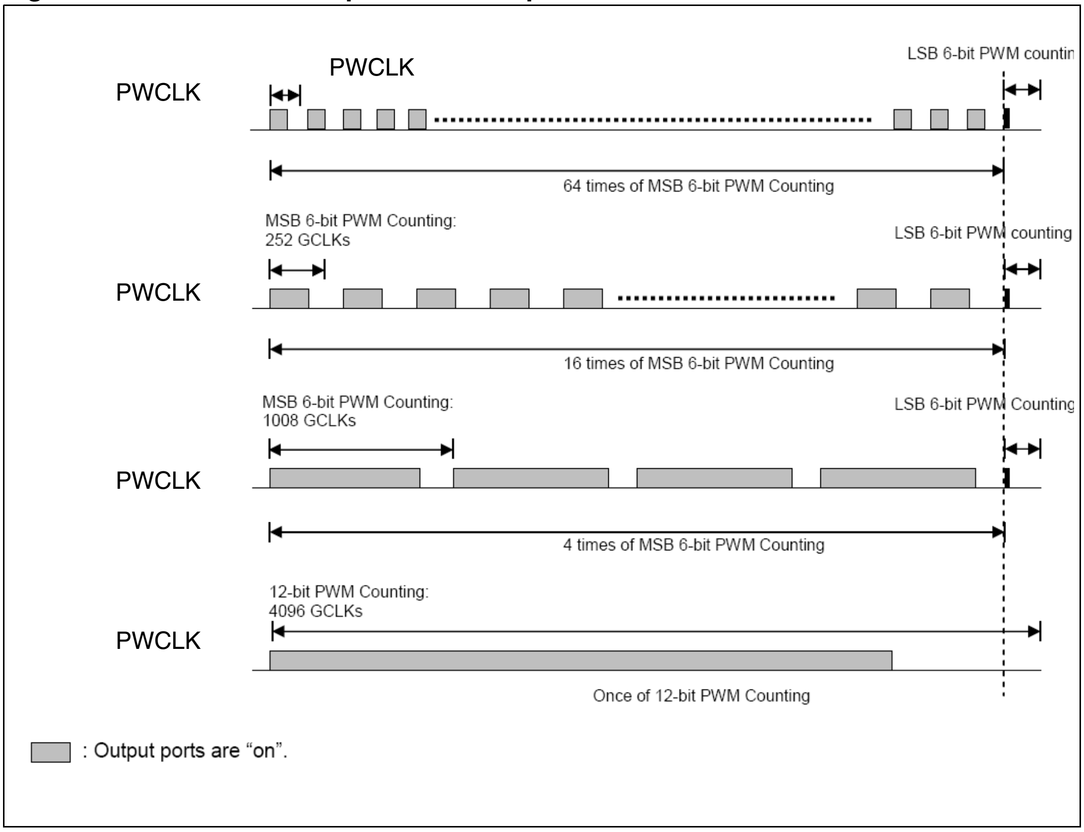
9 Setting the PWM gray scale counter

STP1612PW05 provides a 12-bit or 16-bit PWM color depth. Each serial data input will be implemented according to the e-PWM algorithm.

9.1 PWM data synchronization

STP1612PW05 defines the different counting algorithms that support e-PWM, technology, (scrambled PWM). With e-PWM, the total PWM cycles can be broken down into MSB (most significant bits) and LSB (least significant bits) of gray scale cycles, and the MSB information can be dithered across many refresh cycles to achieve overall same high bit resolution. STP1612PW05 also allows changing different counting algorithms and provides the best output linearity when there are fewer transitions of output.

Figure 8. 12-bit e-PWM operation example



9.2 Synchronization for PWM counting

The data synchronization between the incoming data flow and the output channels is managed through the bit A within the configuration register.

If the bit A is set to “0” the device performs itself the data synchronization: when all the new data are loaded with a “global latch”, the device wait until all the PWM counter completes the counting cycle before updating them with the new data, at the next CLK rising edge.

Conversely, if bit A is set to “1” (default), the data synchronization is not performed by the device and is managed by the microcontroller, which has to take care of the data and signals. If this is not done, there might be artefacts on the output image.

Figure 9. Synchronization for PWM counting

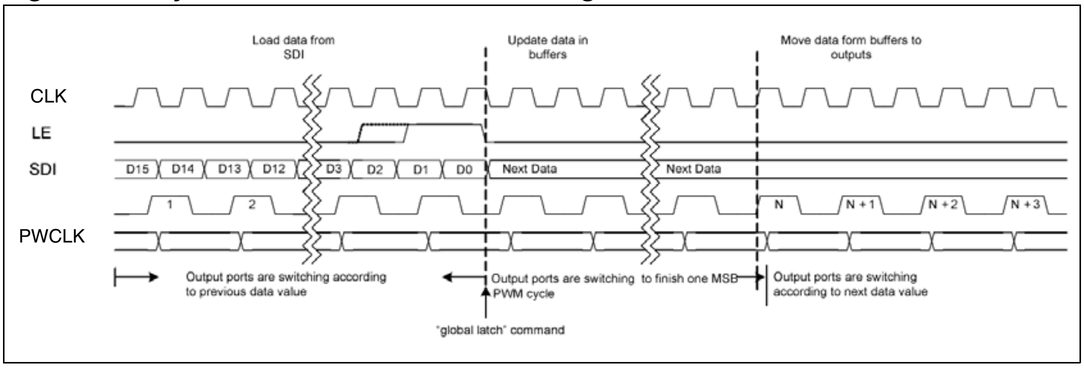
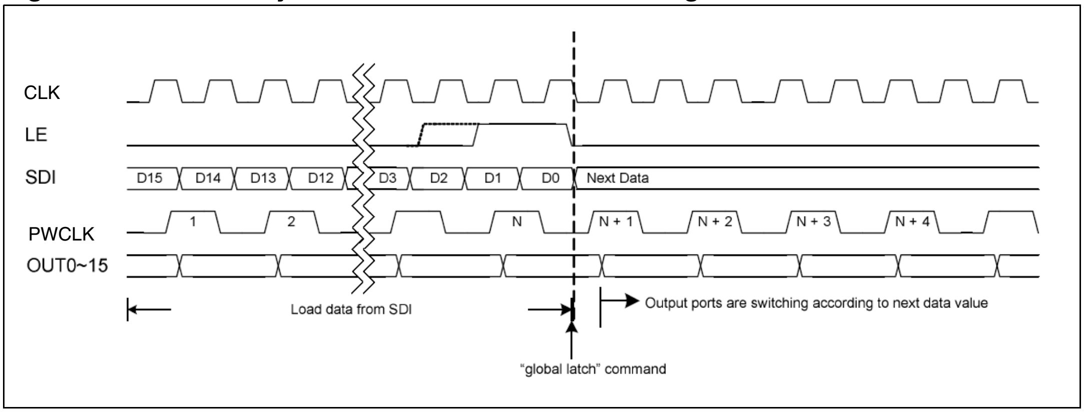


Figure 10. Without synchronization for PWM counting



10 Error detection conditions

The STP1612PW05 can detect open channels (OD) and LED short-circuits (SD).

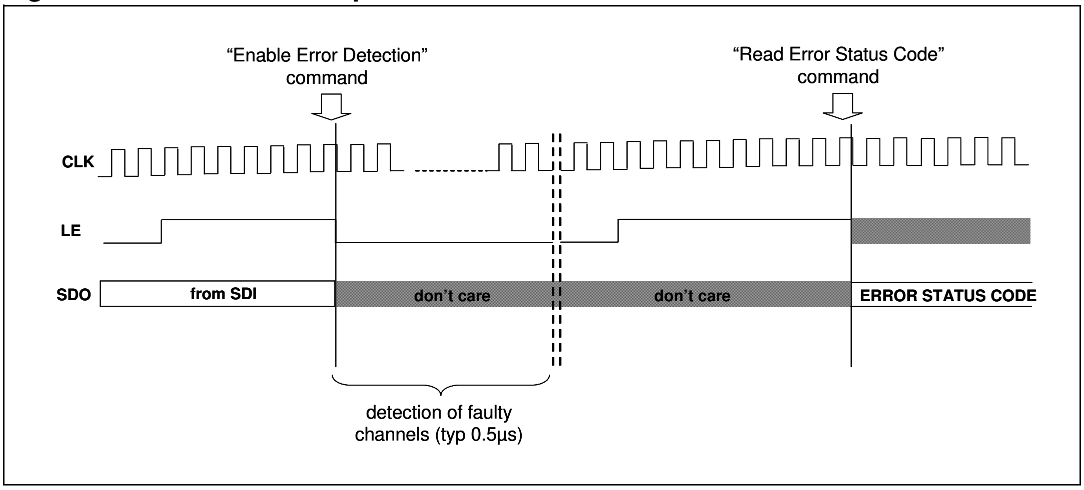
The detection circuitry performs open- and short-circuit detection simultaneously and needs that all channels must be on. However the short test duration (0.5 µs typ) does not impact the image quality.

According to *Table 11*, the command “Enable Error Detection” starts the diagnostic process. After 0.5 µs (typ) the faults detection has already been carried out and, through the command “Read Error Status Code”, the status is available on the serial output (SDO).

A bit set to "1" in the Error Status Code represents a channel considered good, whereas a "0" represents a failed output (open/short).

Figure 11 describes the error detection process.

Figure 11. Error detection process



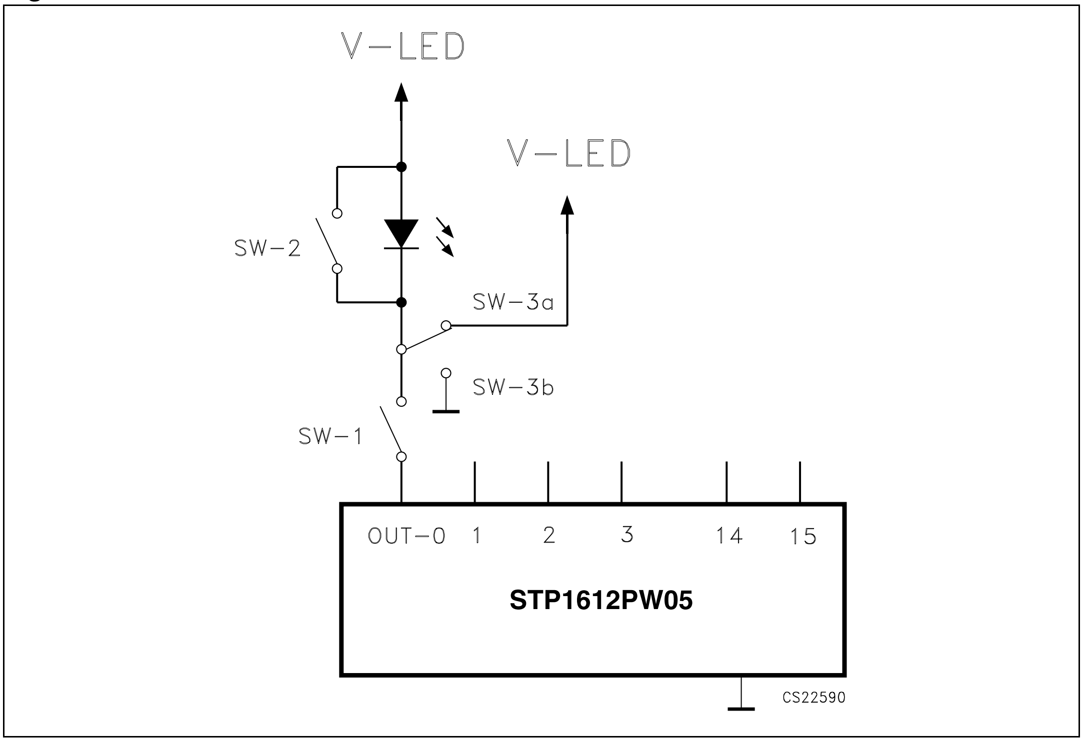
The *Table 13* and *Figure 12* explains the fault conditions detected by the diagnostic circuitry and how the detection is performed.

Table 13. Detection conditions (V_{DD} = 3.3 to 5 V temp. range -40 to 125 °C)

SW-1 or SW-3b	Open line or output short to GND detected	==> $I_{ODEC} \leq 0.5 \times I_O$
SW-2 or SW-3a	Short on LED or short to V-LED detected	==> $V_O \geq 2.3$ V

Note: Where: I_O = the output current programmed by the R_{EXT}, I_{ODEC} = the detected output current in detection mode

Figure 12. Detection circuit



11 Setting output current

The output current (I_{OUT}) is set by an external resistor, R_{ext}.

It is calculated from the equation:

$V_{R\text{-}EXT} = 1.24 \times G$; $I_{OUT} = (V_{R\text{-}EXT}/R_{ext}) \times 560$

Whereas R_{ext} is the resistance of the external resistor connected to R-EXT terminal and $V_{R\text{-}EXT}$ is its voltage. G is the digital current gain, which is set by the bit9 – bit2 of the configuration register. The default value of G is 1. For your information, the output current is about 20 mA when R_{ext} = 34.70 kΩ and 10 mA when R_{ext} = 69.6 kΩ if G is set to default value 1. The formula and setting for G are described in next section.

Figure 13. Rext vs output current

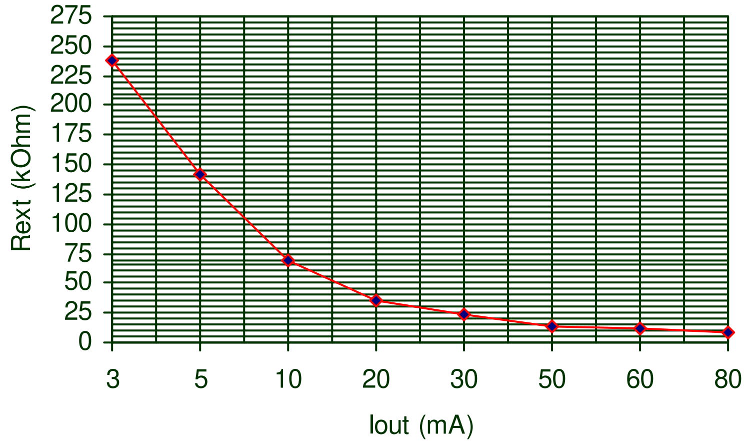


Table 14. Rext vs output current (1)

Iout (mA)	Rext (kΩ)
3	238.2
5	142.2
10	69.6
20	34.70
30	22.94
50	13.72
60	11.40
80	8.63

1. T_A = 25 °C, V_{dd} = 3.3 V; 5.0 V, V_{Led} = 3.0 V, V_{drop} = 1.5 V, HC = 0101011 (default)

12 Constant current

The STP1612PW05 assures nearly no variation in current both from channel to channel and from IC to IC.

The typical variation of the current between channels of the same IC is ±1.5%, whereas the variation between ICs is around ±3%.

Moreover the current characteristic of the output stage is flat (see *Figure 14* and *Figure 15*). This contributes to keep the current constant regardless of the variation of the LEDs forward voltage (V_F) and consequently guarantees uniformity of brightness.

Figure 14. I_{OUT}vs voltage drop across current generators (3.3 V supply voltage)

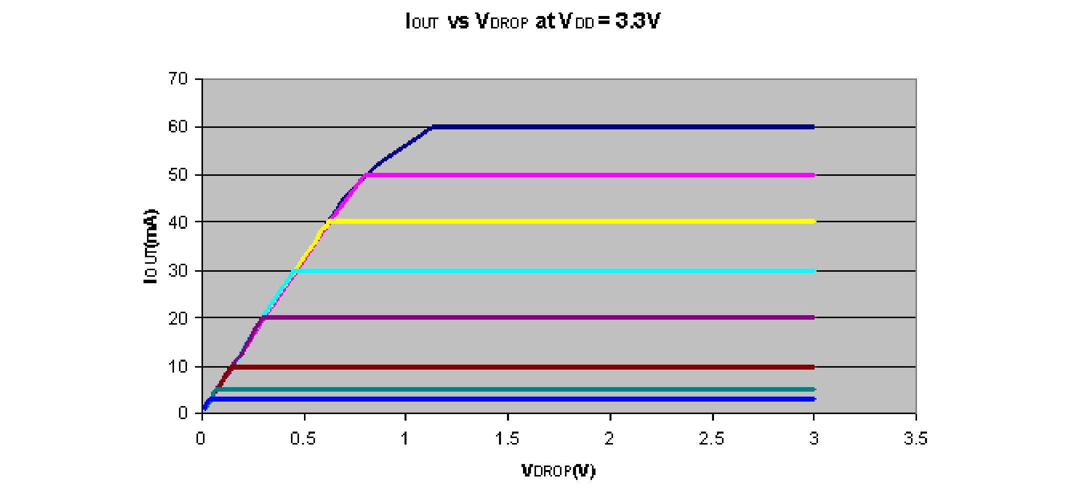
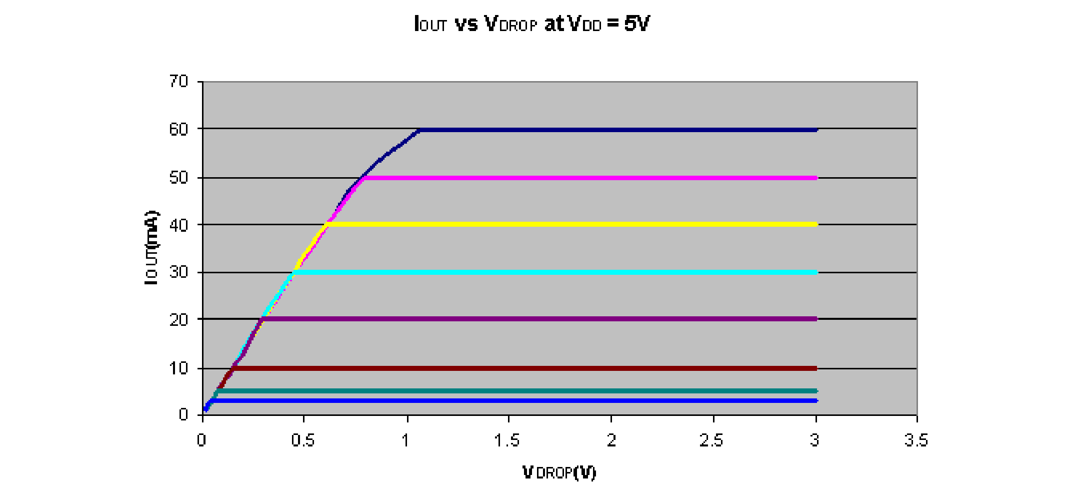


Figure 15. I_{OUT} vs voltage drop across current generators (5 V supply voltage)

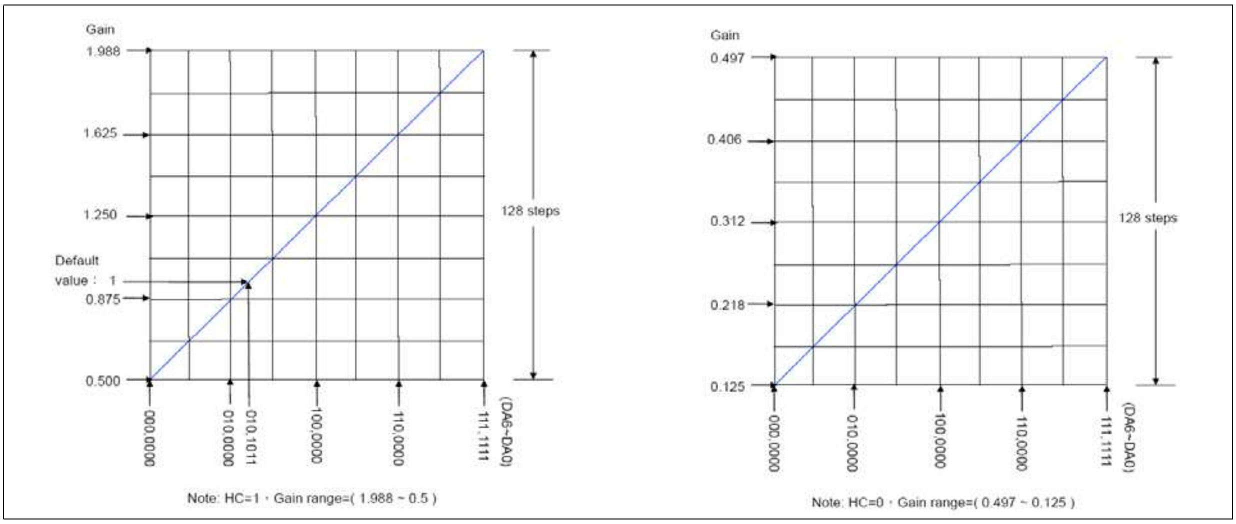


The typical characteristics in *Figure 14* and *Figure 15* also show the minimum voltage drop required to assure that the current generators regulate the desired current.

This must be taken into account when choosing the suitable value of the LED supply voltage (see dedicated section).

13 Current gain adjustment

Figure 16. Gain vs DA6 - DA0



The bit 9 to bit 2 of the configuration register set the gain of output current, i.e., G. Being 8-bit in total, ranging from 8'b00000000 to 8'b11111111, these bits allow the user to set the output current gain up to 256 levels. These bits can be further defined in the configuration register as follows:

Configuration register

MSB LSB

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	HC	DA6	DA5	DA4	DA3	DA2	DA1	DA0	-	-

1. Bit 9 is HC bit. The setting is in the low current range when HC=0, and in the high current range when HC=1.
2. Bit 8 to bit 2 are DA6 ~ DA0.

The relationship between these bits and current gain G is:

HC = 1, D = (256G-128)/3

HC = 0, D = (1024G-128)/3

and D in the above decimal numeration can be converted to its equivalent in binary form by the following equation:

$D = DA6x2^6 + DA5x2^5 + DA4x2^4 + DA3x2^3 + DA2x2^2 + DA1x2^1 + DA0x2^0$

In other words, these bits can be looked as a floating number with 1-bit exponent HC and 7-bit mantissa DA6~DA0.

For example,

HC = 1, G = 1.25, D = (256x1.25-128)/3 = 64

the D in binary form would be:

$D = 64 = 1x2^6+0x2^5+0x2^4+0x2^3+0x2^2+0x2^1+0x2^0$

The bit 9 to bit 2 of the configuration register are set to 8’b1100,0000.

14 Delay time of staggered output

This feature prevents large inrush current from the power line and reduces the bypass capacitors.

The outputs are organized in four groups OUT4n, OUT4n+1, OUTn4+2, OUT4n+3 and each group has 40 ns delay between the previous one.

E.g.: OUT4n has no delay, OUTn4+1 has 40ns delay, OUTn4+2 has 80ns delay, OUTn4+3 has 120 ns delay.

15 Thermal protection

Thermal flag provides an indication about the status of the junction temperature. When the junction temperature reaches 150 °C the bit E of the configuration register is set to “1”, signaling dangerous operating condition. This flag is useful when thermal shutdown function is disabled.

The thermal shutdown function, if activated by configuration register (bit “1” set to 1), turns-off all output channels if the junction exceeds 150 °C. As soon as the junction temperature is below 140 °C the outputs channels will be turned ON. In thermal shutdown mode, the digital core is active and data flow is guaranteed.