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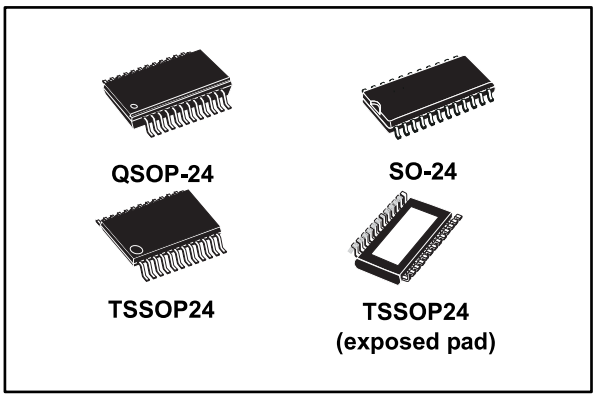
STP16CP05

Low voltage 16-bit constant current LED sink driver

Datasheet - production data



Features

- Low voltage power supply down to 3 V
- 16 constant current output channels
- Adjustable output current through external resistor
- Serial data IN/parallel data OUT
- Can be driven by a 3.3 V microcontroller
- Output current: 5 to 100 mA
- Max clock frequency 30 MHz
- ESD protection: 2 kV HBM, 200 V MM

Description

The STP16CP05 is a monolithic, low voltage, low current power 16-bit shift register designed for LED panel displays. The STP16CP05 contains a 16-bit serial-in, parallel-out shift register that feeds a 16-bit, D-type storage register. In the output stage, sixteen regulated current sources provide from 5 mA to 100 mA constant current to drive the LEDs.

The output current setup time is 40 ns (typ.), thus improving the system performance.

The LEDs' brightness can be controlled by using an external resistor to adjust the STP16CP05 output current.

The STP16CP05 guarantees a 20 V output driving capability, allowing users to connect more LEDs in series. The high clock frequency, 30 MHz, makes the device suitable for high data rate transmission. The 3.3 V voltage supply is useful in applications that interface with a 3.3 V micro controller.

Table 1: Device summary

Order code	Package	Packing
STP16CP05MTR	SO-24	1000 parts per reel
STP16CP05TTR	TSSOP24	2500 parts per reel
STP16CP05XTTR	TSSOP24 exposed pad	2500 parts per reel
STP16CP05PTR	QSOP-24	2500 parts per reel

Contents

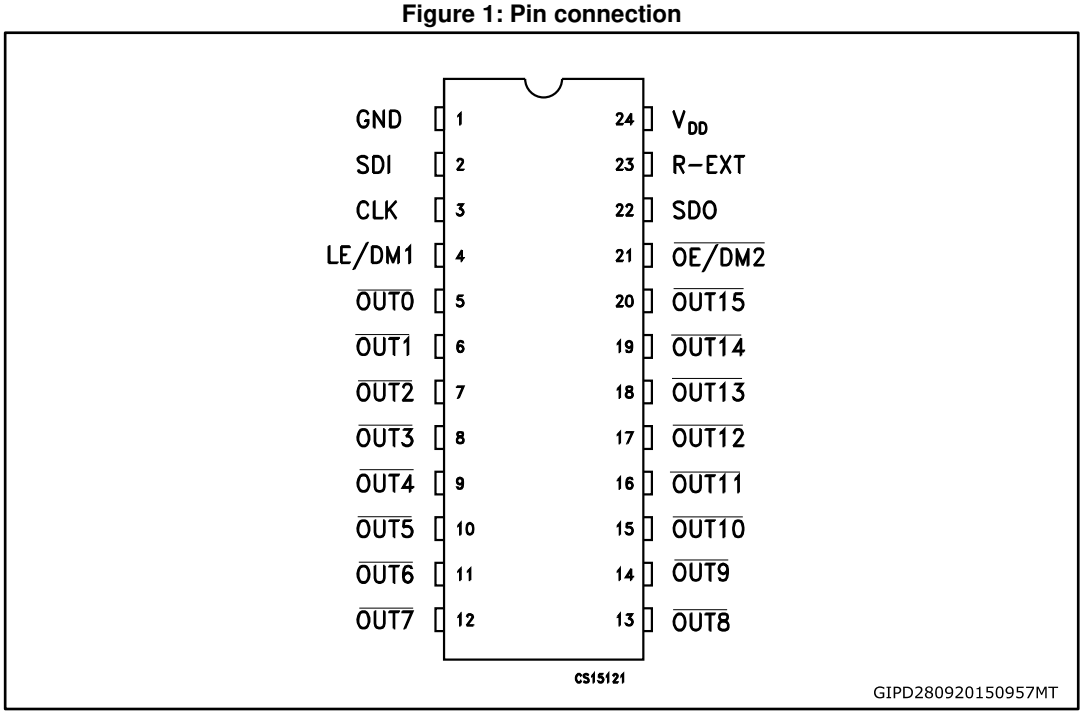
1 Summary description

Table 2: Typical current accuracy

Output voltage	Current accuracy		Output current	V_{DD}	Temperature
	Between bits	Between ICs			
≥ 1.3 V	± 1.5 %	± 5 %	20 to 100 mA	3.3 V to 5 V	25 °C

1.1 Pin connection and description

Figure 1: Pin connection



The exposed pad should be electrically connected to a metal land electrically isolated or connected to ground.

Table 3: Pin description

Pin n°	Symbol	Name and function
1	GND	Ground terminal
2	SDI	Serial data input terminal
3	CLK	Clock input terminal
4	LE/DM1	Latch input terminal
5-20	OUT 0-15	Output terminal
21	$\overline{OE}$/DM2	Input terminal of output enable (active low)
22	SDO	Serial data out terminal
23	R-EXT	Input terminal for an external resistor for constant current programming
24	V_{DD}	Supply voltage terminal

2 Electrical ratings

2.1 Absolute maximum ratings

Stressing the device above the ratings listed in the “absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other condition above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage	0 to 7	V
V_O	Output voltage	-0.5 to 20	V
I_O	Output current	100	mA
V_I	Input voltage	-0.4 to V_{DD}	V
I_{GND}	GND terminal current	1600	mA
f_{CLK}	Clock frequency	50	MHz
T_J	Junction temperature range	-40 to +170	°C

2.2 Thermal data

Table 5: Thermal data

Symbol	Parameter		Value	Unit
T_{OPR}	Operating temperature range		-40 to +125	°C
T_{STG}	Storage temperature range		-55 to +150	°C
R_{thJA}	Thermal resistance junction-ambient (1)	SO-24	42.7	°C/W
		TSSOP24	55	°C/W
		TSSOP24 (2) exposed pad	37.5	°C/W
		QSOP-24	55	°C/W

Notes:

(1) According with JEDEC standard 51-7.

(2) The exposed pad should be soldered directly to the PCB to realize the thermal benefits.

2.3 Recommended operating conditions

@ T_A = 25 °C

Table 6: Recommended operating conditions

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage		3.0	-	5.5	V
V_O	Output voltage			-	20	V
I_O	Output current	OUTn	3	-	100	mA
I_{OH}	Output current	SERIAL-OUT		-	+1	mA
I_{OL}	Output current	SERIAL-OUT		-	-1	mA
V_{IH}	Input voltage		0.7 V_{DD}	-	V_{DD}	V
V_{IL}	Input voltage		-0.3	-	0.3 V_{DD}	V
t_{wLAT}	LE/DM1 pulse width	V_{DD} = 3.0 V to 5.0 V	6	-		ns
t_{wCLK}	CLK pulse width		8	-		ns
t_{wEN}	$\overline{OE/DM2}$ pulse width		100	-		ns
$t_{SETUP(D)}$	Setup time for DATA		5	-		ns
$t_{HOLD(D)}$	Hold time for DATA		3	-		ns
$t_{SETUP(L)}$	Setup time for LATCH		18	-		ns
f_{CLK}	Clock frequency	Cascade operation (1) V_{DD} = 5 V		-	30	MHz

Notes:

(1) If the device is connected in cascade, it may not be possible achieve the maximum data transfer. Please consider the timings carefully.

3 Electrical characteristics

V_{DD} = 3.3 V to 5 V, T_A = 25 °C, unless otherwise specified.

Table 7: Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IH}	Input voltage high level		0.7 V_{DD}		V_{DD}	V
V_{IL}	Input voltage low level		GND		0.3 V_{DD}	V
I_{OH}	Output leakage current	V_{OH} = 20 V			1	µA
V_{OL}	Output voltage (serial-OUT)	I_{OL} = 1 mA			0.4	V
V_{OH}	Output voltage (serial-OUT)	I_{OH} = -1 mA	V_{DD}-0.4V			V
I_{OL1}	Output current	V_O = 0.3 V, R_{ext} = 4.2 kΩ	4.25	5	5.75	mA
I_{OL2}		V_O = 0.3 V, R_{ext} = 1 kΩ	19	20	21	
I_{OL3}		V_O = 1.3 V, R_{ext} = 200 Ω	96	100	104	
ΔI_{OL1}	Output current error between bit (all output ON)	V_O = 0.3 V, R_{ext} = 4.2 kΩ		± 5	± 8	%
ΔI_{OL2}		V_O = 0.3 V, R_{ext} = 1 kΩ		± 1.5	± 3	
ΔI_{OL3}		V_O = 1.3 V, R_{ext} = 200 Ω		± 1.2	± 3	
$R_{SIN(up)}$	Pull-up resistor		150	300	600	kΩ
$R_{SIN(down)}$	Pull-down resistor		100	200	400	kΩ
$I_{DD(OFF1)}$	Supply current (OFF)	R_{ext} = 1 kΩ, OUT 0 to 15 = OFF		4		mA
$I_{DD(OFF2)}$		R_{ext} = 250 Ω, OUT 0 to 15 = OFF		11.2		
$I_{DD(ON1)}$	Supply current (ON)	R_{ext} = 1 kΩ, OUT 0 to 15 = ON		4.5		
$I_{DD(ON2)}$		R_{ext} = 250 Ω, OUT 0 to 15 = ON		11.7		
Thermal	Thermal protection			170		°C

V_{DD} = 5 V, T_A = 25 °C, unless otherwise specified.

Table 8: Switching characteristics

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
t_{PLH1}	Propagation delay time, CLK- $\overline{OUTn}$, LE/DM1 = H, $\overline{OE/DM2}$ = L	$V_{IH} = V_{DD}$ V_{IL} = GND C_L = 10 pF I_O = 20 mA V_L = 3.0 V R_{ext} = 1 KΩ R_L = 60 Ω	V_{DD} = 3.3 V	-	45	74	
			V_{DD} = 5 V	-	24	38	ns
t_{PLH2}	Propagation delay time, LE/DM1- $\overline{OUTn}$, $\overline{OE/DM2}$ = L		V_{DD} = 3.3 V	-	48	77	
			V_{DD} = 5 V	-	27	46	ns
t_{PLH3}	Propagation delay time, $\overline{OE/DM2}$ - $\overline{OUTn}$, LE/DM1 = H		V_{DD} = 3.3 V	-	75	128	
			V_{DD} = 5 V	-	43	64	ns
t_{PLH}	Propagation delay time, CLK-SDO		V_{DD} = 3.3 V	-	19	28	
			V_{DD} = 5 V	-	11	16.5	ns
t_{PHL1}	Propagation delay time, CLK- $\overline{OUTn}$, LE/DM1 = H, $\overline{OE/DM2}$ = L		V_{DD} = 3.3 V	-	15	23	
			V_{DD} = 5 V	-	10	14	ns
t_{PHL2}	Propagation delay time, LE/DM1 $\overline{-OUTn}$, $\overline{OE/DM2}$ = L		V_{DD} = 3.3 V	-	13	18.5	
			V_{DD} = 5 V	-	9	12	ns
t_{PHL3}	Propagation delay time, $\overline{OE/DM2}$ - $\overline{OUTn}$, LE/DM1 = H		V_{DD} = 3.3 V	-	17	24.5	
			V_{DD} = 5 V	-	14	19.5	ns
t_{PHL}	Propagation delay time, CLK-SDO		V_{DD} = 3.3 V	-	23	35	
			V_{DD} = 5 V	-	14	21	ns
t_{ON}	Output rise time 10~90% of voltage waveform		V_{DD} = 3.3 V	-	35	68	
			V_{DD} = 5 V	-	21	31.5	ns
t_{OFF}	Output fall time 90~10% of voltage waveform		V_{DD} = 3.3 V	-	10.5	15	
			V_{DD} = 5 V	-	11	15.5	ns
t_r	CLK rise time (1)			-		5000	ns
t_f	CLK fall time (1)			-		5000	ns

Notes:

(1) In order to achieve high cascade data transfer, please consider tr/tf timings carefully.

4 Equivalent circuit and outputs

Figure 2: OE/DM2 terminal

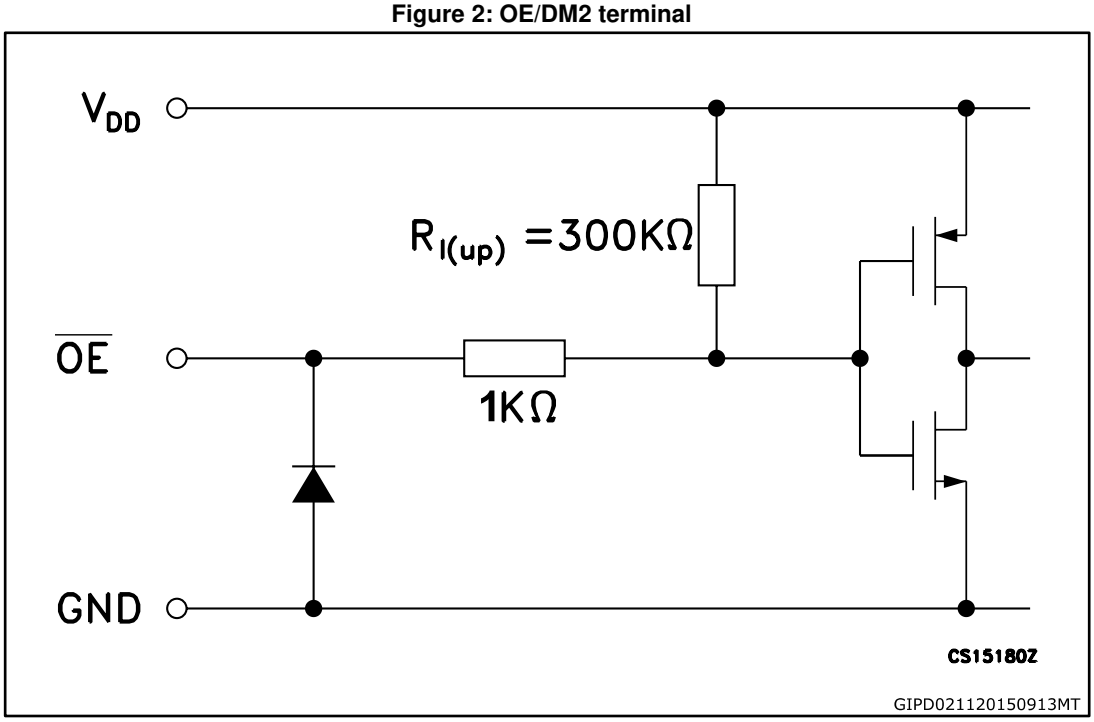


Figure 3: LE/DM1 terminal

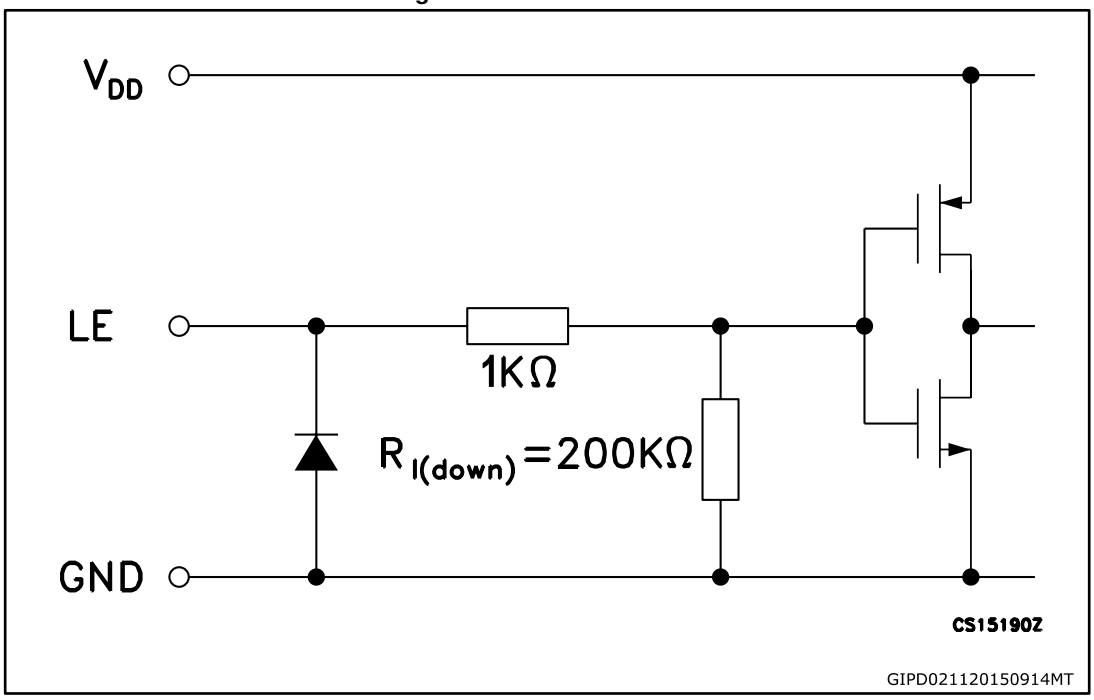


Figure 4: CLK, SDI terminal

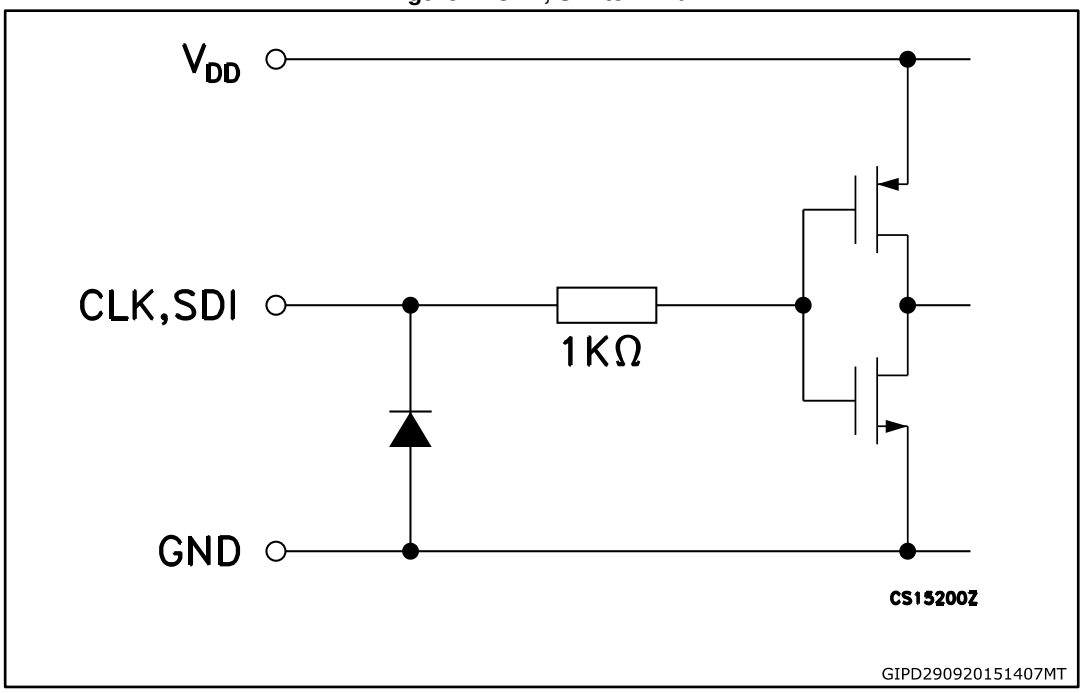


Figure 5: SDO terminal

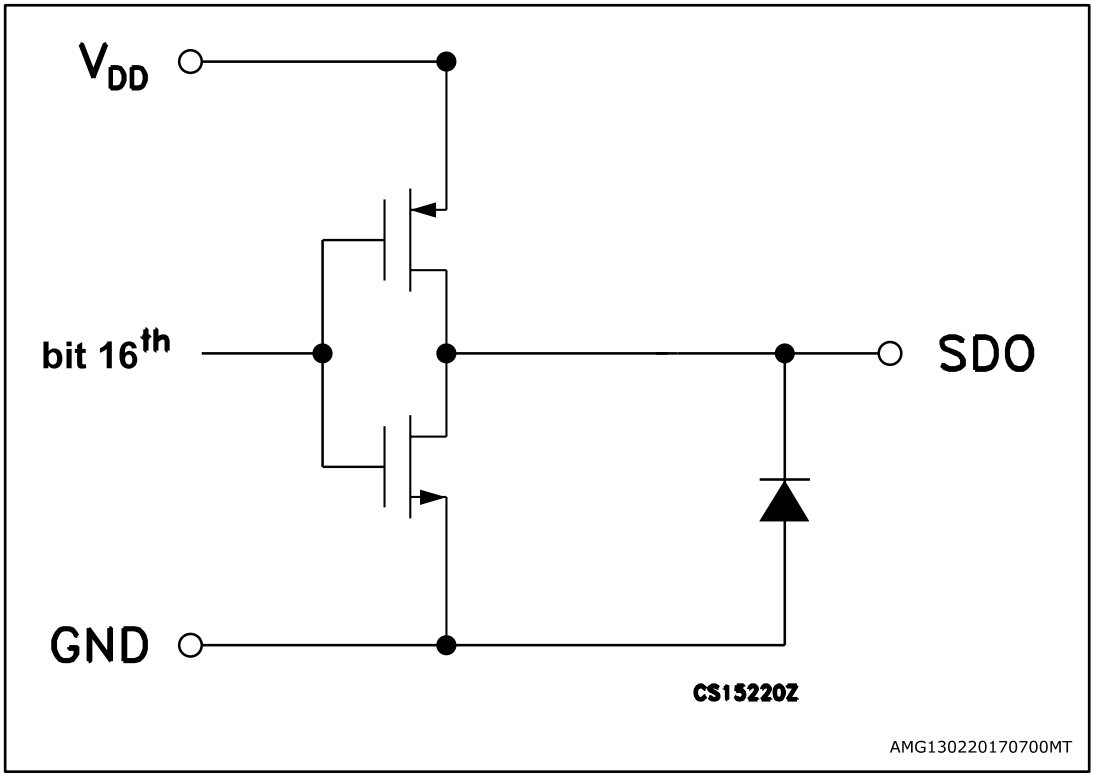
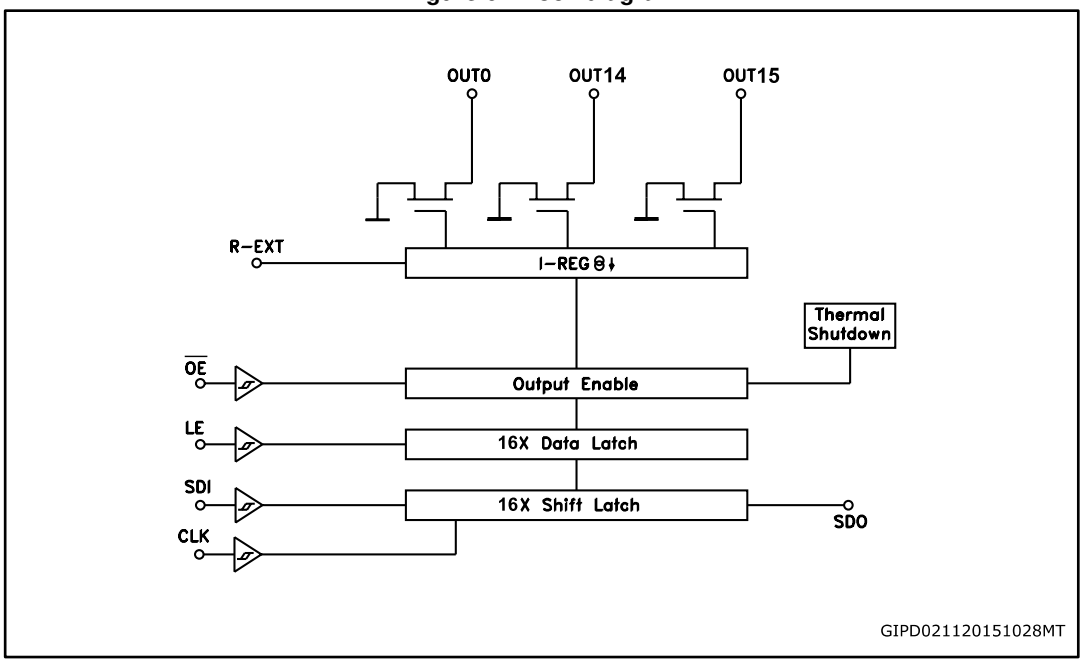


Figure 6: Block diagram



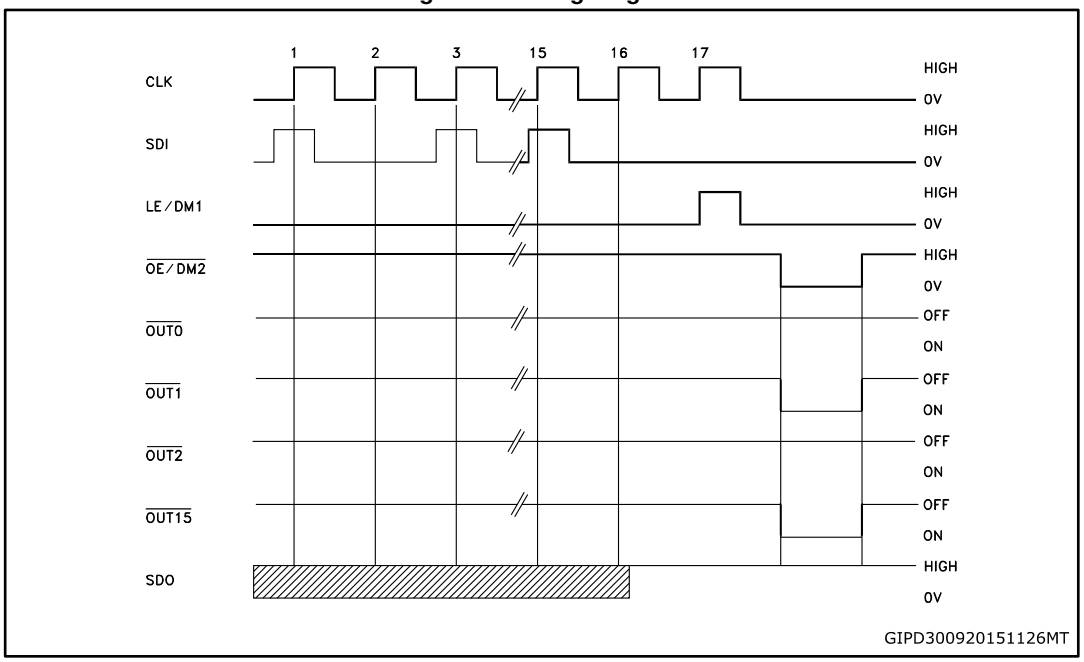
5 Timing diagrams

Table 9: Truth table

CLOCK	LE/DM1	$\overline{OE}$/DM2	SERIAL-IN	$\overline{OUT0}$ ..... $\overline{OUT7}$ ..... $\overline{OUT15}$	SDO
_|¯	H	L	Dn	Dn ..... Dn - 7 ..... Dn -15	Dn - 15
_|¯	L	L	Dn + 1	No change	Dn - 14
_|¯	H	L	Dn + 2	Dn + 2 ..... Dn - 5 ..... Dn -13	Dn - 13
¯|_	X	L	Dn + 3	Dn + 2 ..... Dn - 5 ..... Dn -13	Dn - 13
¯|_	X	H	Dn + 3	OFF	Dn - 13

OUTn = ON when Dn = H OUTn = OFF when Dn = L.

Figure 7: Timing diagram



1 Latch and output enable terminals are level-sensitive and are not synchronized with rising or falling edge of CLK signal.

2 When LE/DM1 terminal is low level, the latch circuit holds previous set of data.

3 When LE/DM1 terminal is high level, the latch circuit refreshes new set of data from SDI chain.

4 When OE/DM2 terminal is at low level, the output terminals Out 0 to Out 15 respond to data in the latch circuits, either ‘1’ for ON or ‘0’ for OFF.

5 When OE/DM2 terminal is at high level, all output terminals are switched OFF.

Figure 8: Clock, serial-in, serial-out

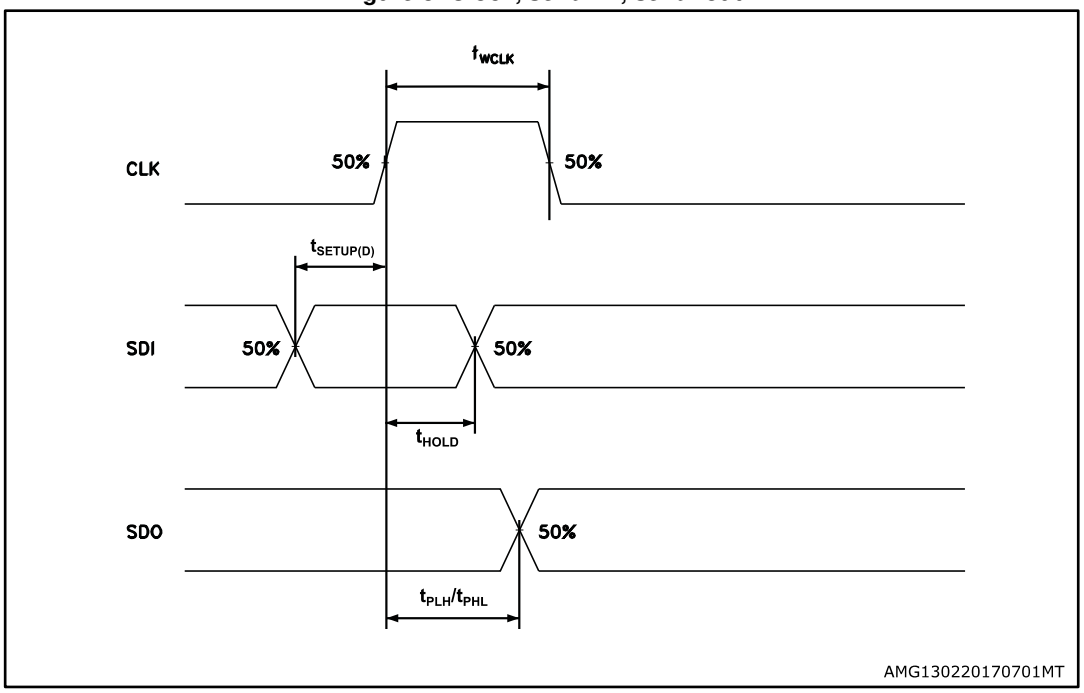


Figure 9: Clock, serial-in, latch, enable, outputs

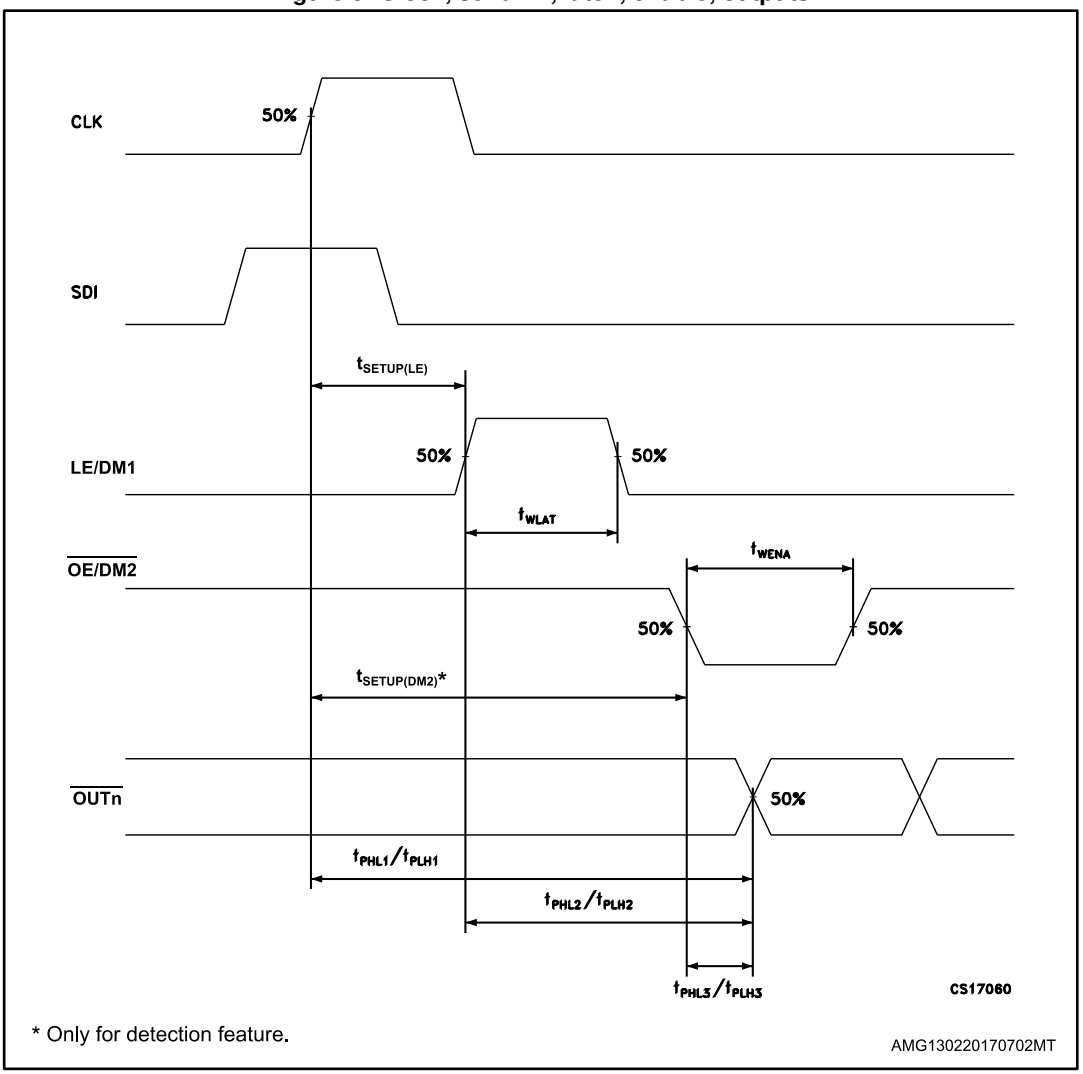
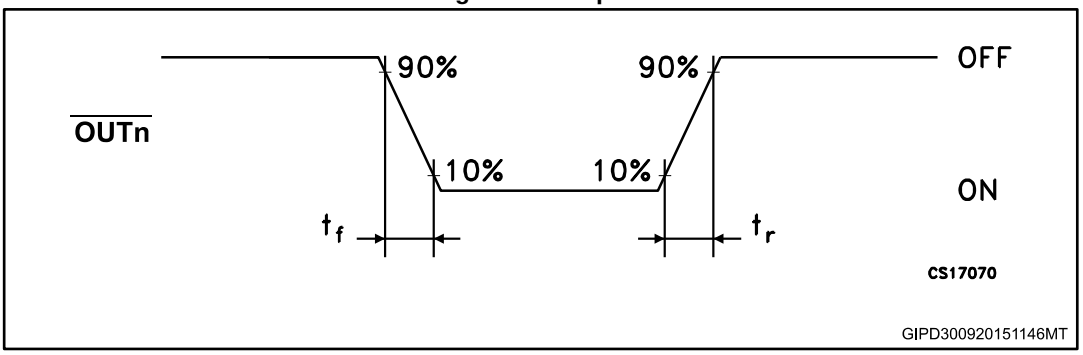


Figure 10: Outputs



6 Typical characteristics

Figure 11: Output current-R_{EXT} resistor

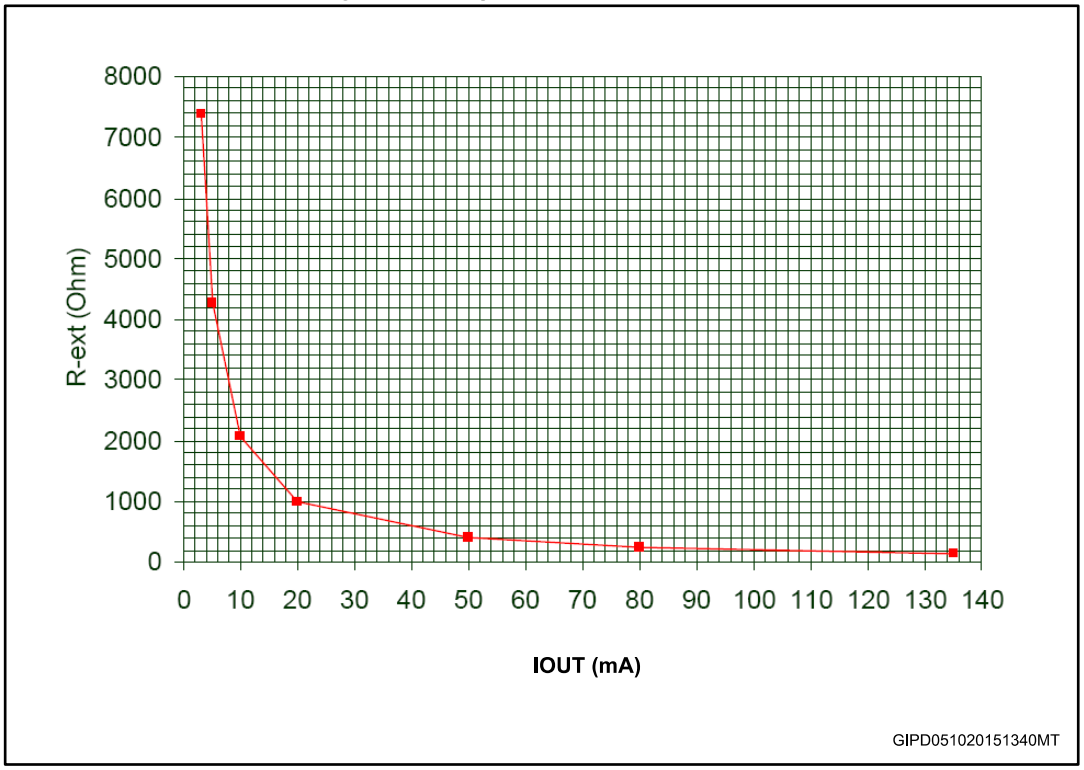


Table 10: Output current-R_{EXT} resistor

R_{EXT} (Ω)	Output current (mA)
7370	3
4270	5
2056	10
1006	20
382	50
251	80
200	100

Figure 12: Output current vs ± ΔI_{OL}(%) T_A = 25 °C

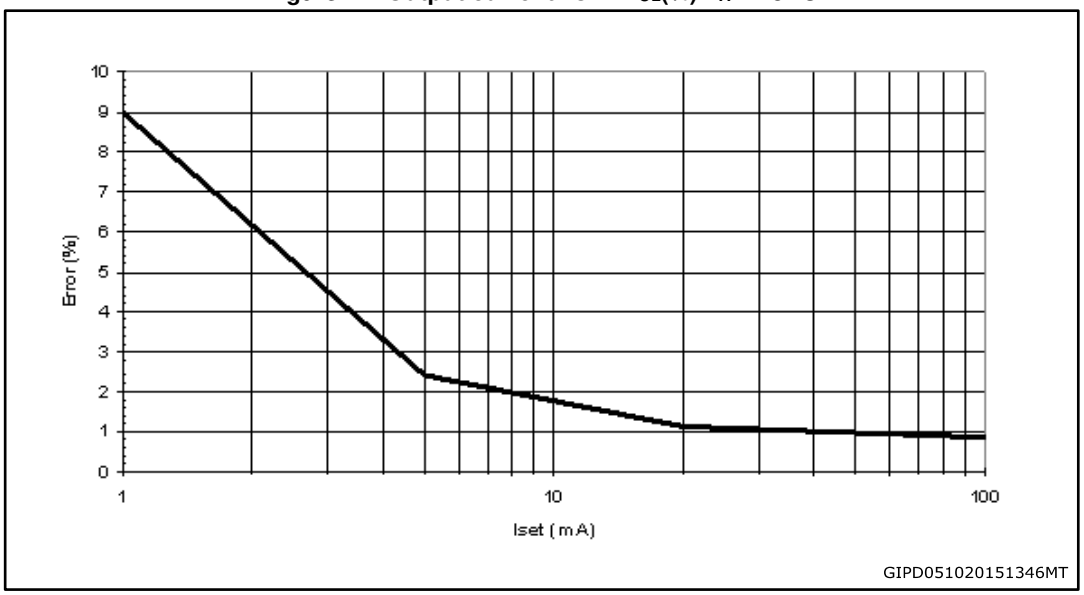


Figure 13: ISET vs drop out voltage (V_{drop}) T_A = 25 °C

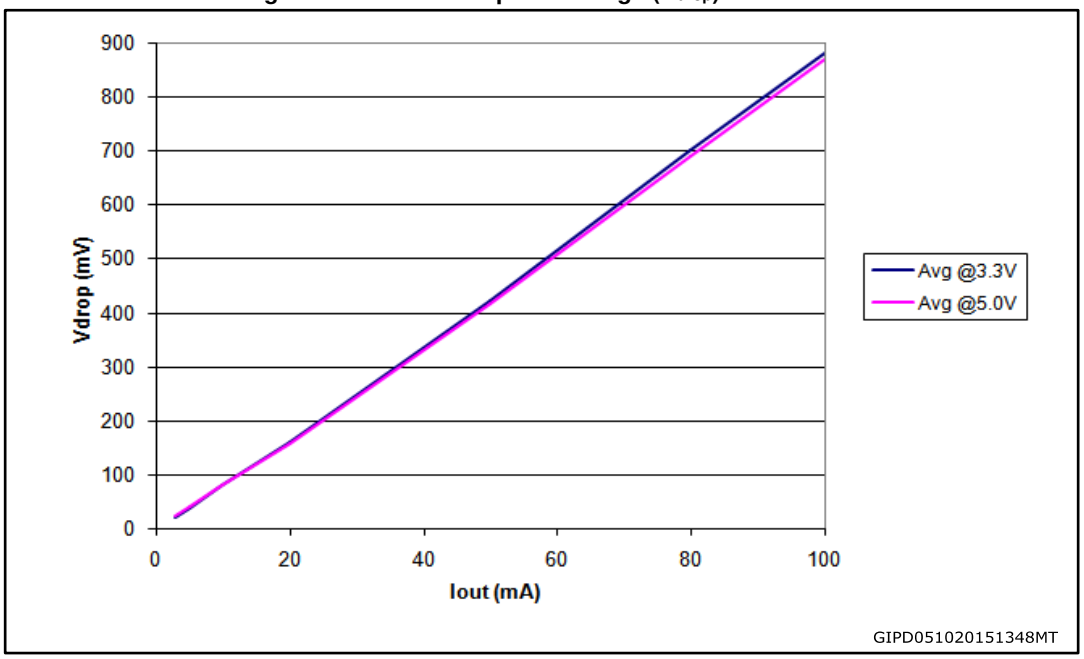
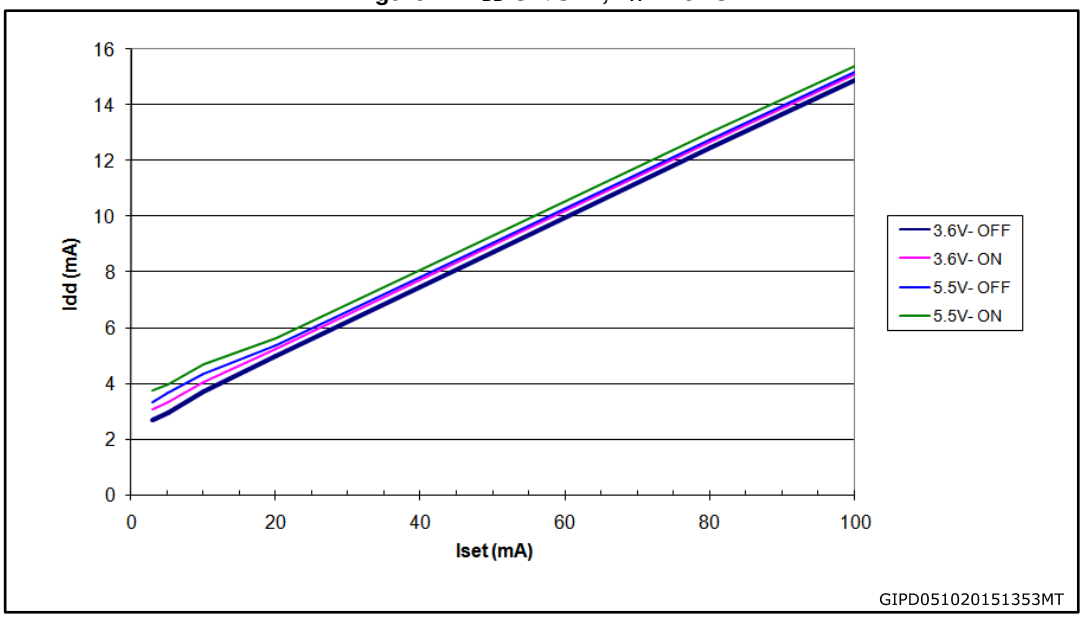


Table 11: I_{SET} vs dropout voltage (V_{drop})

Iout (mA)	Avg (mV) @ 3.3 V	Avg (mV) @ 5.0 V
3	20	22
5	37	40
10	79	79
20	160	158
50	422	415
80	700	690
100	880	870

Figure 14: I_{DD} ON/OFF, T_A = 25 °C



7 Test circuit

Figure 15: DC characteristic

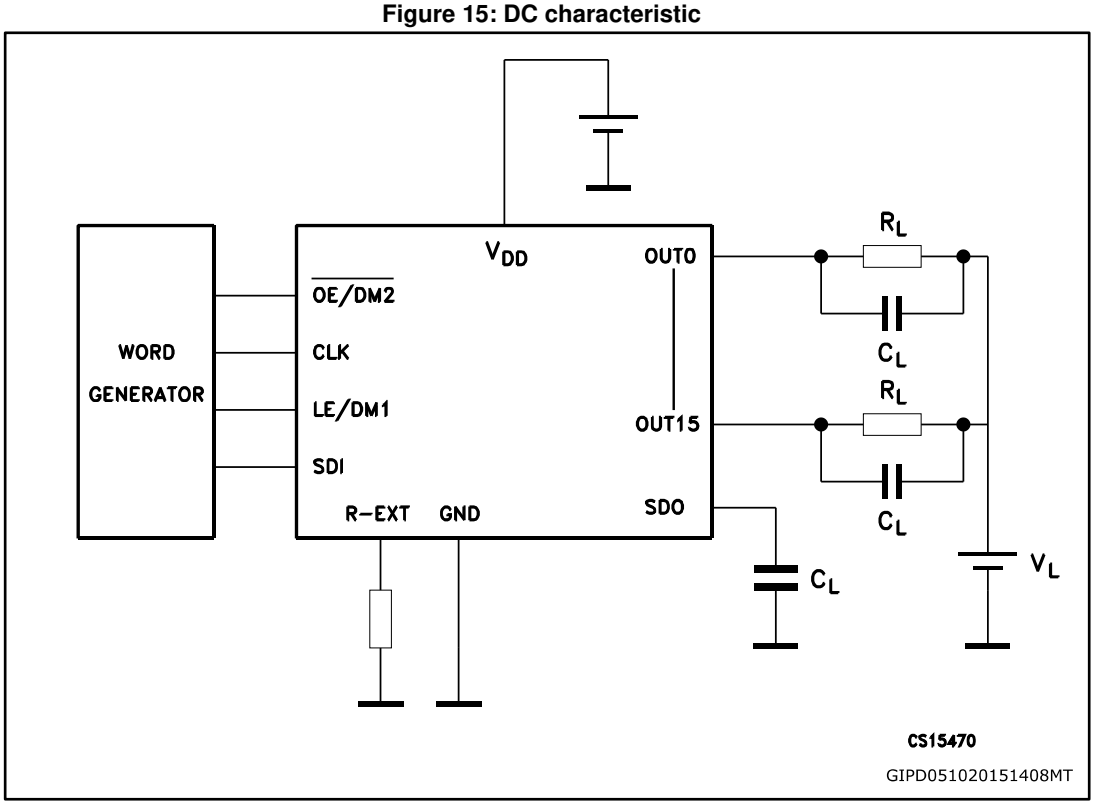


Figure 16: AC characteristic

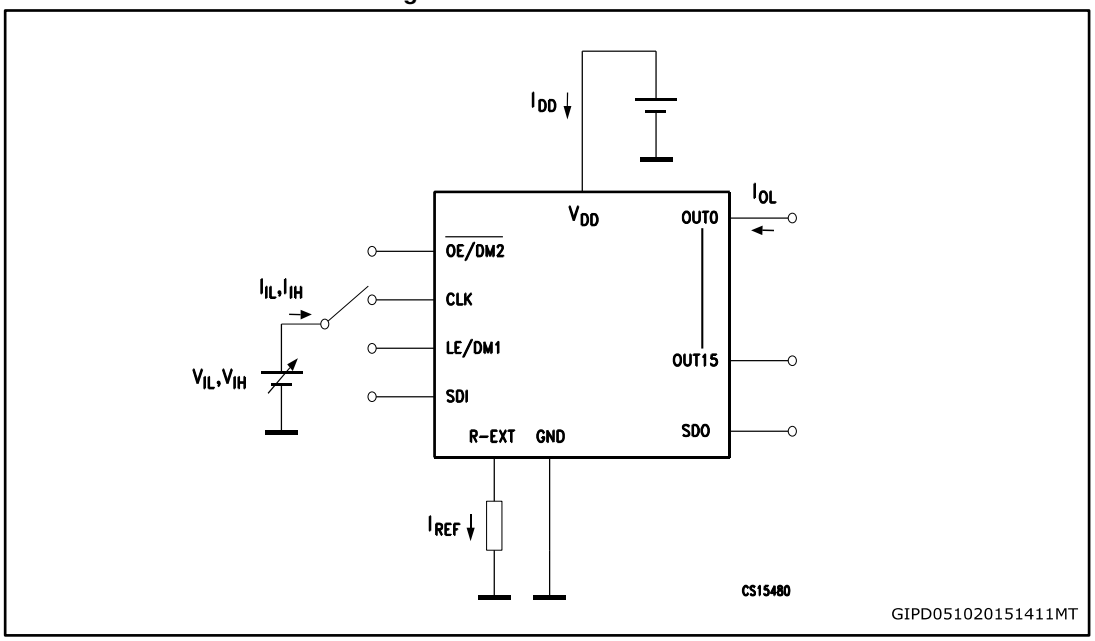
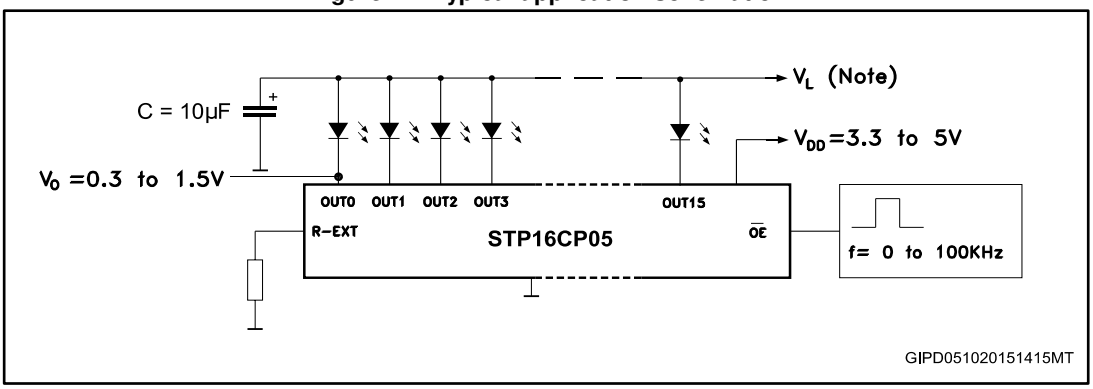


Figure 17: Typical application schematic



V_L will be determined by the V_F of the LEDs.

Test condition: temp. = 25 °C, V_{DD} = 3.0 V, V_{IN} = V_{DD}, C_L = 10 pF, freq. = 1 MHz, Ch1 = $\overline{OE}$/DM2 , Ch2 = SDI, Ch3 = V_{OUT}, Ch4 = I_{OUT}

Figure 18: Turn ON output current setup

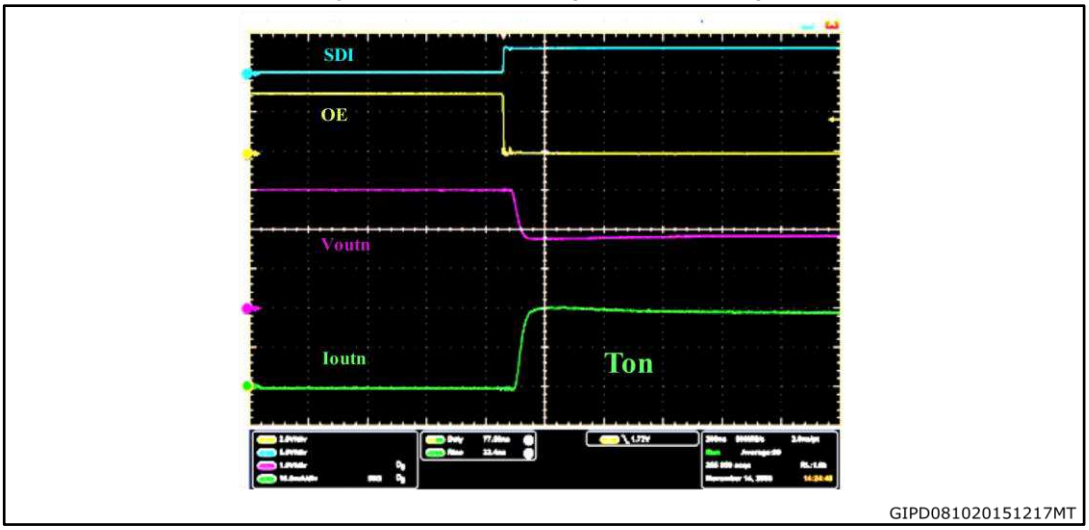
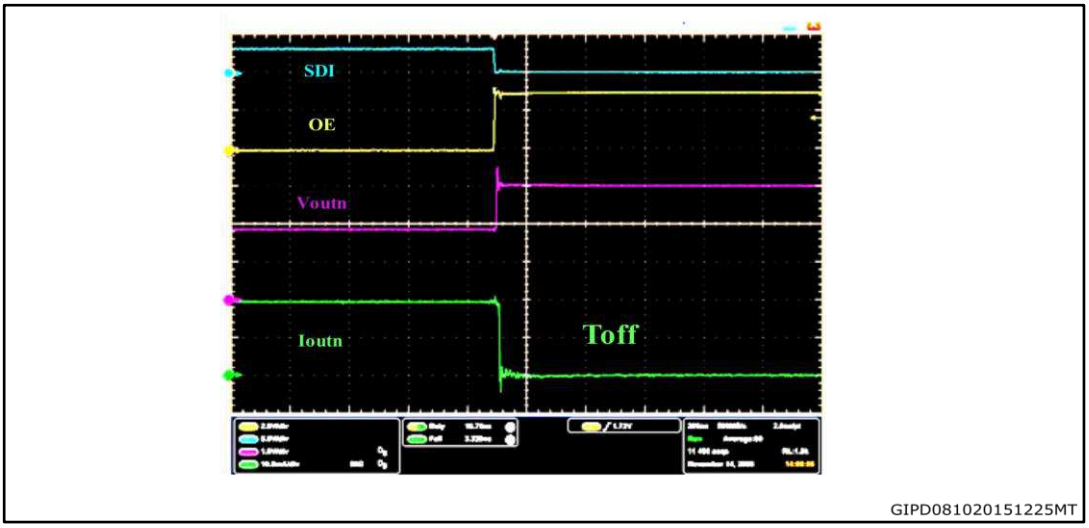


Figure 19: Turn OFF output current setup



8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

8.1 QSOP-24 package information

Figure 20: QSOP-24 package outline

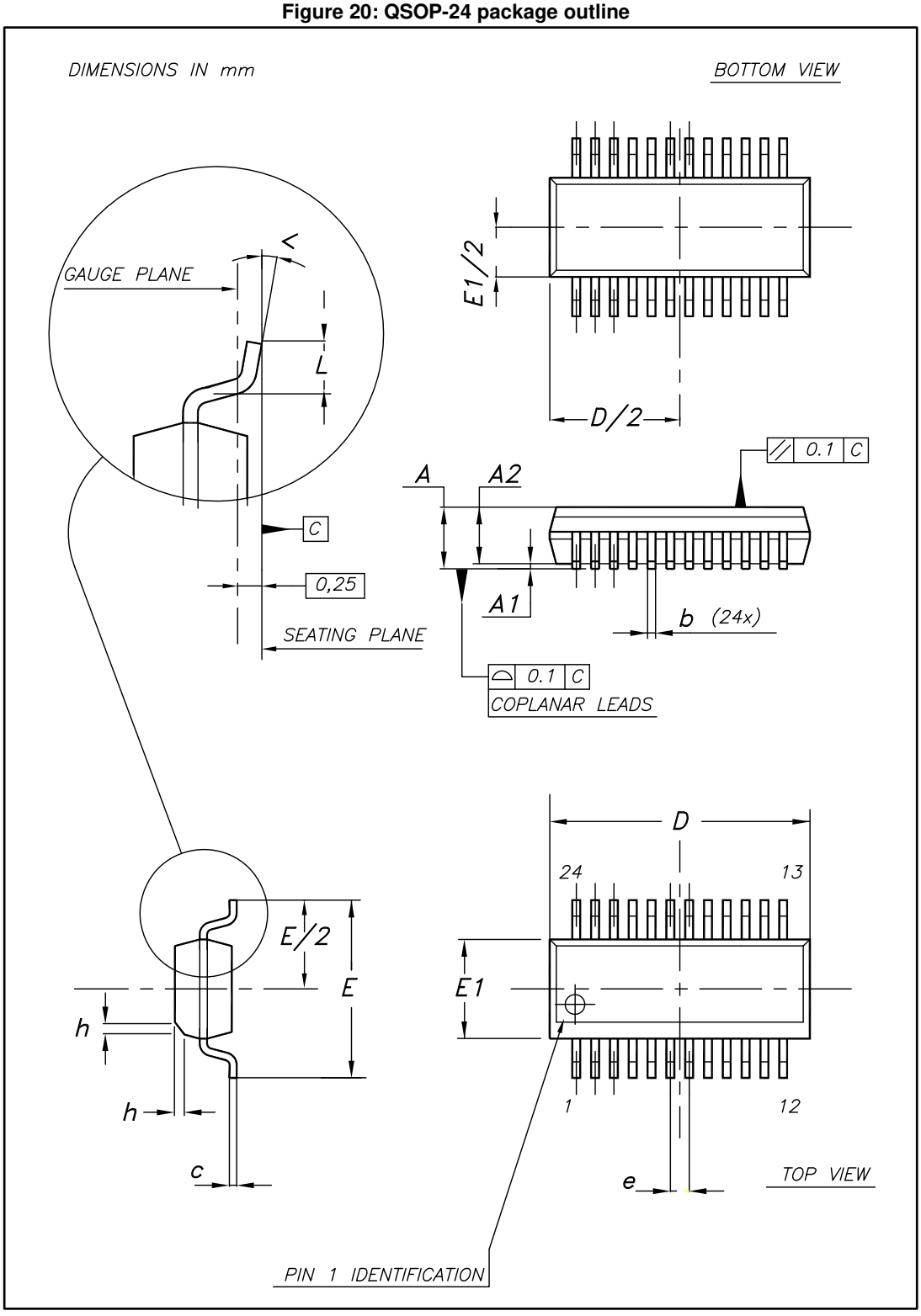


Table 12: QSOP-24 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	1.54	1.62	1.73
A1	0.10	0.15	0.25
A2		1.47	
b	0.20		0.31
c	0.17		0.254
D	8.56	8.66	8.76
E	5.80	6.00	6.20
E1	3.80	3.91	4.01
e		0.635	
L	0.40	0.635	0.89
h	0.25	0.33	0.41
<	0°		8°

8.2 SO-24 package information

Figure 21: SO-24 package outline

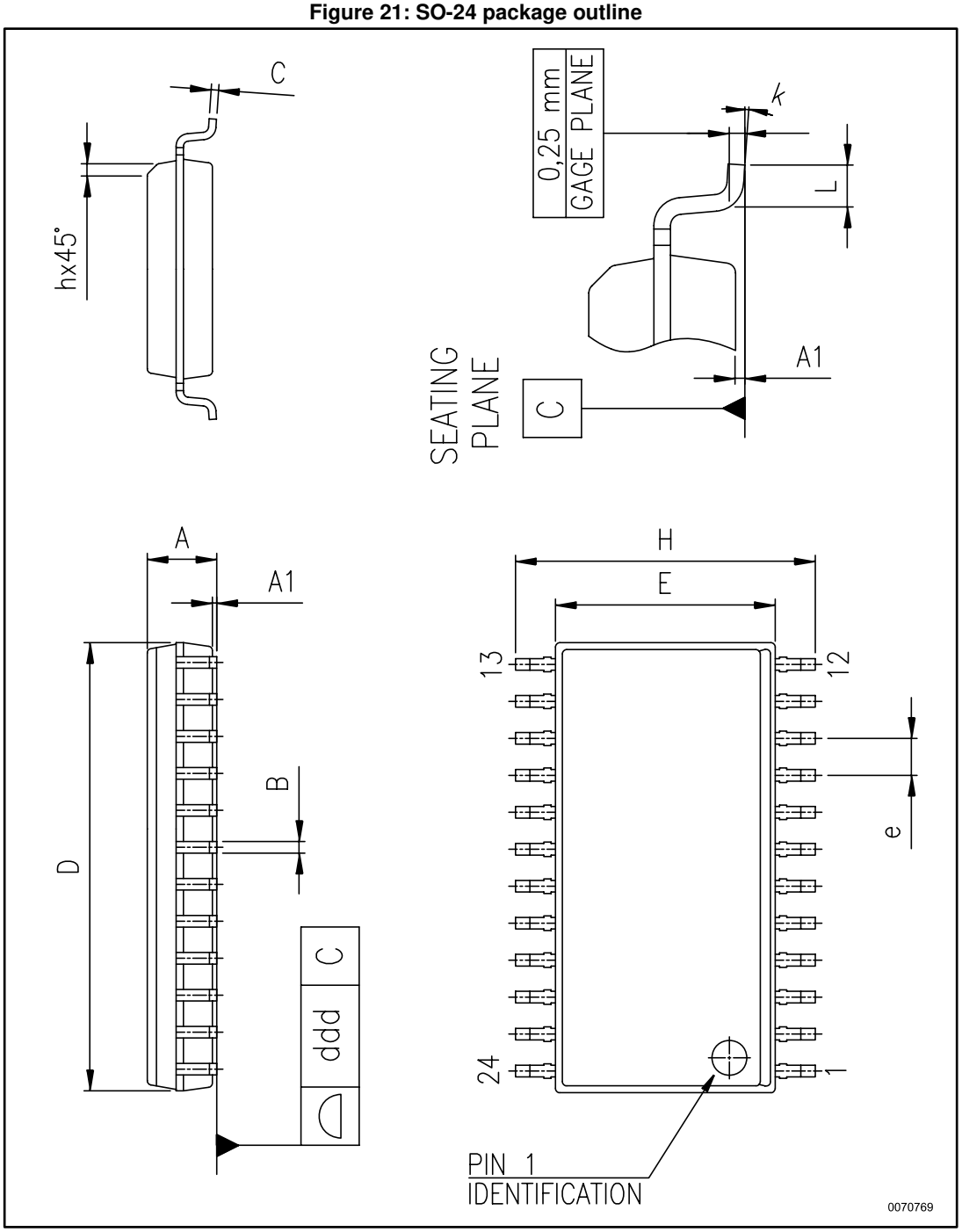


Table 13: SO-24 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.35		2.65
A1	0.10		0.30
B	0.33		0.51
C	0.23		0.32
D	15.20		15.60
E	7.40		7.60
e		1.27	
H	10.00		10.65
h	0.25		0.75
L	0.40		1.27
k	0		8
ddd			0.10

8.3 TSSOP24 package information

Figure 22: TSSOP24 package outline

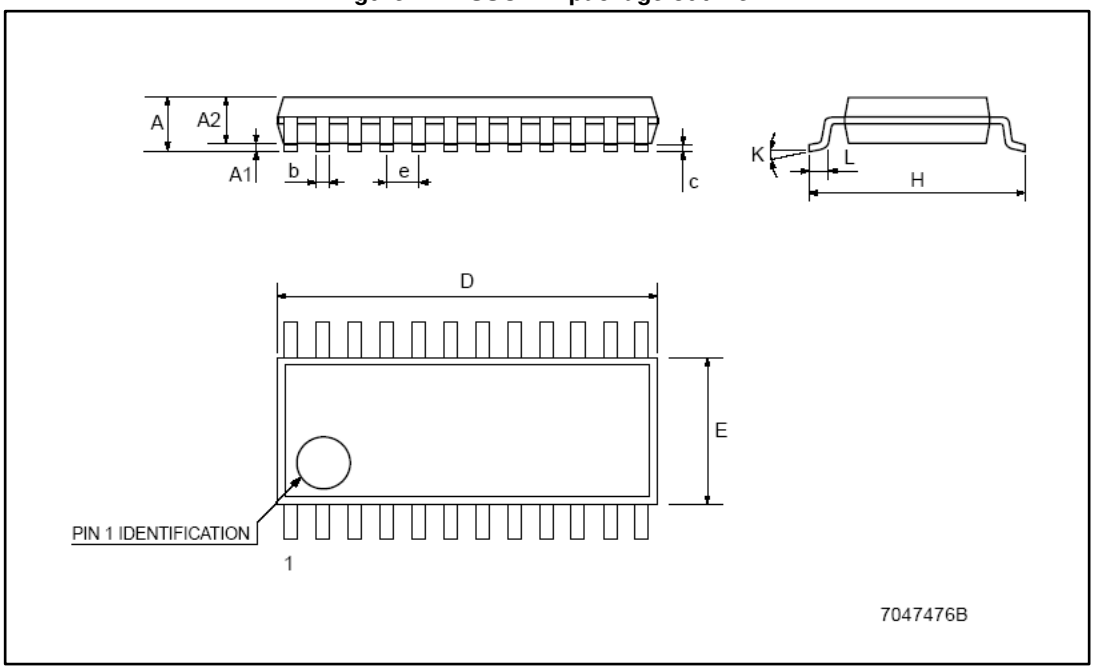


Table 14: TSSOP24 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.1
A1	0.05		0.15
A2		0.9	
b	0.19		0.30
c	0.09		0.20
D	7.7		7.9
E	4.3		4.5
e		0.65 BSC	
H	6.25		6.5
K	0°		8°
L	0.50		0.70

8.4 TSSOP24 exposed pad package information

Figure 23: TSSOP24 exposed pad package outline