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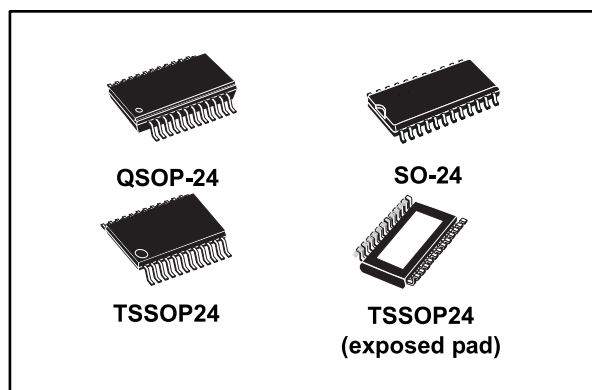
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## Low voltage 16-bit constant current LED sink driver with auto power-saving

Datasheet - production data



### Description

The STP16CPPS05 is a monolithic, low voltage, low current power 16-bit shift register designed for LED panel displays. The device features a 16-bit serial-in, parallel-out shift register that feeds a 16-bit D-type storage register. In the output stage, sixteen regulated current sources are designed to provide 3 to 40 mA of constant current to drive the LEDs.

The STP16CPPS05 output current can be adjusted through an external resistor to control the light intensity of the LEDs. LED brightness is adjustable from 0% to 100% via the  $\overline{\text{OE}}$  pin.

The auto power-shutdown and auto power-ON feature allows the device to save power with no external intervention.

The STP16CPPS05 guarantees a 20 V output driving capability, allowing users to connect more LEDs in series. The high 30 MHz clock frequency makes the device suitable for high data rate transmission. The 3.3 V supply is well suited for applications which interface a 3.3 V MCU. Compared to a standard TSSOP package, the TSSOP with exposed pad increases heat dissipation capability by a factor of 2.5.

### Features

- Low voltage power supply down to 3 V
- 16 constant current output channels
- Adjustable output current through external resistor
- Serial data IN/parallel data OUT
- Auto power-saving
- 3.3 V MCU-driving capability
- Output current: 3 to 40 mA
- 30 MHz clock frequency
- Available in high thermal efficiency TSSOP exposed pad
- ESD protection: 2 kV HBM, 200 V MM

Table 1: Device summary

Order code	Package	Packing
STP16CPPS05MTR	SO-24	1000 parts per reel
STP16CPPS05TTR	TSSOP24	2500 parts per reel
STP16CPPS05XTTR	TSSOP24 exposed pad	2500 parts per reel
STP16CPPS05PTR	QSOP-24	2500 parts per reel

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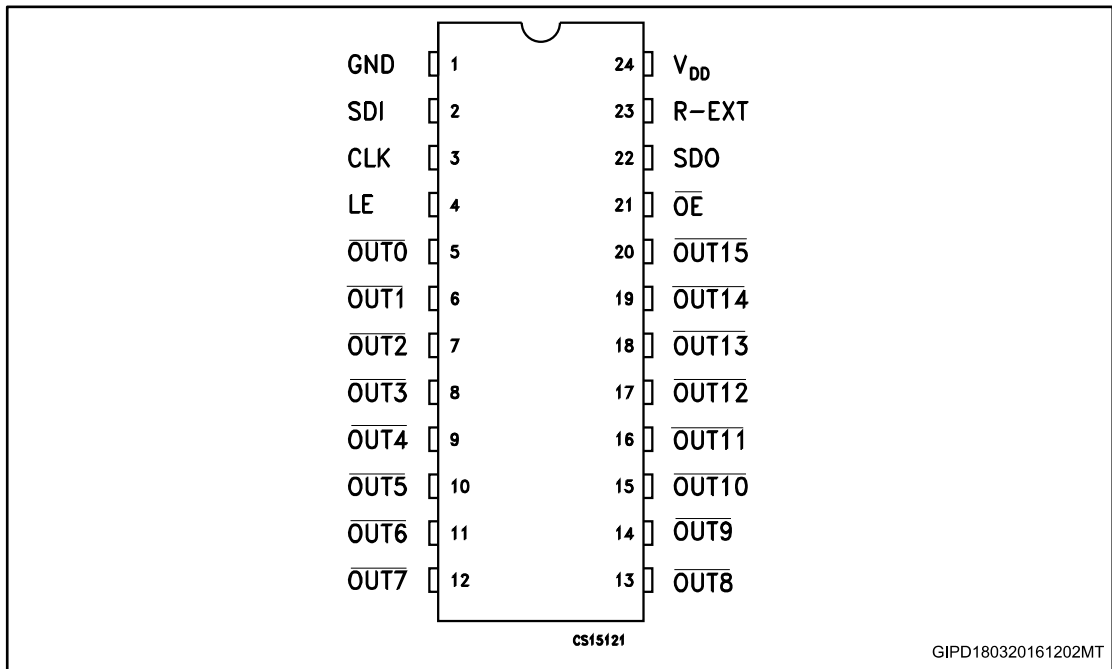
# 1 Summary description

Table 2: Typical current accuracy

Output voltage	Current accuracy		Output current	V <sub>DD</sub>	Temperature
	Between bits	Between ICs			
≥ 1.3 V	± 1%	± 2%	5 to 40 mA	3.3 V to 5 V	25 °C

## 1.1 Pin connection and description

Figure 1: Pin connection



The exposed pad should be electrically connected to a metal land electrically isolated or connected to ground.

Table 3: Pin description

Pin n°	Symbol	Name and function
1	GND	Ground terminal
2	SDI	Serial data input terminal
3	CLK	Clock input terminal
4	LE	Latch input terminal - detect mode 1 (see operation principle)
5-20	OUT 0-15	Output terminal
21	$\overline{\text{OE}}$	Input terminal of output enable (active low) - detect mode 1 (see operation principle)
22	SDO	Serial data out terminal
23	R-EXT	Input terminal for an external resistor for constant current programming
24	V <sub>DD</sub>	Supply voltage terminal

## 2 Electrical ratings

### 2.1 Absolute maximum ratings

Stressing the device above the ratings listed in the “absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other condition above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Table 4: Absolute maximum ratings**

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	Supply voltage	0 to 7	V
V <sub>O</sub>	Output voltage	-0.5 to 20	V
I <sub>O</sub>	Output current	50	mA
V <sub>I</sub>	Input voltage	-0.4 to V <sub>DD</sub>	V
I <sub>GND</sub>	GND terminal current	800	mA
f <sub>CLK</sub>	Clock frequency	50	MHz
T <sub>J</sub>	Junction temperature range <sup>(1)</sup>	-40 to +170	°C

**Notes:**

<sup>(1)</sup> Such absolute value is based on the thermal shutdown protection.

### 2.2 Thermal data

**Table 5: Thermal data**

Symbol	Parameter	Value	Unit	
T <sub>A</sub>	Operating free-air temperature range	-40 to +125	°C	
T <sub>J-OPR</sub>	Operating thermal junction temperature range	-40 to +150	°C	
T <sub>STG</sub>	Storage temperature range	-55 to +150	°C	
R <sub>thJA</sub>	Thermal resistance junction-ambient <sup>(1)</sup>	SO-24	42.7	°C/W
		TSSOP24	55	°C/W
		TSSOP24 <sup>(2)</sup> exposed pad	37.5	°C/W
		QSOP-24	55	°C/W

**Notes:**

<sup>(1)</sup> According with JEDEC standard 51-7B.

<sup>(2)</sup> The exposed pad should be soldered directly to the PCB to realize the thermal benefits.

## 2.3 Recommended operating conditions

Table 6: Recommended operating conditions

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>DD</sub>	Supply voltage		3.0		5.5	V
V <sub>O</sub>	Output voltage				20	V
I <sub>O</sub>	Output current	OUTn	3		40	mA
I <sub>OH</sub>	Output current	SERIAL-OUT			+1	mA
I <sub>OL</sub>	Output current	SERIAL-OUT			-1	mA
V <sub>IH</sub>	Input voltage		0.7 V <sub>DD</sub>		V <sub>DD</sub>	V
V <sub>IL</sub>	Input voltage		-0.3		0.3 V <sub>DD</sub>	V
t <sub>wLAT</sub>	LE pulse width	V <sub>DD</sub> = 3.0 V to 5.0 V	20			ns
t <sub>wCLK</sub>	CLK pulse width		10			ns
t <sub>wEN</sub>	$\overline{\text{OE}}$ pulse width		100			ns
t <sub>SETUP(D)</sub>	Setup time for DATA		8			ns
t <sub>HOLD(D)</sub>	Hold time for DATA		5			ns
t <sub>SETUP(L)</sub>	Setup time for LATCH		8			ns
f <sub>CLK</sub>	Clock frequency		Cascade operation <sup>(1)</sup>			30

**Notes:**

<sup>(1)</sup> If the device is connected in cascade, it may not be possible to achieve the maximum data transfer. Please consider the timings carefully.

### 3 Electrical characteristics

$V_{DD} = 3.3 \text{ V}$  to  $5 \text{ V}$ ,  $T_A = 25 \text{ }^\circ\text{C}$ , unless otherwise specified.

**Table 7: Electrical characteristics**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{IH}$	Input voltage high level		$0.7 V_{DD}$		$V_{DD}$	V
$V_{IL}$	Input voltage low level		GND		$0.3 V_{DD}$	V
$I_{OH}$	Output leakage current	$V_{OH} = 20 \text{ V}$			1	$\mu\text{A}$
$V_{OL}$	Output voltage (serial-OUT)	$I_{OL} = 1 \text{ mA}$			0.4	V
$V_{OH}$	Output voltage (serial-OUT)	$I_{OH} = -1 \text{ mA}$	$V_{DD}-0.4\text{V}$			V
$I_{OL1}$	Output current	$V_O = 0.3 \text{ V}$ , $R_{ext} = 4 \text{ k}\Omega$	4.75	5	5.25	mA
$I_{OL2}$		$V_O = 0.3 \text{ V}$ , $R_{ext} = 1 \text{ k}\Omega$	19	20	20	
$I_{OL3}$		$V_O = 1.3 \text{ V}$ , $R_{ext} = 497 \text{ }\Omega$	38	40	42	
$\Delta I_{OL1}$	Output current error between bit (all output ON)	$V_O = 0.3 \text{ V}$ , $I_O = 5 \text{ mA}$ , $R_{ext} = 4 \text{ k}\Omega$		$\pm 1$	$\pm 5$	%
$\Delta I_{OL2}$		$V_O = 0.3 \text{ V}$ , $I_O = 20 \text{ mA}$ , $R_{ext} = 980 \text{ }\Omega$		$\pm 0.5$	$\pm 3$	
$\Delta I_{OL3}$		$V_O = 1.3 \text{ V}$ , $I_O = 40 \text{ mA}$ , $R_{ext} = 490 \text{ }\Omega$		$\pm 0.5$	$\pm 3$	
$R_{SIN(up)}$	Pull-up resistor		150	300	600	$\text{k}\Omega$
$R_{SIN(down)}$	Pull-down resistor		100	200	400	$\text{k}\Omega$
$I_{DD(OFF1)}$	Supply current (OFF)	$R_{EXT} = 1 \text{ k}\Omega$ , $I_{OUT} = 20 \text{ mA}$ , OUT 0 to 15 = OFF		5.4	7.5	mA
$I_{DD(OFF2)}$		$R_{EXT} = 497 \text{ }\Omega$ , $I_{OUT} = 40 \text{ mA}$ , OUT 0 to 15 = OFF		8.0	9.5	
$I_{DD(ON1)}$	Supply current (ON)	$R_{EXT} = 1 \text{ k}\Omega$ , $I_{OUT} = 20 \text{ mA}$ , OUT 0 to 15 = ON		5.5	7.5	
$I_{DD(ON2)}$		$R_{EXT} = 497 \text{ }\Omega$ , $I_{OUT} = 40 \text{ mA}$ , OUT 0 to 15 = ON		8.1	9.5	
$I_{DD(SH)}$	Shut-down current all latched data = L	$V_{DD} = 3.3 \text{ V}$		160	200	$\mu\text{A}$
		$V_{DD} = 5 \text{ V}$		190	240	
Thermal	Thermal protection			170		$^\circ\text{C}$

$V_{DD} = 3.3\text{ V to }5\text{ V}$ ,  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified.

Table 8: Switching characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	
$t_{PLH1}$	Propagation delay time, CLK- $\overline{\text{OUTn}}$ , LE = H, $\overline{\text{OE}} = \text{L}$		$V_{DD} = 3.3\text{ V}$	-	53.5	86.5	ns
			$V_{DD} = 5\text{ V}$	-	32	46.5	
$t_{PLH2}$	Propagation delay time, LE- $\overline{\text{OUTn}}$ , $\overline{\text{OE}} = \text{L}$		$V_{DD} = 3.3\text{ V}$	-	48	75.5	ns
			$V_{DD} = 5\text{ V}$	-	30	43	
$t_{PLH3}$	Propagation delay time, $\overline{\text{OE}} - \overline{\text{OUTn}}$ , LE = H		$V_{DD} = 3.3\text{ V}$	-	71.5	118	ns
			$V_{DD} = 5\text{ V}$	-	43	62	
$t_{PLH}$	Propagation delay time, CLK-SDO		$V_{DD} = 3.3\text{ V}$	15	21	31	ns
			$V_{DD} = 5\text{ V}$	11	15	21	
$t_{PHL1}$	Propagation delay time, CLK- $\overline{\text{OUTn}}$ , LE = H, $\overline{\text{OE}} = \text{L}$	$V_{IH} = V_{DD}$ $V_{IL} = \text{GND}$ $C_L = 10\text{ pF}$ $I_O = 20\text{ mA}$ $V_L = 3.0\text{ V}$ $R_{ext} = 1\text{ K}\Omega$ $R_L = 60\text{ }\Omega$	$V_{DD} = 3.3\text{ V}$	-	27.5	39	ns
			$V_{DD} = 5\text{ V}$	-	22	30.5	
$t_{PHL2}$	Propagation delay time, LE- $\overline{\text{OUTn}}$ , $\overline{\text{OE}} = \text{L}$		$V_{DD} = 3.3\text{ V}$	-	11.5	17.5	ns
			$V_{DD} = 5\text{ V}$	-	8	11.5	
$t_{PHL3}$	Propagation delay time, $\overline{\text{OE}} - \overline{\text{OUTn}}$ , LE = H		$V_{DD} = 3.3\text{ V}$	-	24	33.5	ns
			$V_{DD} = 5\text{ V}$	-	21	28.5	
$t_{PHL}$	Propagation delay time, CLK-SDO		$V_{DD} = 3.3\text{ V}$	17.5	24	36	ns
			$V_{DD} = 5\text{ V}$	12.5	17	25	
$t_{ON}$	Output rise time 10~90% of voltage waveform		$V_{DD} = 3.3\text{ V}$	-	29	54	ns
			$V_{DD} = 5\text{ V}$	-	10	17	
$t_{OFF}$	Output fall time 90~10% of voltage waveform		$V_{DD} = 3.3\text{ V}$	-	4.5	6	ns
			$V_{DD} = 5\text{ V}$	-	3.5	5	
$t_r$	CLK rise time <sup>(1)</sup>		-		5000	ns	
$t_f$	CLK fall time <sup>(1)</sup>		-		5000	ns	

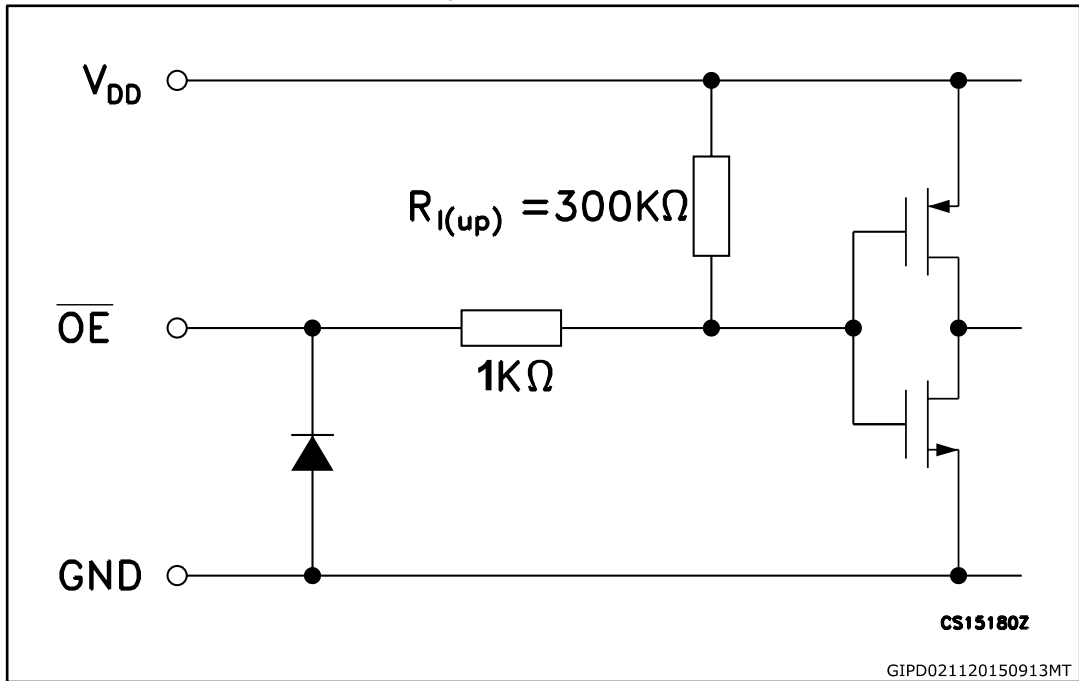
**Notes:**

<sup>(1)</sup> In order to achieve high cascade data transfer, please consider  $t_r/t_f$  timings carefully.



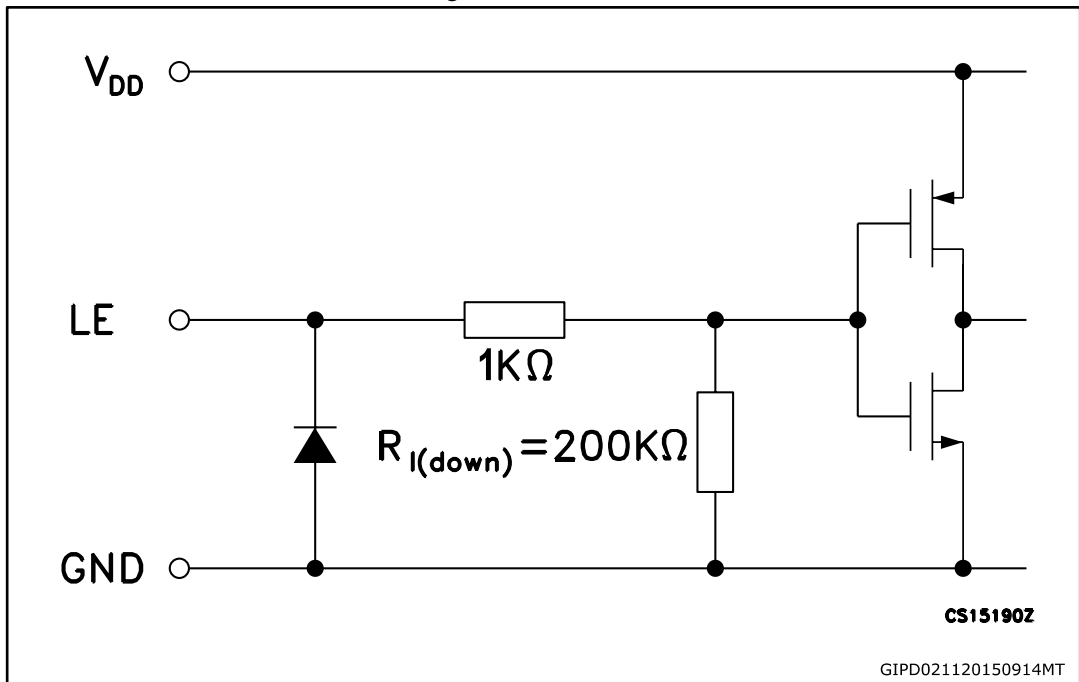
### 4 Equivalent circuit and outputs

Figure 2: OE terminal



GIPD021120150913MT

Figure 3: LE terminal



GIPD021120150914MT

Figure 4: CLK, SDI terminal

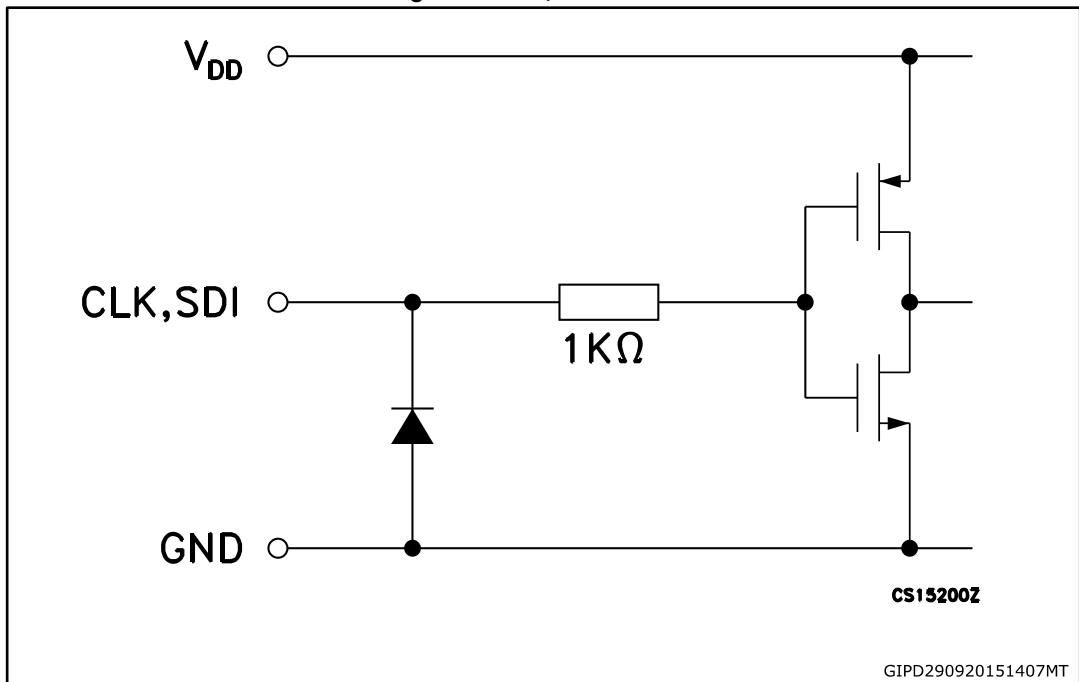


Figure 5: SDO terminal

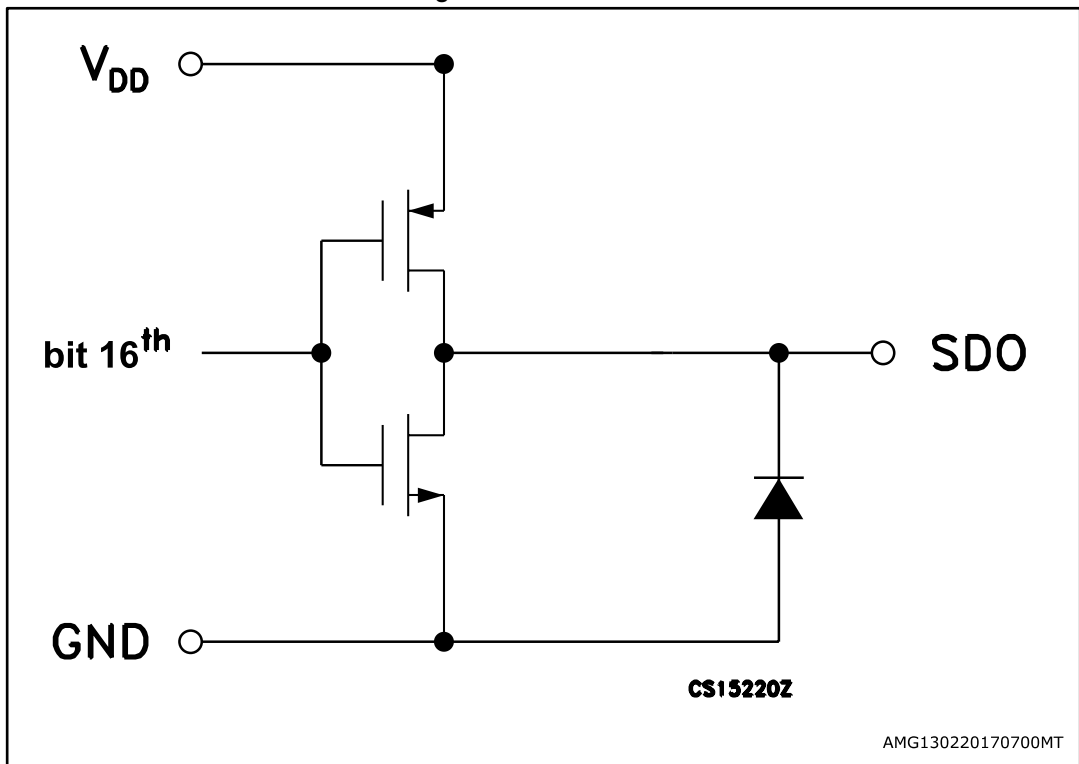
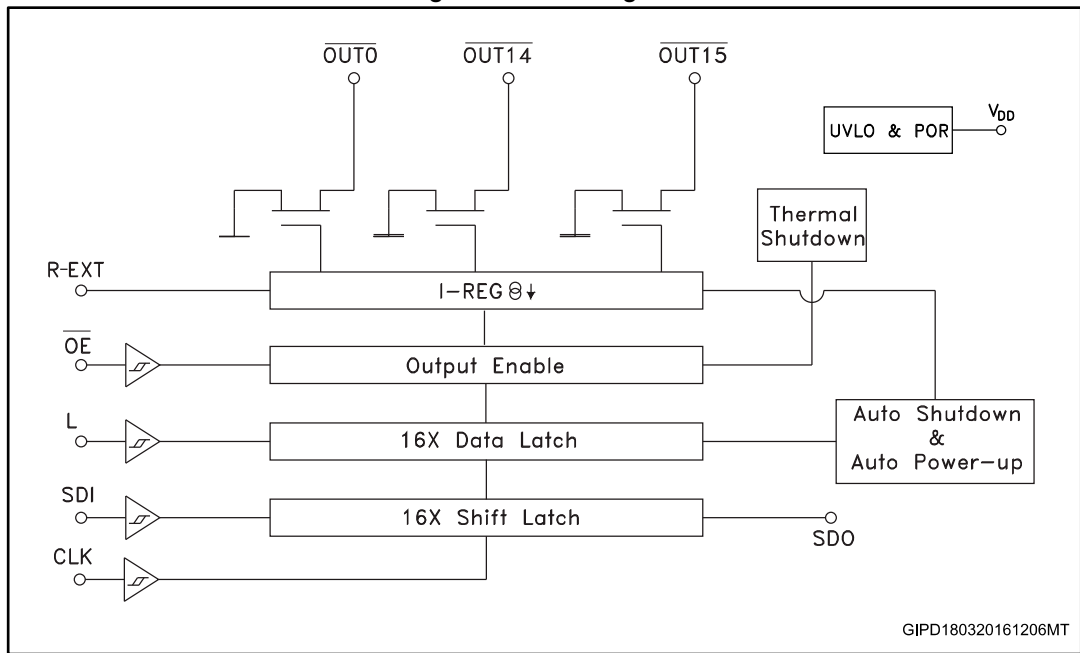


Figure 6: Block diagram



# 5 Timing diagrams

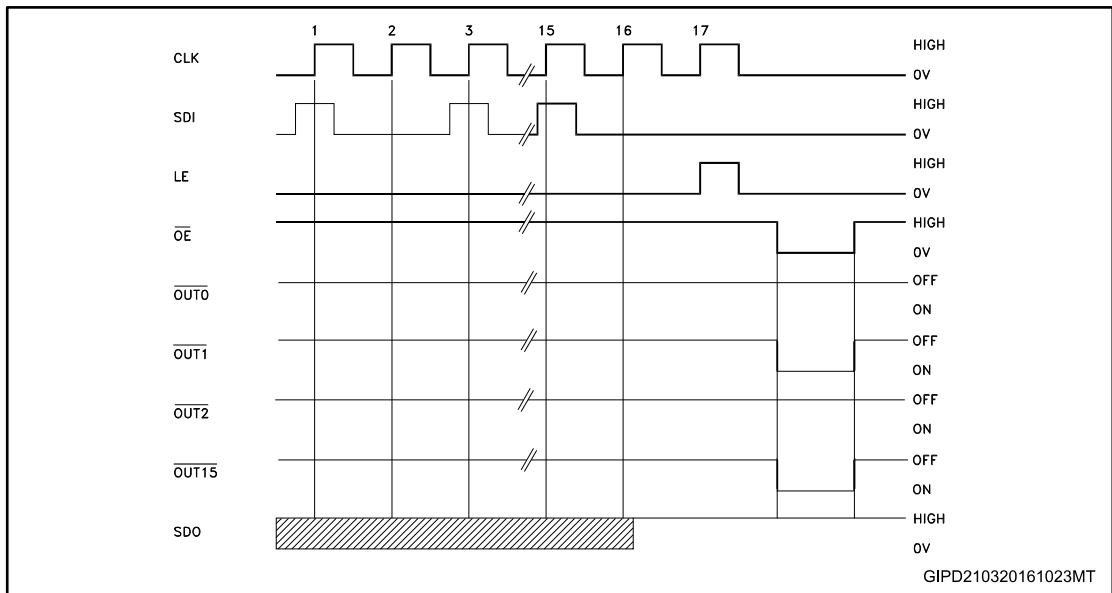
Table 9: Truth table

CLOCK	LE	$\overline{OE}$	SERIAL-IN	$\overline{OUT0}$ ..... $\overline{OUT7}$ ..... $\overline{OUT15}$	SDO
	H	L	Dn	Dn ..... Dn - 7 ..... Dn - 15	Dn - 15
	L	L	Dn + 1	No change	Dn - 14
	H	L	Dn + 2	Dn + 2 ..... Dn - 5 ..... Dn - 13	Dn - 13
	X	L	Dn + 3	Dn + 2 ..... Dn - 5 ..... Dn - 13	Dn - 13
	X	H	Dn + 3	OFF	Dn - 13



OUTn = ON when Dn = H OUTn = OFF when Dn = L.

Figure 7: Timing diagram



1 Latch and output enable terminals are level-sensitive and are not synchronized with rising or falling edge of CLK signal.

2 When LE terminal is low level, the latch circuit holds previous set of data.

3 When LE terminal is high level, the latch circuit refreshes new set of data from SDI chain.

4 When  $\overline{OE}$  terminal is at low level, the output terminals Out 0 to Out 15 respond to data in the latch circuits, either '1' for ON or '0' for OFF.

5 When  $\overline{OE}$  terminal is at high level, all output terminals are switched OFF.

Table 10: Enable IO: shutdown truth table

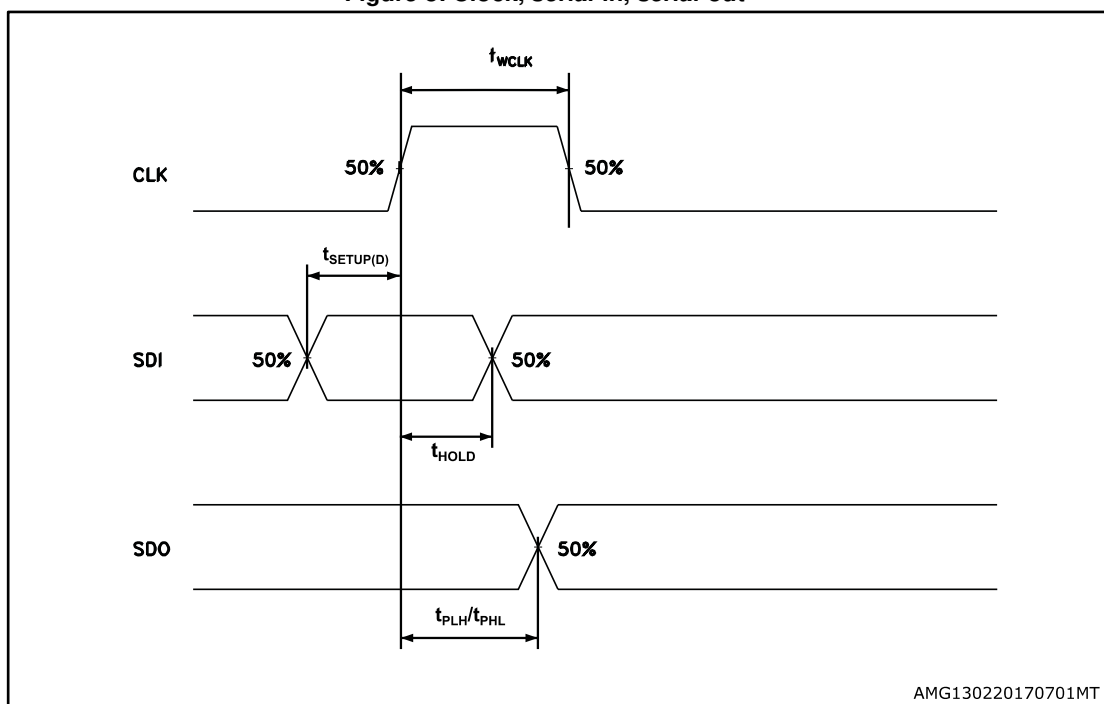
CLOCK	LE	SDI <sub>0</sub> ..... SDI <sub>7</sub> ..... SDI <sub>15</sub>	SH	Auto power-up	OUT <sub>n</sub>
	H	All = L	Active	Not active <sup>(1)</sup>	OFF
	L	No change	No change	No change	No change
	H	One or more = H	Not active	Active	X <sup>(2)</sup>

Notes:

<sup>(1)</sup> At power-up, the device starts in shutdown mode.

<sup>(2)</sup> Undefined.

Figure 8: Clock, serial-in, serial-out



AMG130220170701MT

Figure 9: Clock, serial-in, latch, enable, outputs

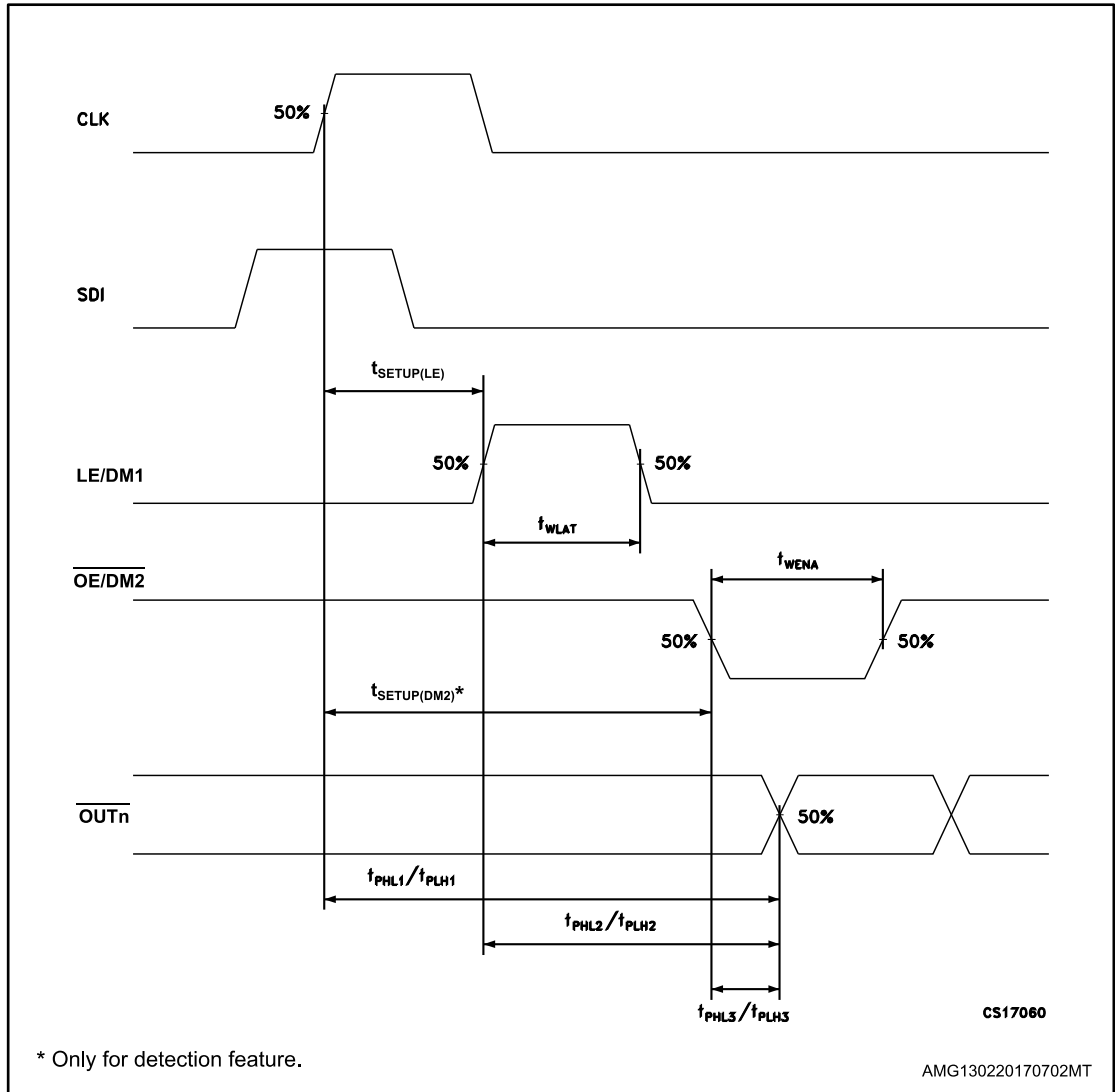
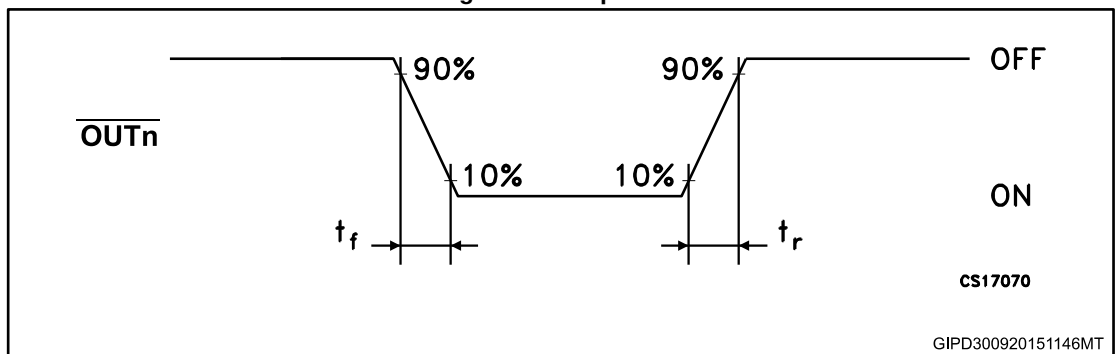


Figure 10: Outputs



## 6 Typical characteristics

Figure 11: Output current vs. R-EXT resistor

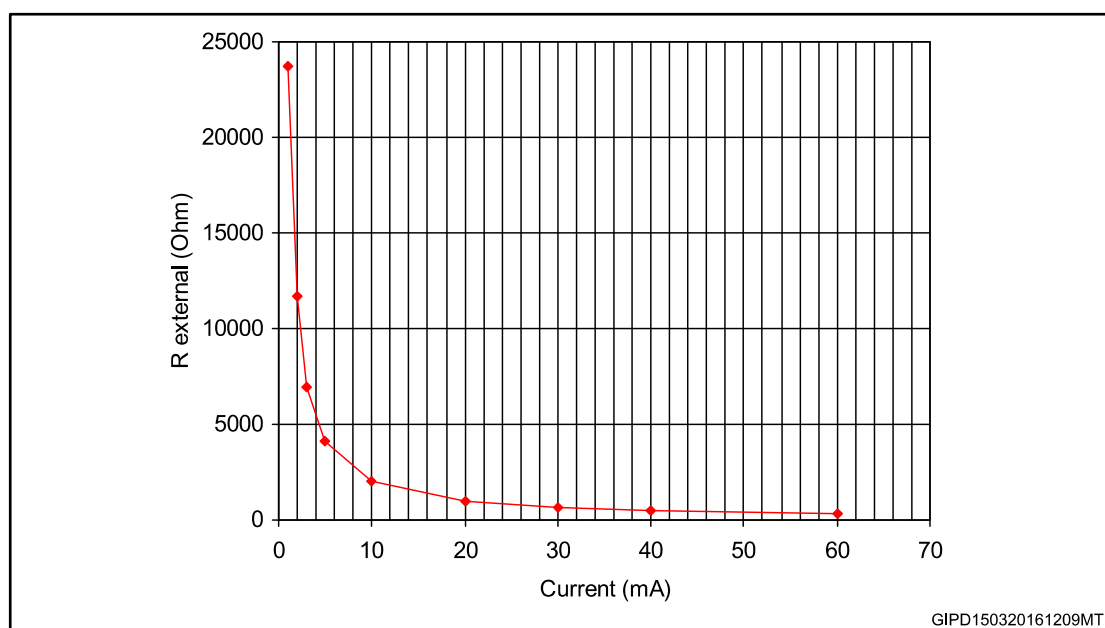


Table 11: Output current vs. R-EXT resistor

R-EXT (Ω)	Output current (mA)
23700	1
11730	2
6930	3
4090	5
2025	10
1000	20
667	30
497	40
331	60

Conditions:

Temperature = 25 °C,  $V_{DD} = 3.3\text{ V}; 5.0\text{ V}$ ,  $I_{SET} = 3\text{ mA}; 5\text{ mA}; 10\text{ mA}; 20\text{ mA}; 50\text{ mA}; 60\text{ mA}$ .

Figure 12:  $I_{SET}$  vs drop out voltage ( $V_{drop}$ )

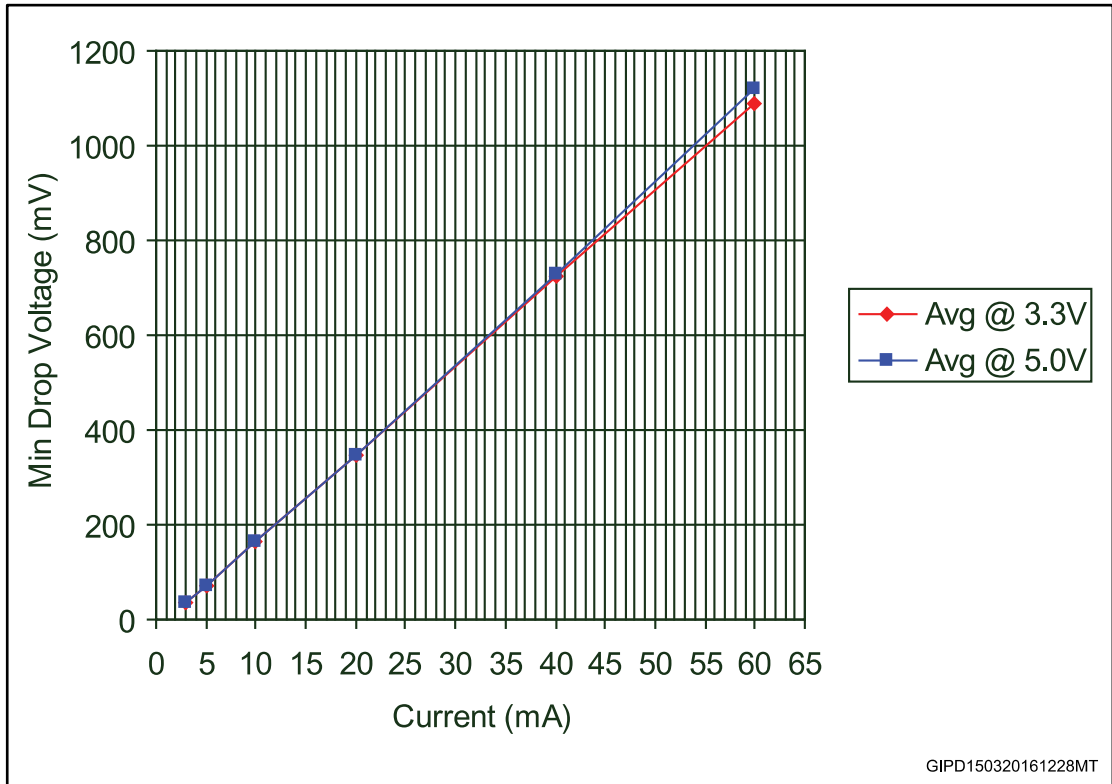


Table 12:  $I_{SET}$  vs drop out voltage ( $V_{drop}$ )

$I_{out}$ (mA)	Avg (mV) @ 3.3 V	Avg (mV) @ 5.0 V
3	36	37
5	71	72
10	163	163
20	346	347
40	724	724
60	1080	1110



$T_A = 25\text{ }^\circ\text{C}$ ,  $V_{dd} = 3.3\text{ V}$ ;  $5\text{ V}$

Figure 13: Output current vs.  $\pm \Delta I_{OL}(\%)$

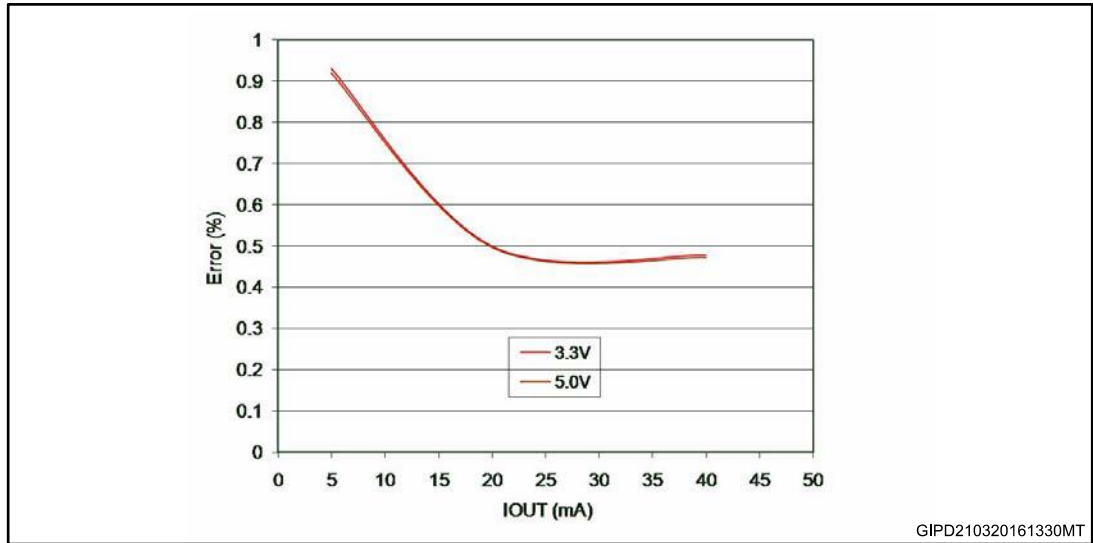


Figure 14: I<sub>dd</sub> ON/OFF

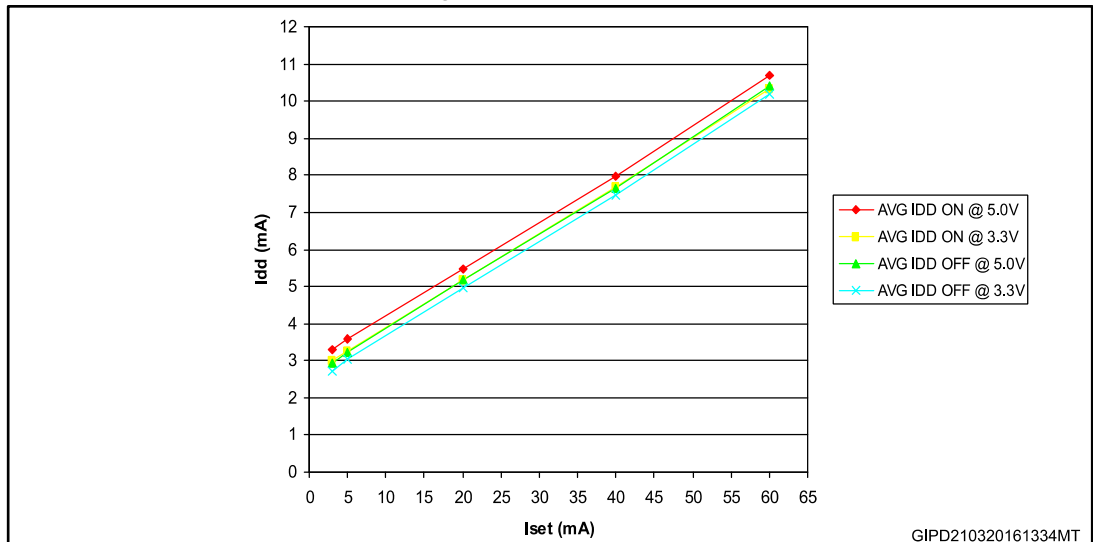
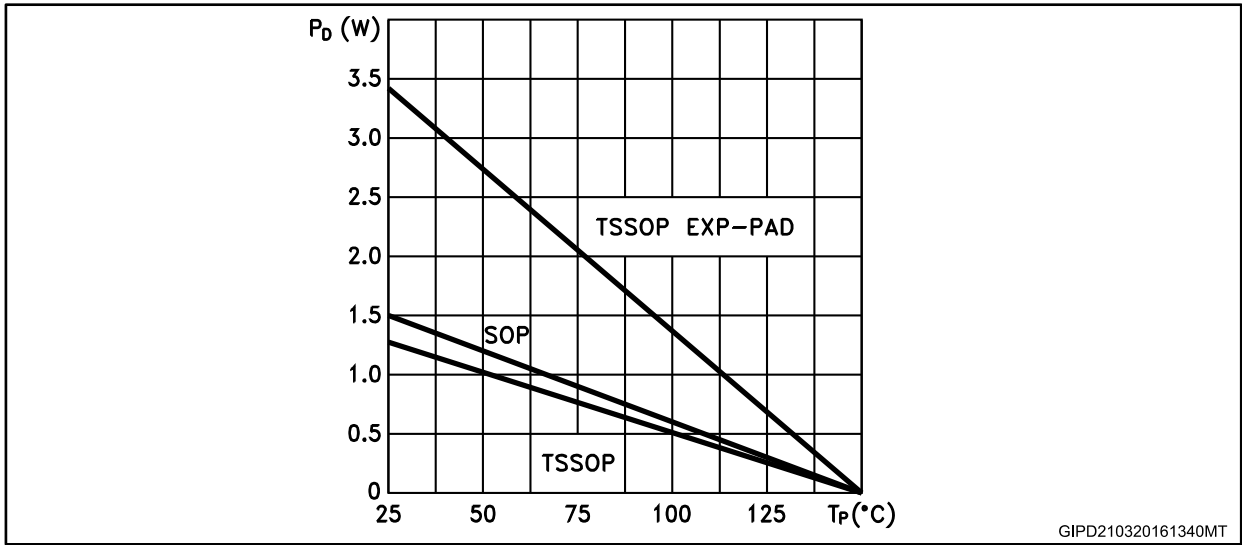


Figure 15: Power dissipation vs. package temperature



The exposed pad should be soldered to the PCB to obtain the thermal benefits.

Figure 16: Turn ON output current characteristics<sup>(1)</sup>



GIPD210320161342MT

Figure 17: Turn OFF output current characteristics<sup>(2)</sup>



GIPD210320161343MT

Notes:

(1) The reference level for the  $T_{ON}$  characteristics is 50% of  $\overline{OE}$  signal and 90% of output current.

(2) The reference level for the  $T_{OFF}$  characteristics is 50% of  $\overline{OE}$  signal and 10% of output current.

Electrical conditions:

Vdd = 3.3 V, Vin = Vdd, Vled = 3.0 V, RL = 60 Ω, CL = 10 pF

Ch1 (Yellow) =  $\overline{OE}$ , Ch2 (Blue) = CLK, Ch3 (Purple) = VOUT, Ch4 (Green) = OUT

## 7 Auto power-saving

The auto power-saving feature minimizes the quiescent current if no active data is detected on the latches and auto powers-up the device as the first active data is latched.

Figure 18: Auto power-saving feature



Electrical conditions:

Temp. = 25 °C, Vdd = 3.3 V, Vin = Vdd, Vled = 3.0 V, RL = 60 Ω, CL = 10 pF

Ch1 (Yellow) =  $\overline{OE}$ , Ch2 (Blue) = CLK, Ch3 (Purple) = LE, Ch4 (Green) =  $i_{DD}$

I<sub>DD</sub> consumption:

I<sub>DD</sub> (normal operation) = 4.2 mA

I<sub>DD</sub> (shut down condition) = 190 μA

Figure 19: First output ON after switching from auto power saving to normal operating condition



Electrical conditions:

temp. = 25 °C, Vdd = 3.3 V, Vin = Vdd, Vled = 3.0 V, Iset = 20 mA

Ch1 (Yellow) = SDI, Ch2 (Blue) = CLK, Ch3 (Purple) = LE, Ch4 (Green) = first output ON



When the device goes from AUTO power saving to normal operative condition, the first output that switch ON shows TON condition as seen in the plot above.

## 8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 8.1 QSOP-24 package information

Figure 20: QSOP-24 package outline

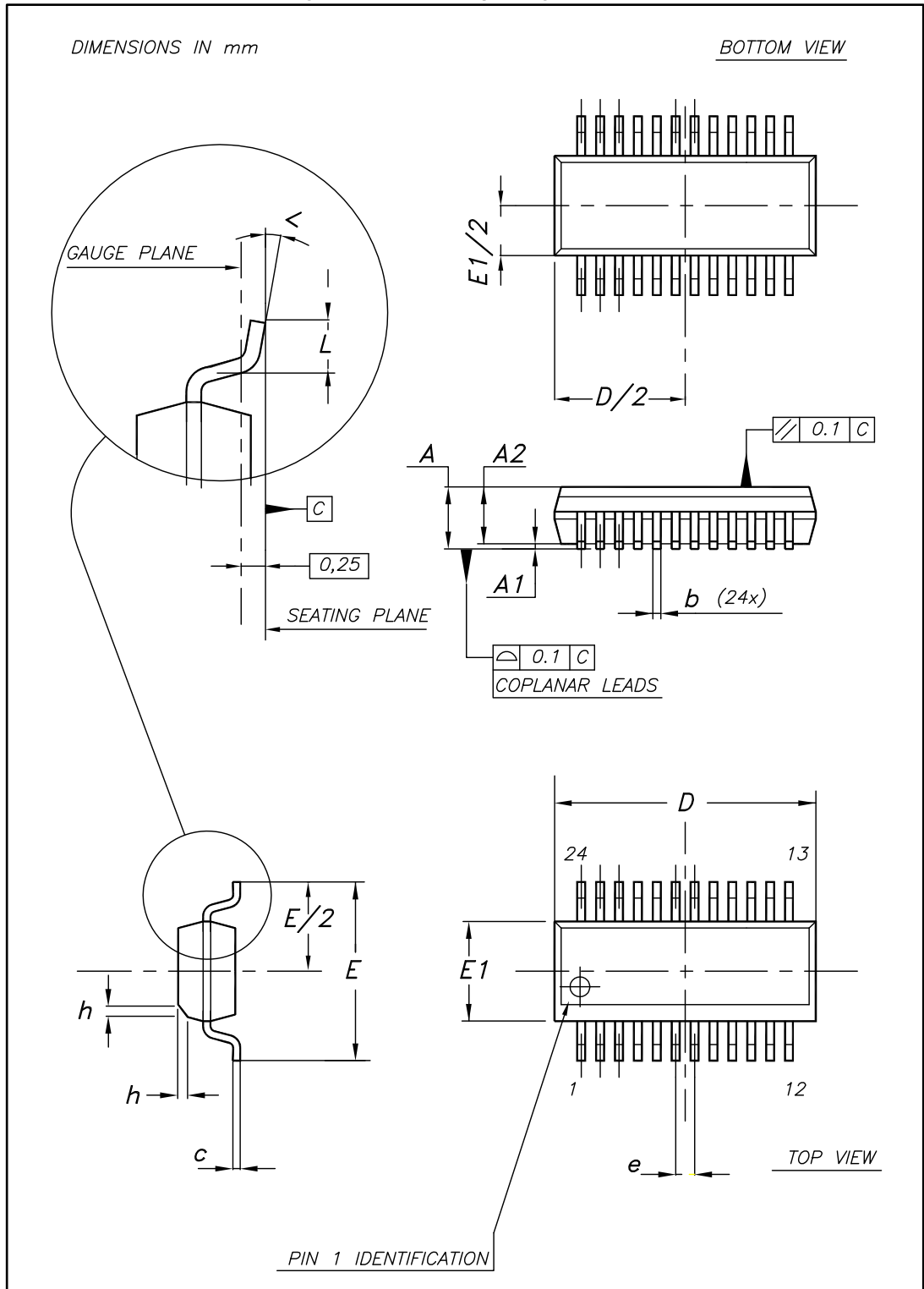


Table 13: QSOP-24 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	1.54	1.62	1.73
A1	0.10	0.15	0.25
A2		1.47	
b	0.20		0.31
c	0.17		0.254
D	8.56	8.66	8.76
E	5.80	6.00	6.20
E1	3.80	3.91	4.01
e		0.635	
L	0.40	0.635	0.89
h	0.25	0.33	0.41
<	0°		8°

### 8.2 SO-24 package information

Figure 21: SO-24 package outline

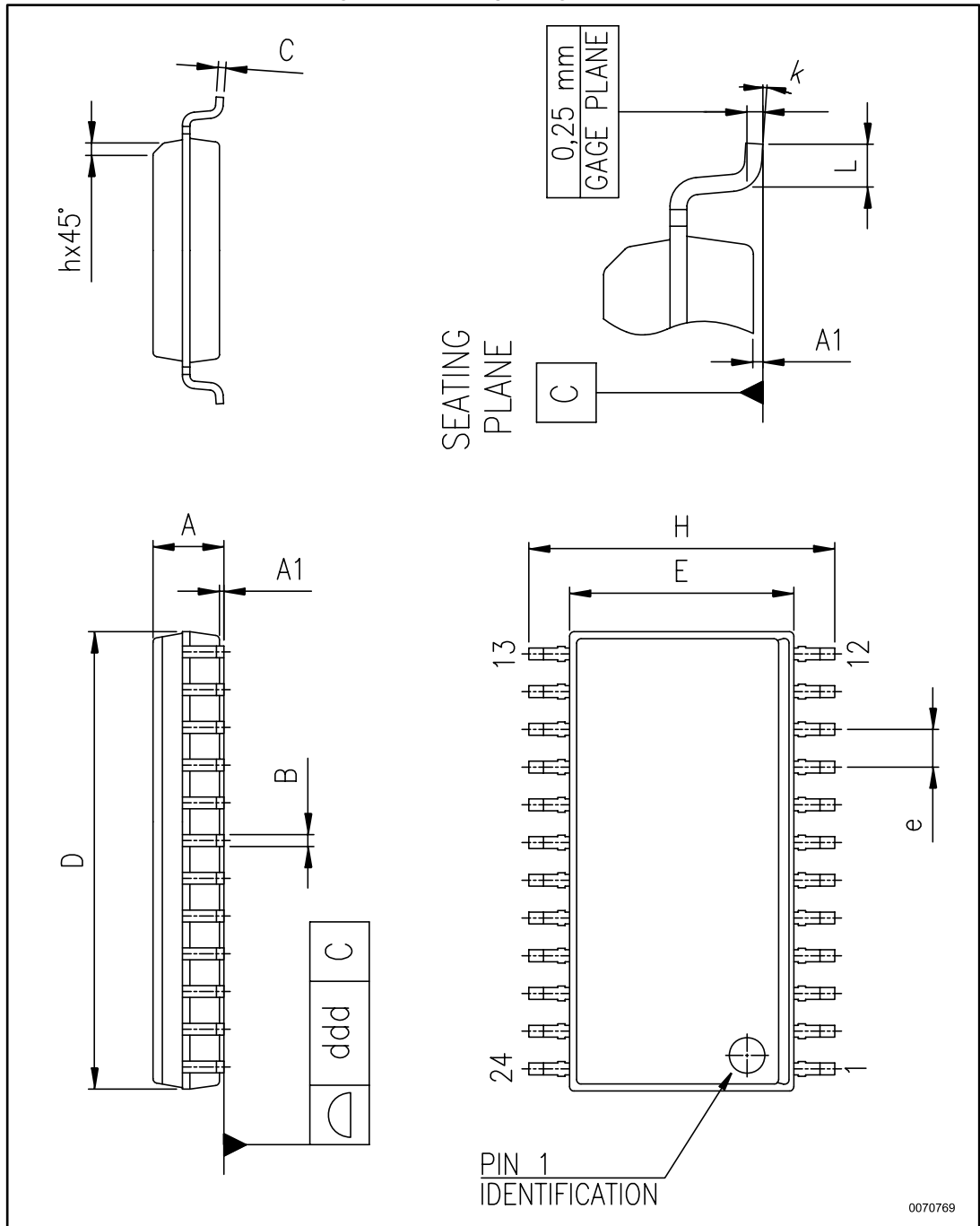


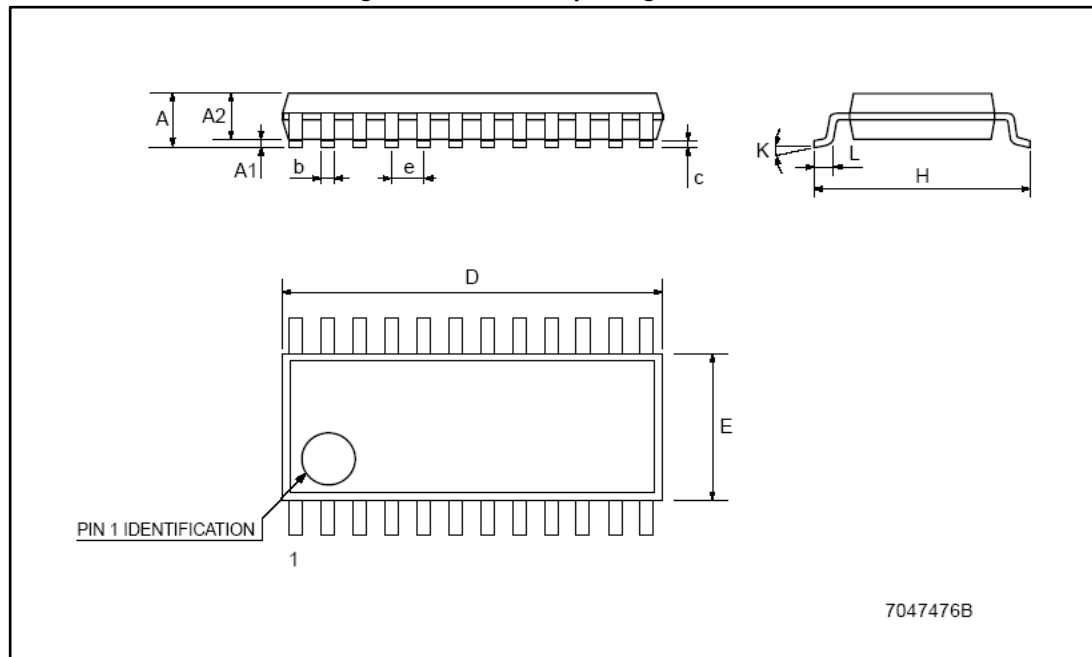


Table 14: SO-24 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.35		2.65
A1	0.10		0.30
B	0.33		0.51
C	0.23		0.32
D	15.20		15.60
E	7.40		7.60
e		1.27	
H	10.00		10.65
h	0.25		0.75
L	0.40		1.27
k	0		8
ddd			0.10

### 8.3 TSSOP24 package information

Figure 22: TSSOP24 package outline



7047476B

Table 15: TSSOP24 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.1
A1	0.05		0.15
A2		0.9	
b	0.19		0.30
c	0.09		0.20
D	7.7		7.9
E	4.3		4.5
e		0.65 BSC	
H	6.25		6.5
K	0°		8°
L	0.50		0.70