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N-channel 500 V, 0.24 Ω typ., 13 A MDmesh™ M2 Power MOSFETs in DPAK, TO-220FP and TO-220 packages

Datasheet - production data

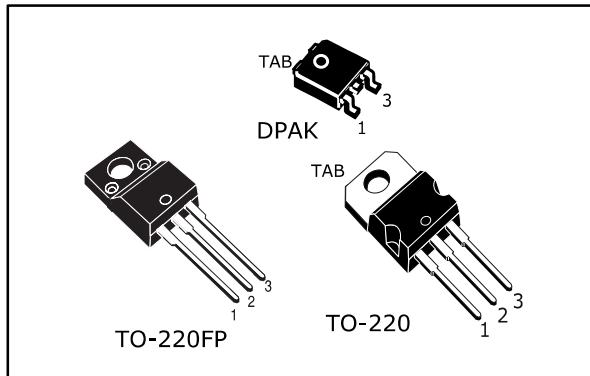
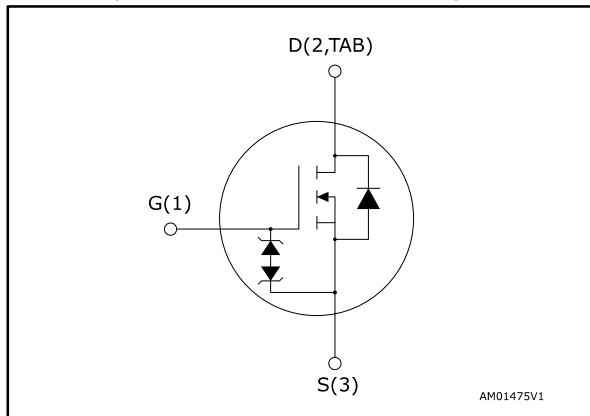


Figure 1: Internal schematic diagram



Features

Order code	V _{DS} @ T _{Jmax}	R _{DS(on)} max.	I _D
STD16N50M2	550 V	0.28 Ω	13 A
STF16N50M2			
STP16N50M2			

- Extremely low gate charge
- Excellent output capacitance (C_{oss}) profile
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

These devices are N-channel Power MOSFETs developed using MDmesh™ M2 technology. Thanks to their strip layout and improved vertical structure, these devices exhibit low on-resistance and optimized switching characteristics, rendering them suitable for the most demanding high efficiency converters.

Table 1: Device summary

Order code	Marking	Package	Packing
STD16N50M2	16N60M2	DPAK	Tape and reel
STF16N50M2		TO-220FP	
STP16N50M2		TO-220	Tube

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value			Unit
		DPAK	TO-220	TO-220FP	
V_{GS}	Gate-source voltage	± 25			V
I_D	Drain current (continuous) at $T_C = 25\text{ °C}$	13			A
I_D	Drain current (continuous) at $T_C = 100\text{ °C}$	8			A
$I_{DM}^{(1)}$	Drain current (pulsed)	52			A
P_{TOT}	Total dissipation at $T_C = 25\text{ °C}$	110	25		W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15			V/ns
$dv/dt^{(3)}$	MOSFET dv/dt ruggedness	50			V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink ($t = 1\text{ s}$, $T_C = 25\text{ °C}$)	2500			V
T_{stg}	Storage temperature range	- 55 to 150			°C
T_j	Operating junction temperature range				

Notes:

(1) Pulse width limited by safe operating area.

(2) $I_{SD} \leq 13\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$; $V_{DS\text{ peak}} < V_{(BR)DSS}$, $V_{DD} = 80\% V_{(BR)DSS}$

(3) $V_{DS} \leq 400\text{ V}$

Table 3: Thermal data

Symbol	Parameter	Value			Unit
		DPAK	TO-220	TO-220FP	
$R_{thj-case}$	Thermal resistance junction-case max.	1.14		5	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient max.	62.5			
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb max.	50			

Notes:

(1) When mounted on 1 inch² FR-4, 2 Oz copper board.

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetetive or not repetetive (pulse width limited by T_{jmax})	4	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25\text{ °C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	215	mJ

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified).

Table 5: On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	V _{GS} = 0 V, I _D = 1 mA	500			V
I _{DSS}	Zero gate voltage drain current	V _{GS} = 0 V, V _{DS} = 500 V			1	μA
		V _{GS} = 0 V, V _{DS} = 500 V, T _C = 125 °C ⁽¹⁾			100	μA
I _{GSS}	Gate-body leakage current	V _{DS} = 0 V, V _{GS} = ±25 V			±10	μA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	2	3	4	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 10 V, I _D = 6.5 A		0.24	0.28	Ω

Notes:

⁽¹⁾Defined by design, not subject to production test.

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = 100 V, f = 1 MHz, V _{GS} = 0 V	-	710	-	pF
C _{oss}	Output capacitance		-	44	-	pF
C _{rss}	Reverse transfer capacitance		-	1.35	-	pF
C _{oss eq.} ⁽¹⁾	Equivalent output capacitance	V _{DS} = 0 V to 400 V, V _{GS} = 0 V	-	192	-	pF
R _G	Intrinsic gate resistance	f = 1 MHz, I _D = 0 A	-	5.2	-	Ω
Q _g	Total gate charge	V _{DD} = 400 V, I _D = 13 A, V _{GS} = 10 V (see Figure 19: "Test circuit for gate charge behavior")	-	19.5	-	nC
Q _{gs}	Gate-source charge		-	4	-	nC
Q _{gd}	Gate-drain charge		-	8	-	nC

Notes:

⁽¹⁾ C_{oss eq.} is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 250 V, I _D = 6.5 A R _G = 4.7 Ω, V _{GS} = 10 V (see Figure 18: "Test circuit for resistive load switching times" and Figure 23: "Switching time waveform")	-	9.6	-	ns
t _r	Rise time		-	7.6	-	ns
t _{d(off)}	Turn-off-delay time		-	32	-	ns
t _f	Fall time		-	10	-	ns

Table 8: Source-drain diode

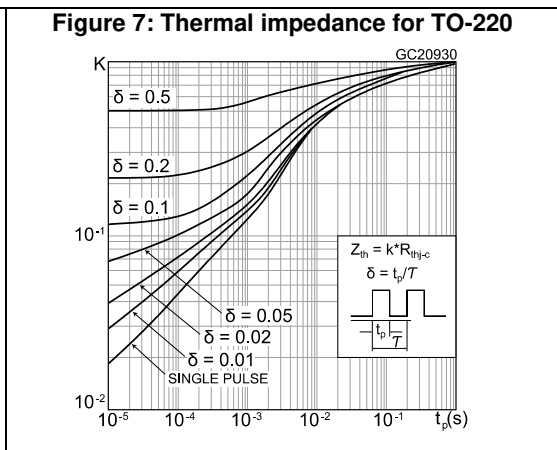
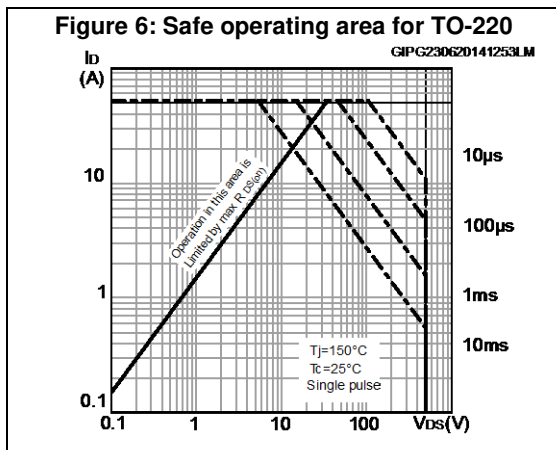
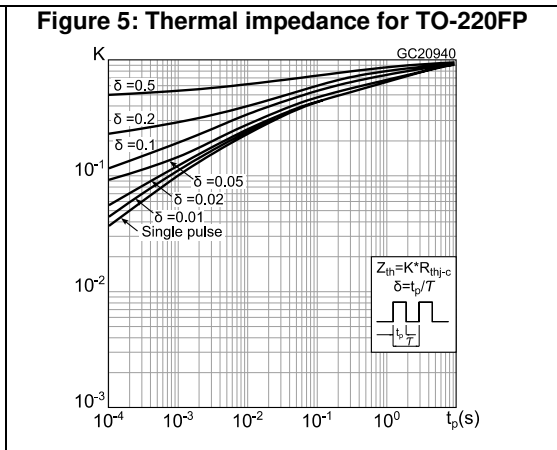
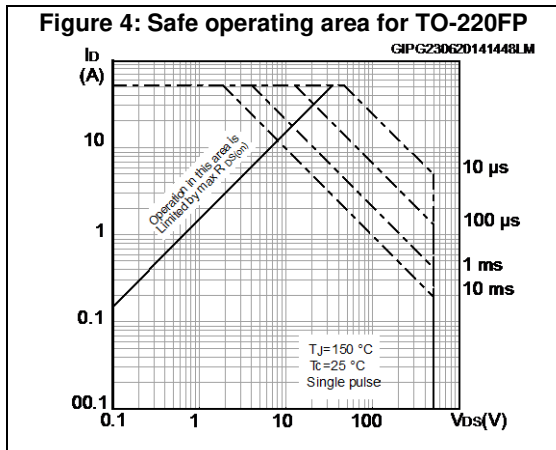
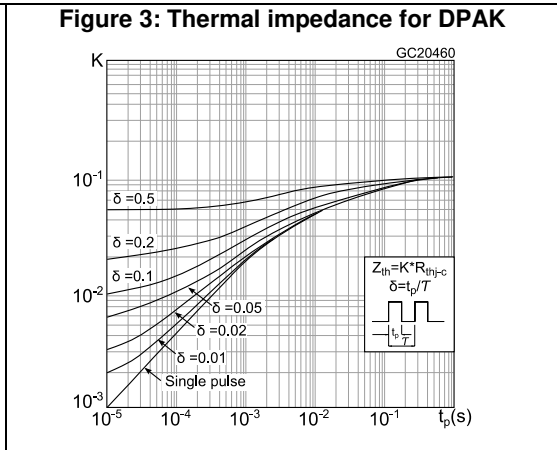
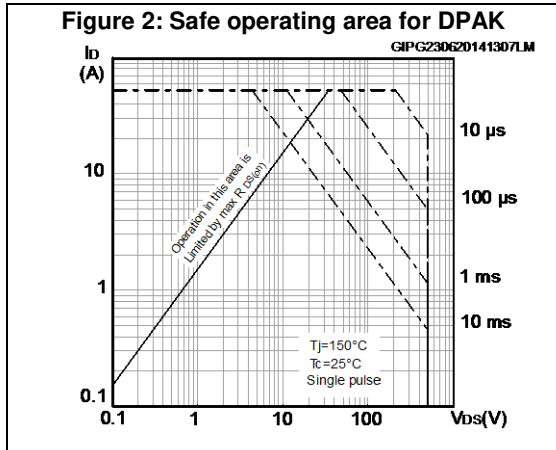
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		13	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		52	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 13\text{ A}$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 13\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$ (see Figure 20: "Test circuit for inductive load switching and diode recovery times")	-	280		ns
Q_{rr}	Reverse recovery charge		-	2.85		μC
I_{RRM}	Reverse recovery current		-	20.5		A
t_{rr}	Reverse recovery time	$I_{SD} = 13\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 20: "Test circuit for inductive load switching and diode recovery times")	-	388		ns
Q_{rr}	Reverse recovery charge		-	4.5		μC
I_{RRM}	Reverse recovery current		-	21		A

Notes:

(1)Pulse width is limited by safe operating area.

(2)Pulse test: pulse duration = 300 μs , duty cycle 1.5%.

2.2 Electrical characteristics (curves)



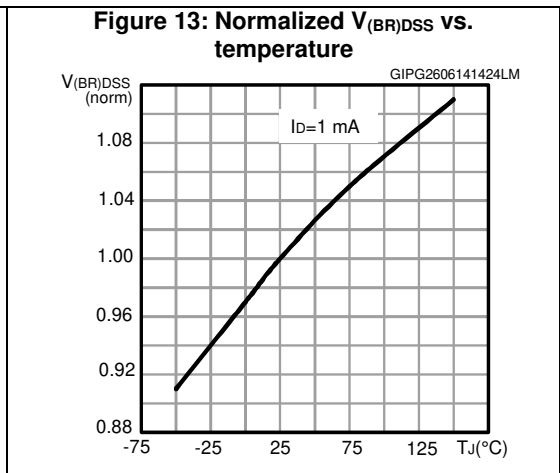
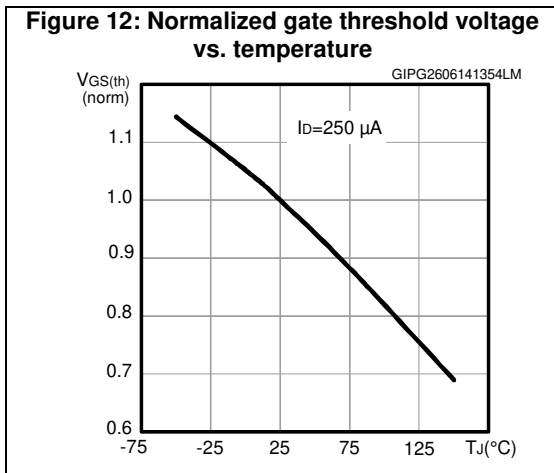
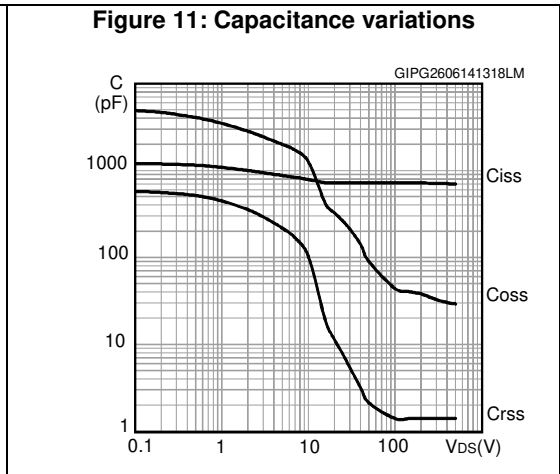
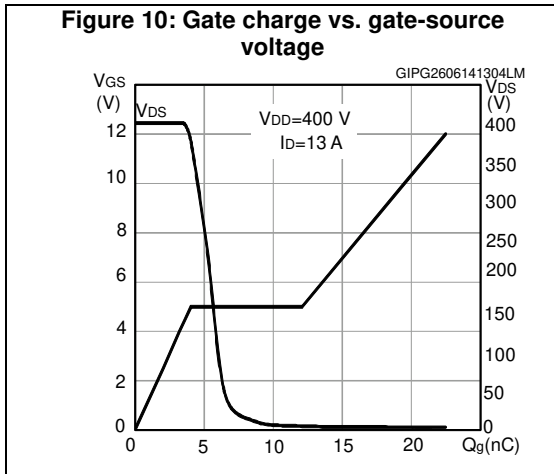
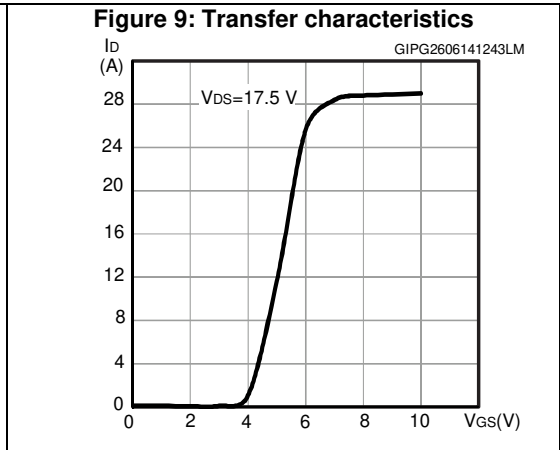
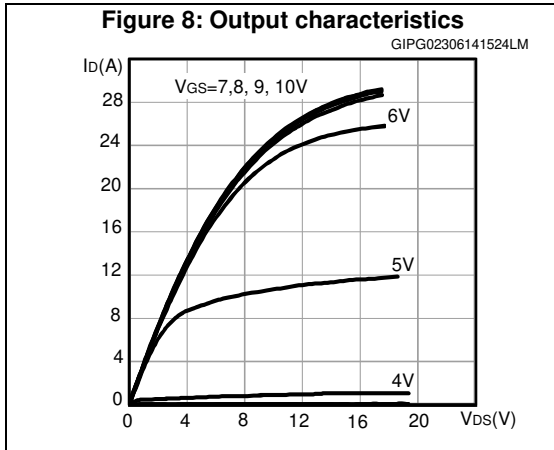


Figure 14: Static drain-source on-resistance

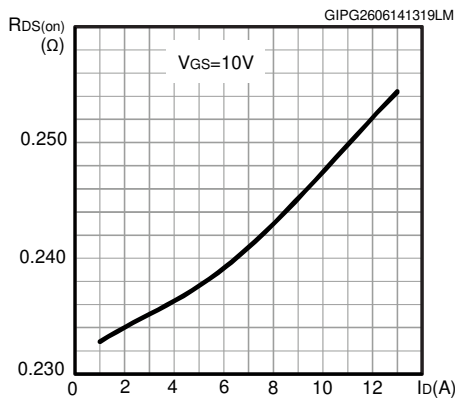


Figure 15: Normalized on-resistance vs. temperature

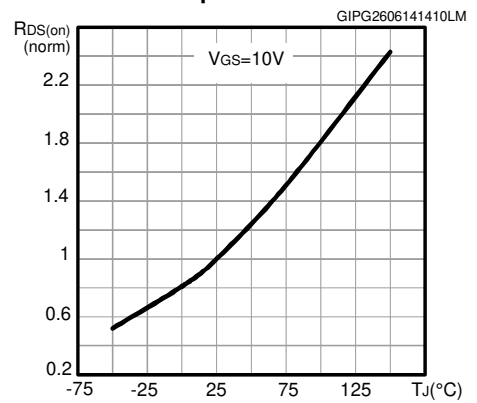


Figure 16: Output capacitance stored energy

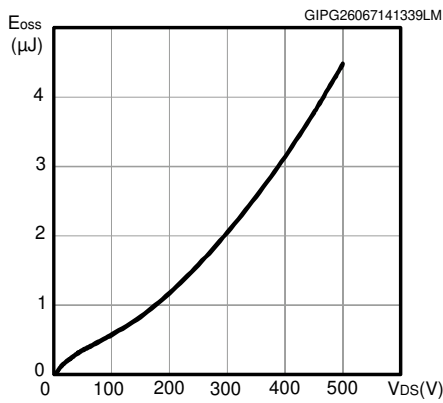
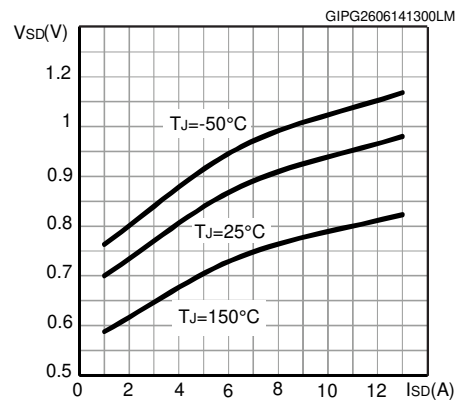
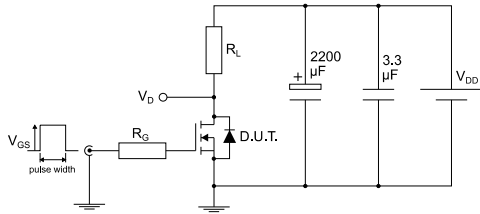


Figure 17: Source-drain diode forward characteristics



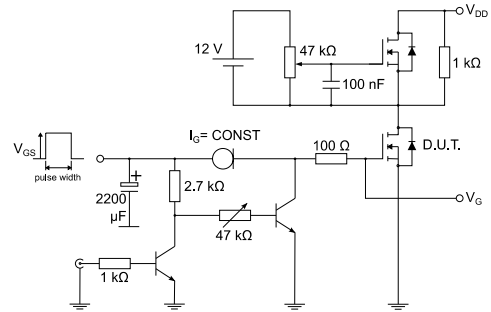
3 Test circuits

Figure 18: Test circuit for resistive load switching times



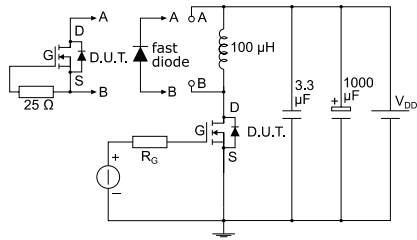
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Figure 19: Test circuit for gate charge behavior



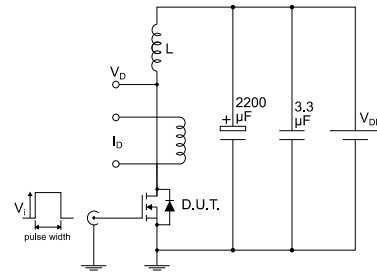
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Figure 20: Test circuit for inductive load switching and diode recovery times



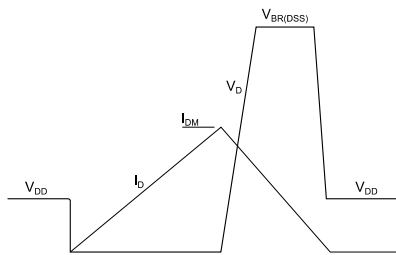
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Figure 21: Unclamped inductive load test circuit



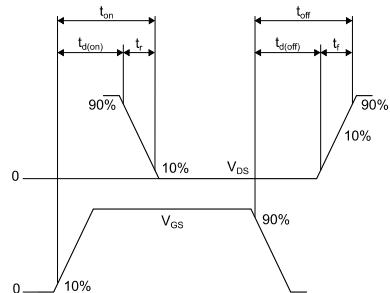
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Figure 22: Unclamped inductive waveform



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Figure 23: Switching time waveform



AM01473v1

4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 DPAK (TO-252) type A2 package information

Figure 24: DPAK (TO-252) type A2 package outline

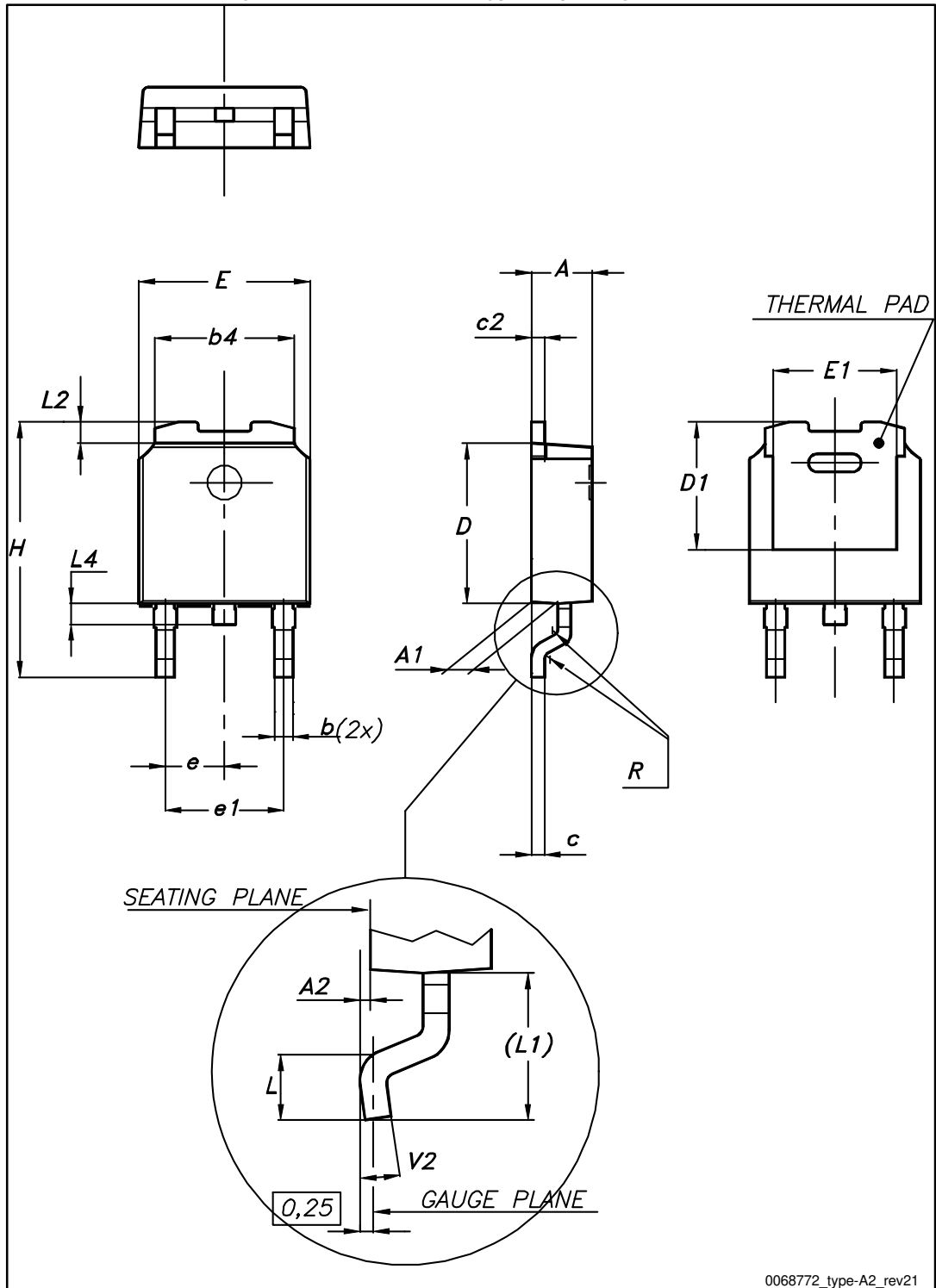
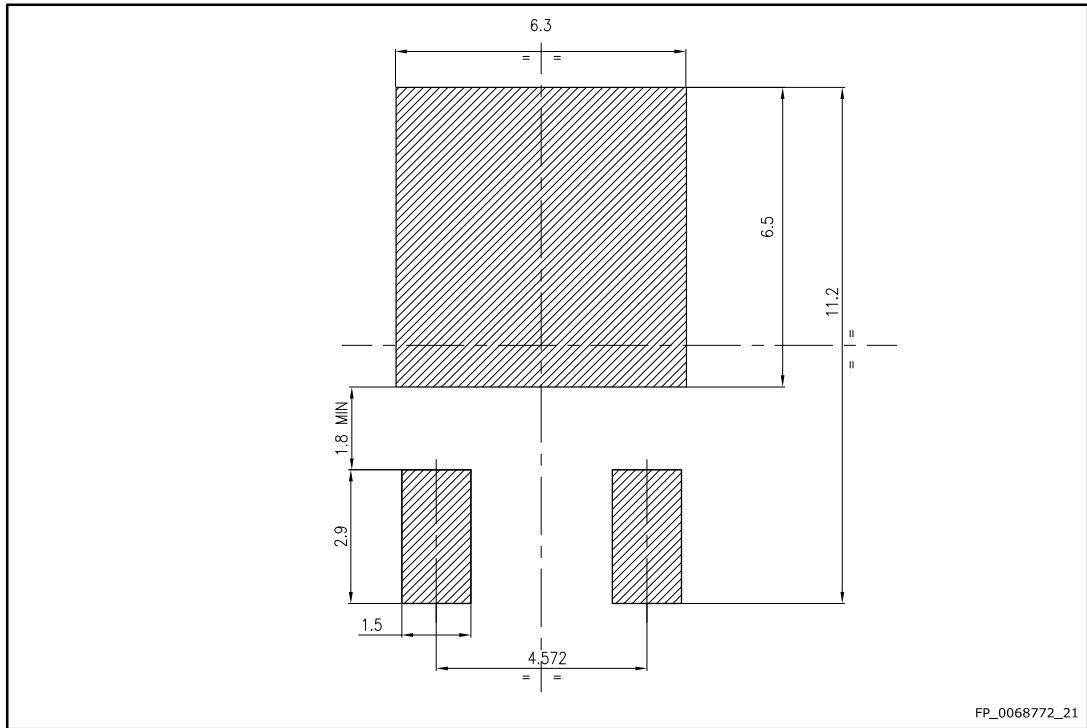


Table 9: DPAK (TO-252) type A2 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	5.10	5.20	5.30
e	2.16	2.28	2.40
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
L1	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 25: DPAK (TO-252) recommended footprint (dimensions are in mm)



4.2 DPAK (TO-252) packing information

Figure 26: DPAK (TO-252) tape outline

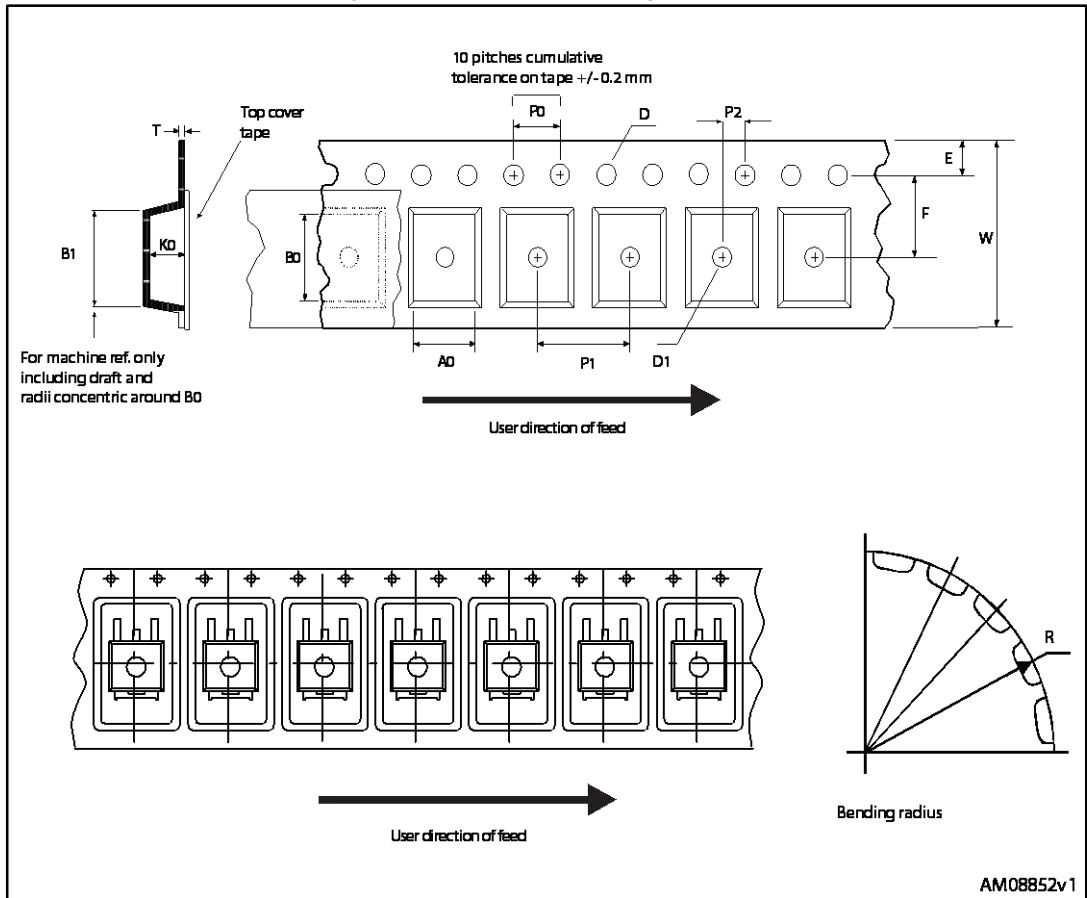


Figure 27: DPAK (TO-252) reel outline

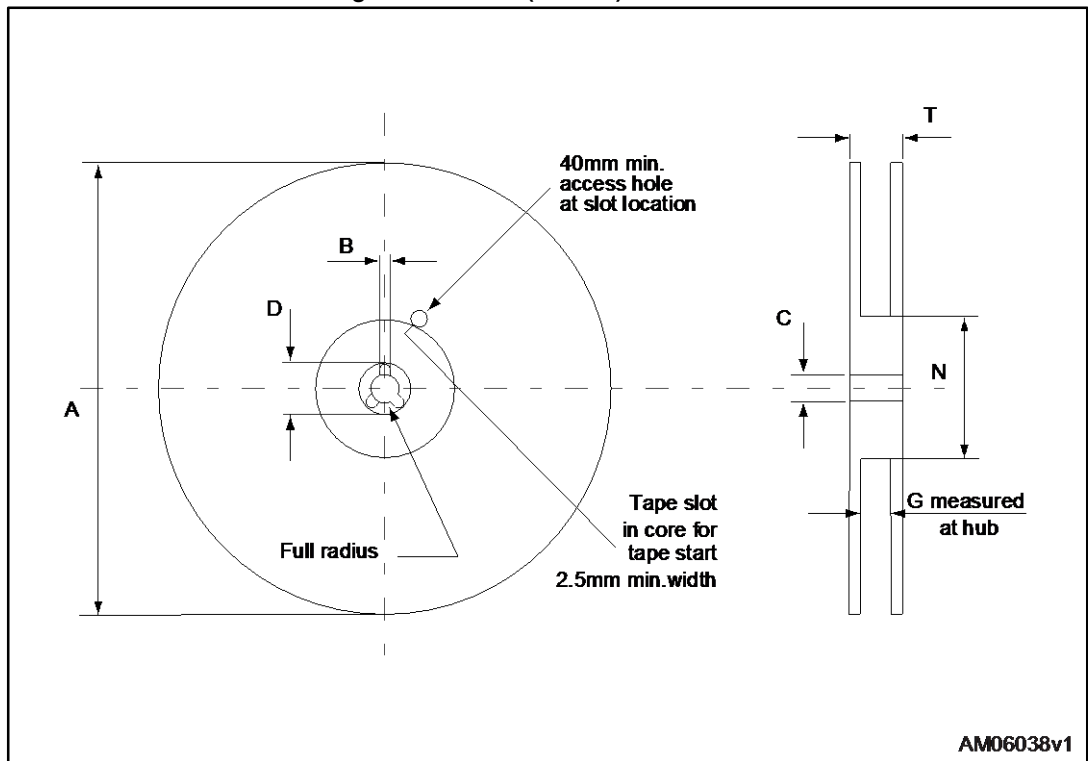
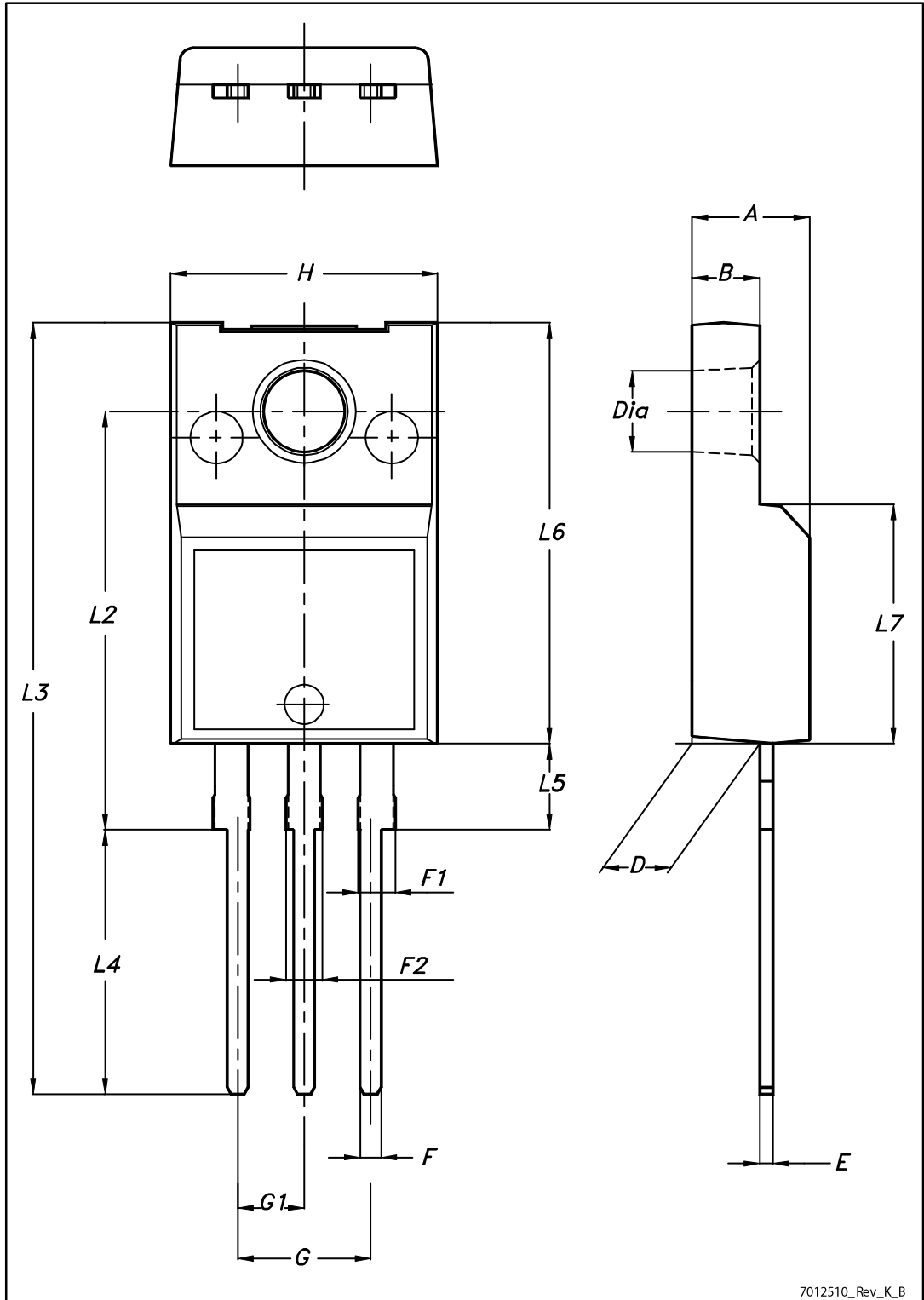


Table 10: DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

4.3 TO-220FP package information

Figure 28: TO-220FP package outline



7012510_Rev_K_B

Table 11: TO-220FP package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

Table 12: TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95

5 Revision history

Table 13: Document revision history

Date	Revision	Changes
04-Jul-2014	1	Initial release.
18-Jul-2014	2	Updated <i>Figure 9</i> .
31-Jul-2014	3	Updated <i>Figure 2</i> and <i>Figure 4</i> .
25-Aug-2016	4	Datasheet promoted from preliminary data to production data Changed: <i>Section 4.1: "DPAK (TO-252) type A2 package information"</i> Minor text changes

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