
Chipsmall
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Geelead Technology Limited
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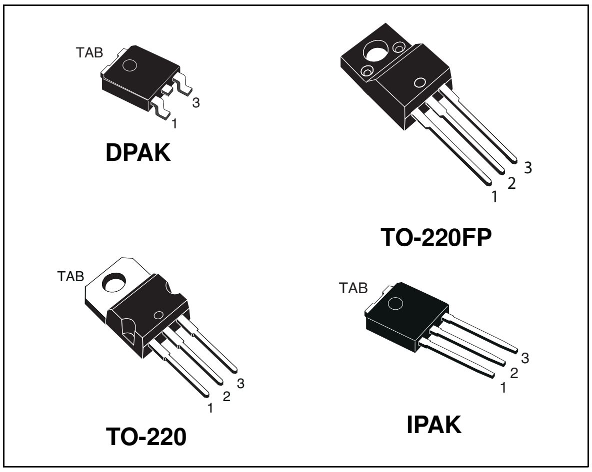
采购部

STD9N65M2, STF9N65M2, STP9N65M2, STU9N65M2

N-channel 650 V, 0.79 Ω typ., 5 A MDmesh M2 Power MOSFETs in DPAK, TO-220FP, TO-220 and IPAK packages

Datasheet - production data



Features

Order codes	V_{DS}	$R_{DS(on)}$ max	I_D
STD9N65M2	650 V	0.9 Ω	5 A
STF9N65M2			
STP9N65M2			
STU9N65M2			

- Extremely low gate charge
- Excellent output capacitance (C_{oss}) profile
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

These devices are N-channel Power MOSFETs developed using the MDmesh™ M2 technology. Thanks to the strip layout associated to an improved vertical structure, the devices exhibit both low on-resistance and optimized switching characteristics. They are therefore suitable for the most demanding high efficiency converters.

Figure 1. Internal schematic diagram

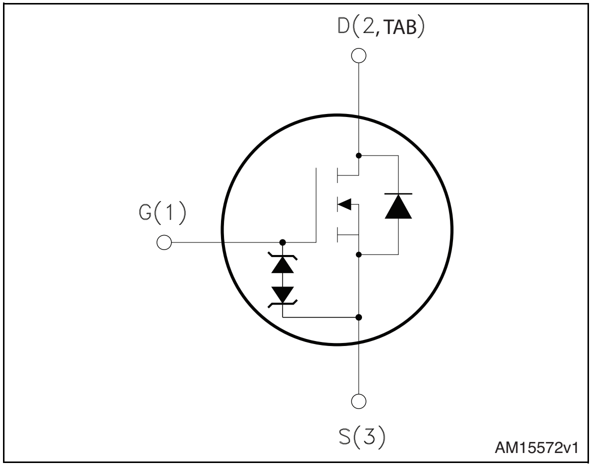


Table 1. Device summary

Order codes	Marking	Package	Packaging
STD9N65M2	9N65M2	DPAK	Tape and reel
STF9N65M2		TO-220FP	Tube
STP9N65M2		TO-220	
STU9N65M2		IPAK	

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		DPAK, TO-220, IPAK	TO-220FP	
V_{GS}	Gate-source voltage	± 25		V
I_D	Drain current (continuous) at T_C = 25 °C	5	$5^{(1)}$	A
I_D	Drain current (continuous) at T_C = 100 °C	3.2	$3.2^{(1)}$	A
I_{DM} (2)	Drain current (pulsed)	20		A
P_{TOT}	Total dissipation at T_C = 25 °C	60	20	W
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1 s; T_C=25 °C)		2500	V
dv/dt (3)	Peak diode recovery voltage slope	15		V/ns
dv/dt(4)	MOSFET dv/dt ruggedness	50		
T_{stg}	Storage temperature	- 55 to 150		°C
T_j	Max. operating junction temperature	150		

1. Current limited by package.
2. Pulse width limited by safe operating area.
3. $I_{SD} \leq 5$ A, di/dt ≤ 400 A/µs; $V_{DS\ peak} < V_{(BR)DSS}$, V_{DD}=400 V
4. $V_{DS} \leq 520$ V

Table 3. Thermal data

Symbol	Parameter	Value				Unit
		DPAK	TO-220FP	TO-220	IPAK	
$R_{thj\text{-}case}$	Thermal resistance junction-case max	2.08	6.25	2.08		°C/W
$R_{thj\text{-}pcb}^{(1)}$	Thermal resistance junction-pcb max	50				°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient max		62.5		100	°C/W

1. When mounted on 1 inch² FR-4, 2 Oz copper board

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax})	1	A
E_{AS}	Single pulse avalanche energy (starting T_j=25°C, I_D= I_{AR}; V_{DD}=50)	105	mJ

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 5. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0, I_D = 1 mA	650			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0, V_{DS} = 650 V			1	µA
		V_{GS} = 0, V_{DS} = 650 V, T_C=125 °C			100	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0, V_{GS} = ± 25 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 2.5 A		0.79	0.9	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0	-	315	-	pF
C_{oss}	Output capacitance		-	18	-	pF
C_{rss}	Reverse transfer capacitance		-	1	-	pF
$C_{oss\ eq}$[1]	Equivalent output capacitance	V_{GS} = 0, V_{DS} = 0 to 520 V	-	109	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz open drain	-	6.6	-	Ω
Q_g	Total gate charge	V_{DD} = 520 V, I_D = 5 A, V_{GS} = 10 V (see *Figure 19*)	-	10	-	nC
Q_{gs}	Gate-source charge		-	2.5	-	nC
Q_{gd}	Gate-drain charge		-	5	-	nC

1. Coss eq. is defined as a constant equivalent capacitance giving the same charging time as Coss when VDS increases from 0 to 80% VDSS

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 325 V, I_D = 2.5 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 18* and *Figure 23*)	-	7.5	-	ns
t_r	Rise time		-	6.6	-	ns
$t_{d(off)}$	Turn-off delay time		-	22.5	-	ns
t_f	Fall time		-	18	-	ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		5	A
I_{SDM} (1)	Source-drain current (pulsed)		-		20	A
V_{SD} (2)	Forward on voltage	V_{GS} = 0, I_{SD} = 5 A	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 5 A, di/dt = 100 A/µs V_{DD} = 60 V (see *Figure 20*)	-	276		ns
Q_{rr}	Reverse recovery charge		-	1.7		µC
I_{RRM}	Reverse recovery current		-	12.5		A
t_{rr}	Reverse recovery time	I_{SD} = 5 A, di/dt = 100 A/µs V_{DD} = 60 V, T_j = 150 °C (see *Figure 20*)	-	312		ns
Q_{rr}	Reverse recovery charge		-	1.9		µC
I_{RRM}	Reverse recovery current		-	12.4		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for DPAK and IPAK

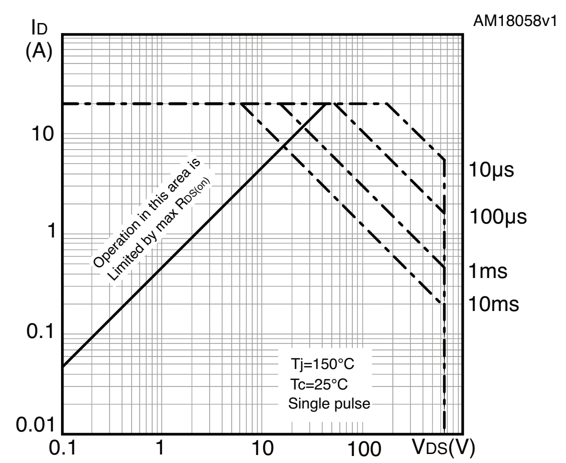


Figure 3. Thermal impedance for DPAK and IPAK

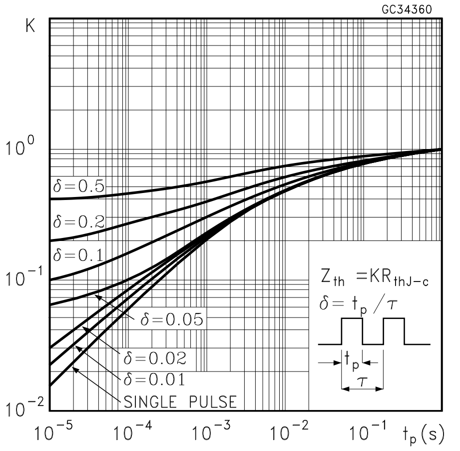


Figure 4. Safe operating area for TO-220FP

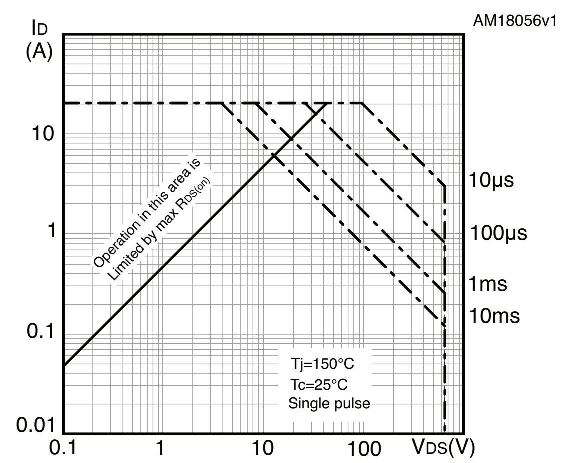


Figure 5. Thermal impedance for TO-220FP

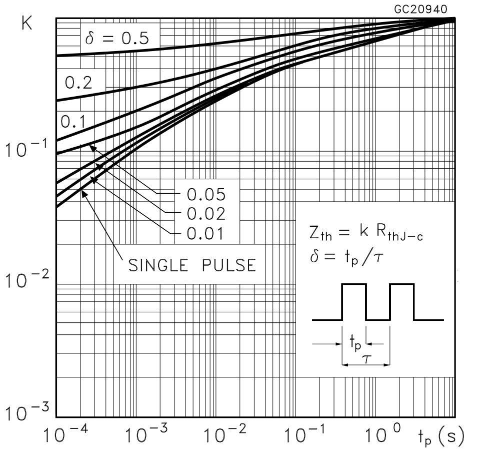


Figure 6. Safe operating area for TO-220

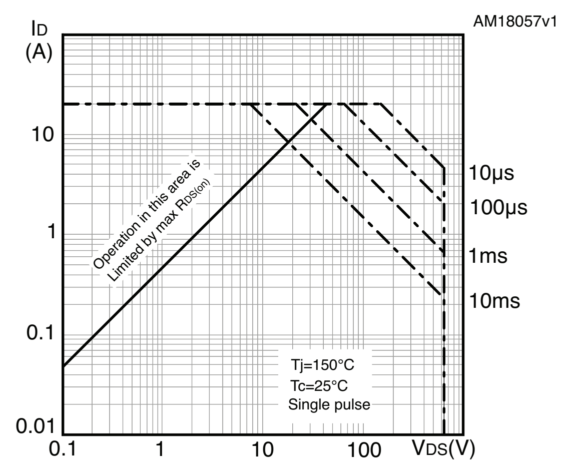


Figure 7. Thermal impedance for TO-220

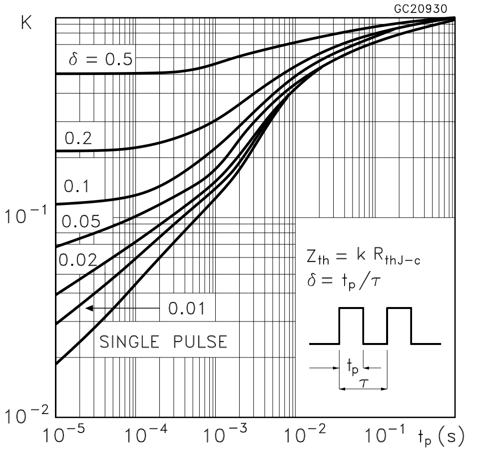


Figure 8. Output characteristics

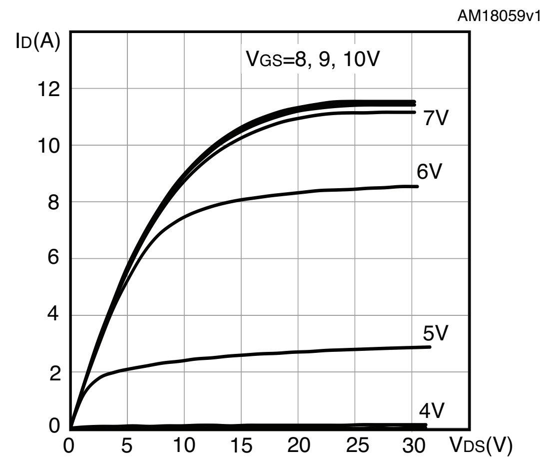


Figure 9. Transfer characteristics

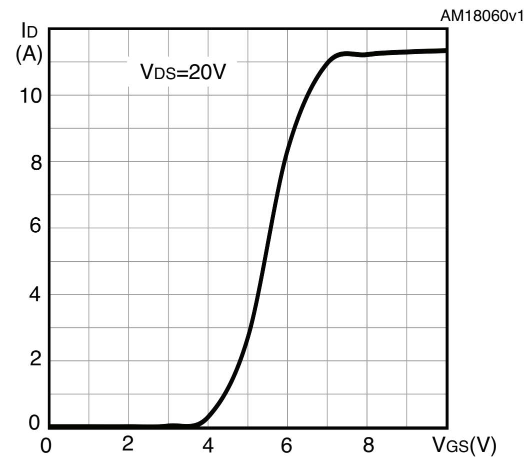


Figure 10. Gate charge vs gate-source voltage

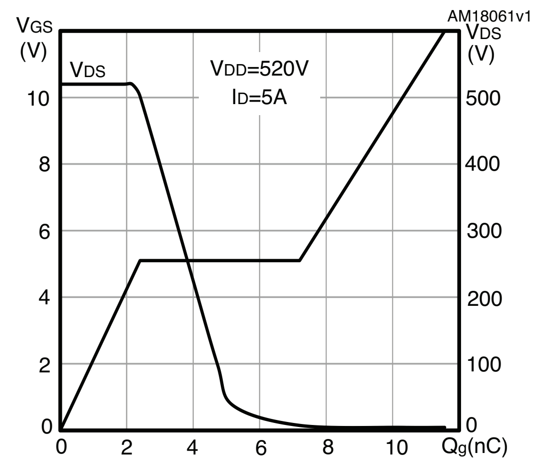


Figure 11. Static drain-source on-resistance

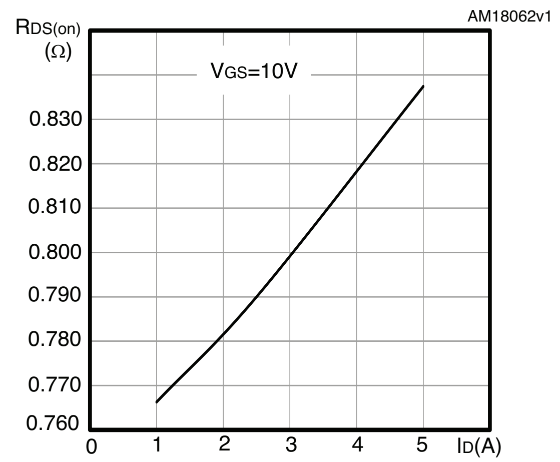


Figure 12. Capacitance variations

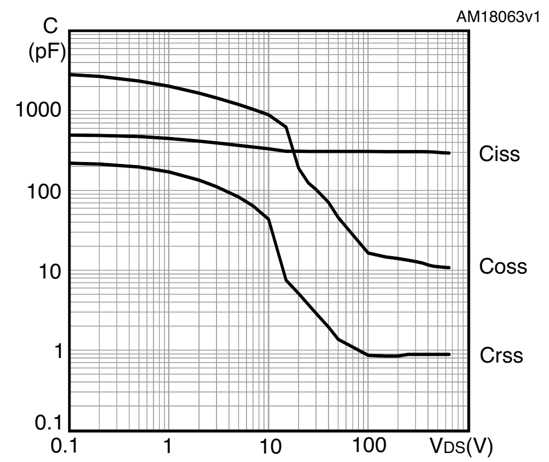


Figure 13. Output capacitance stored energy

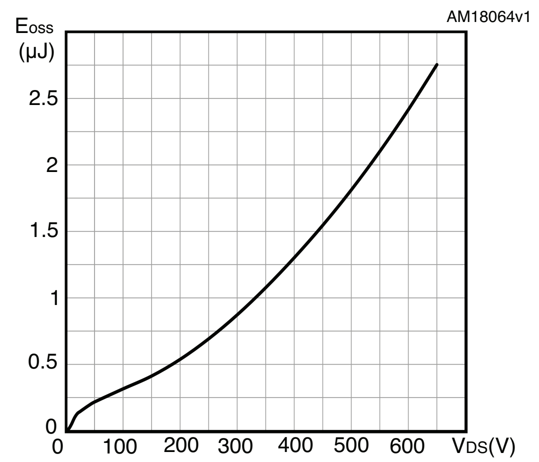


Figure 14. Normalized gate threshold voltage vs temperature

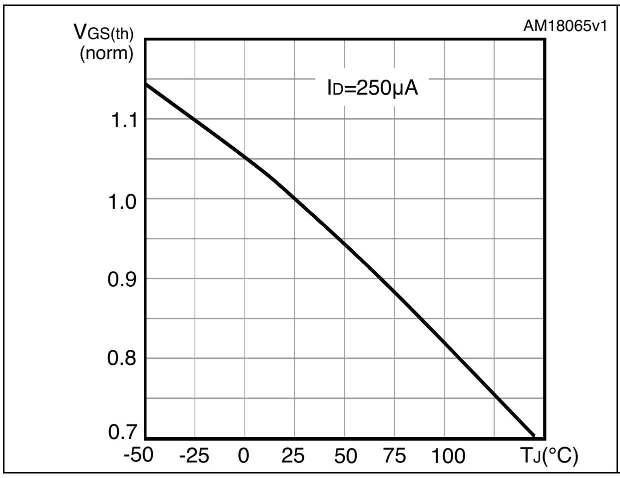


Figure 15. Normalized on-resistance vs temperature

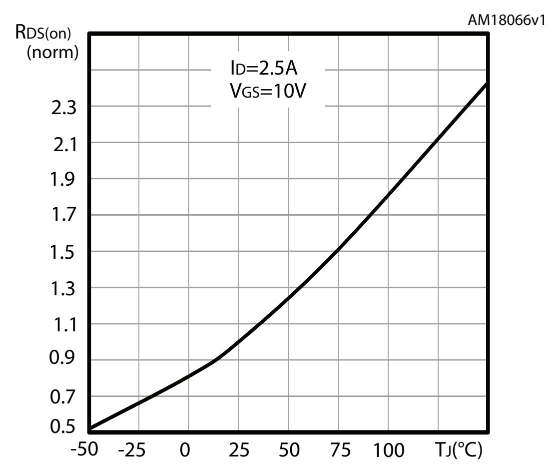


Figure 16. Source-drain diode forward characteristics

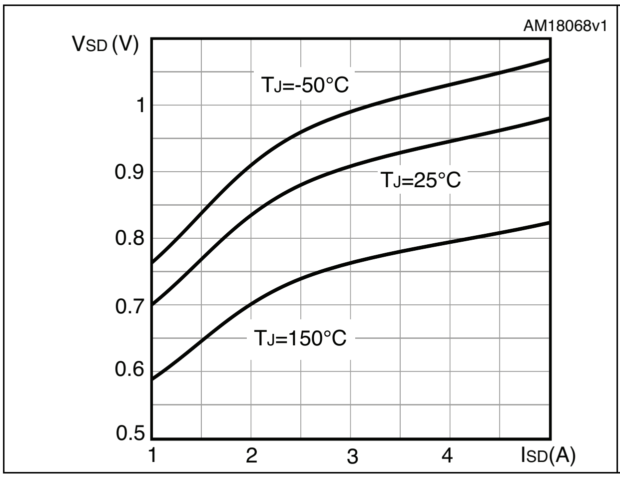
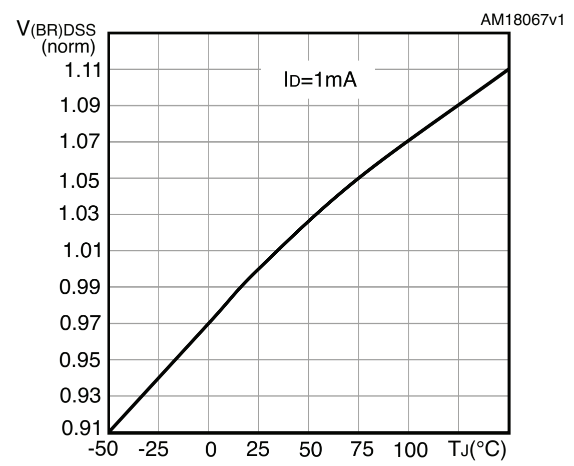


Figure 17. Normalized $V_{(BR)DSS}$ vs temperature



3 Test circuits

Figure 18. Switching times test circuit for resistive load

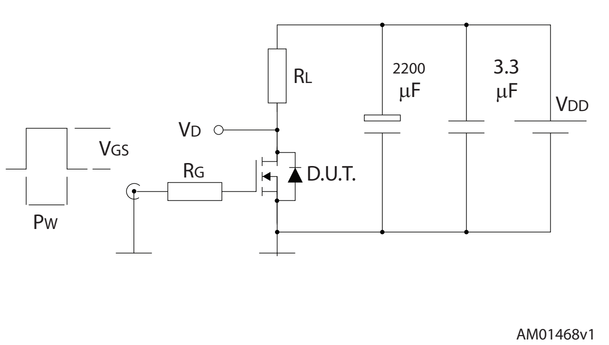


Figure 19. Gate charge test circuit

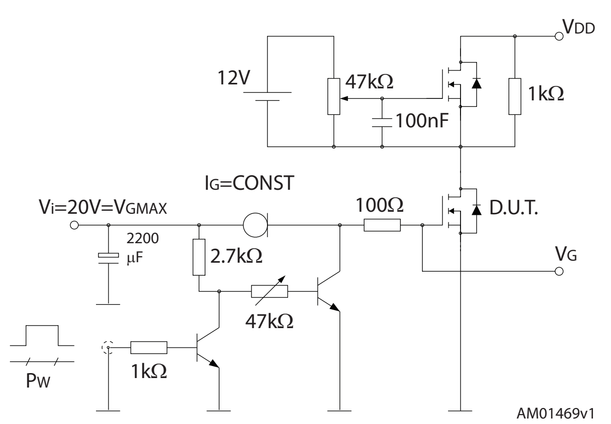


Figure 20. Test circuit for inductive load switching and diode recovery times

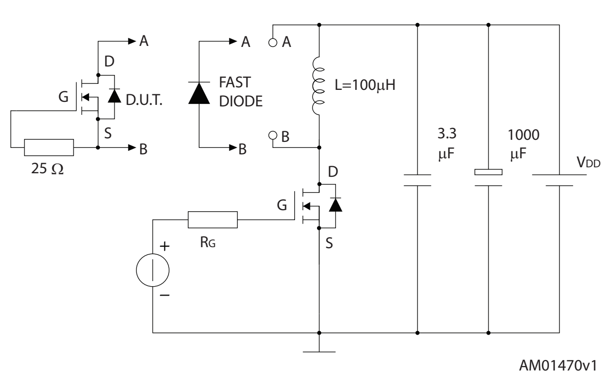


Figure 21. Unclamped inductive load test circuit

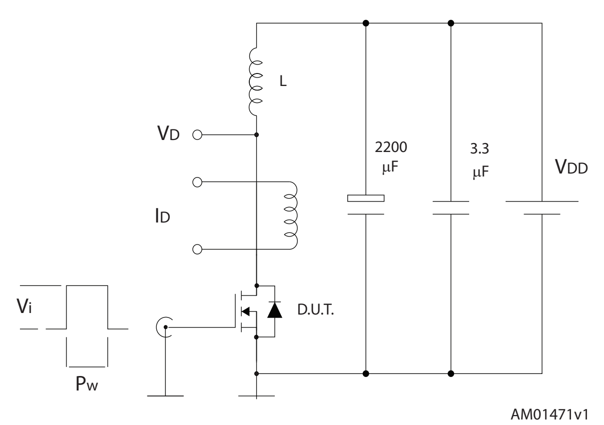


Figure 22. Unclamped inductive waveform

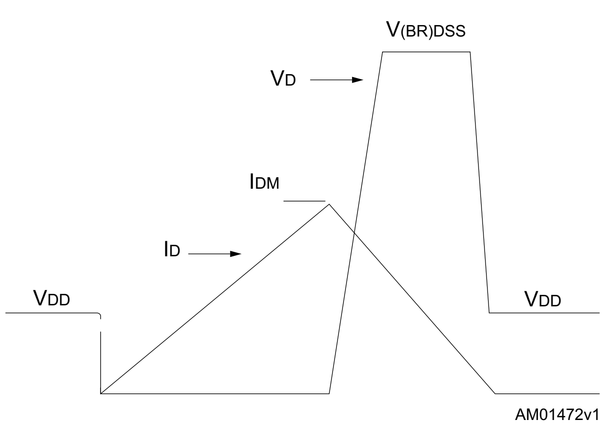
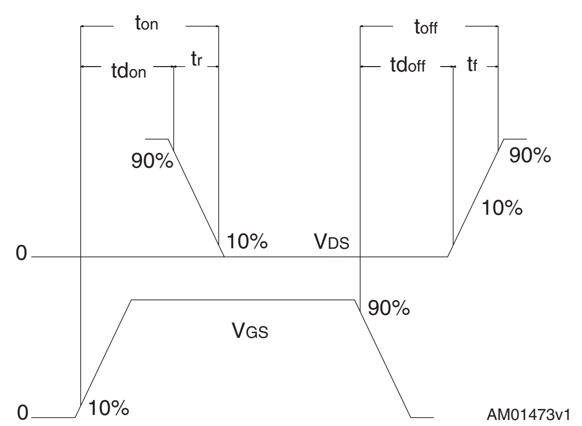


Figure 23. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

4.1 DPAK, STD9N65M2

Figure 24. DPAK (TO-252) type A drawing

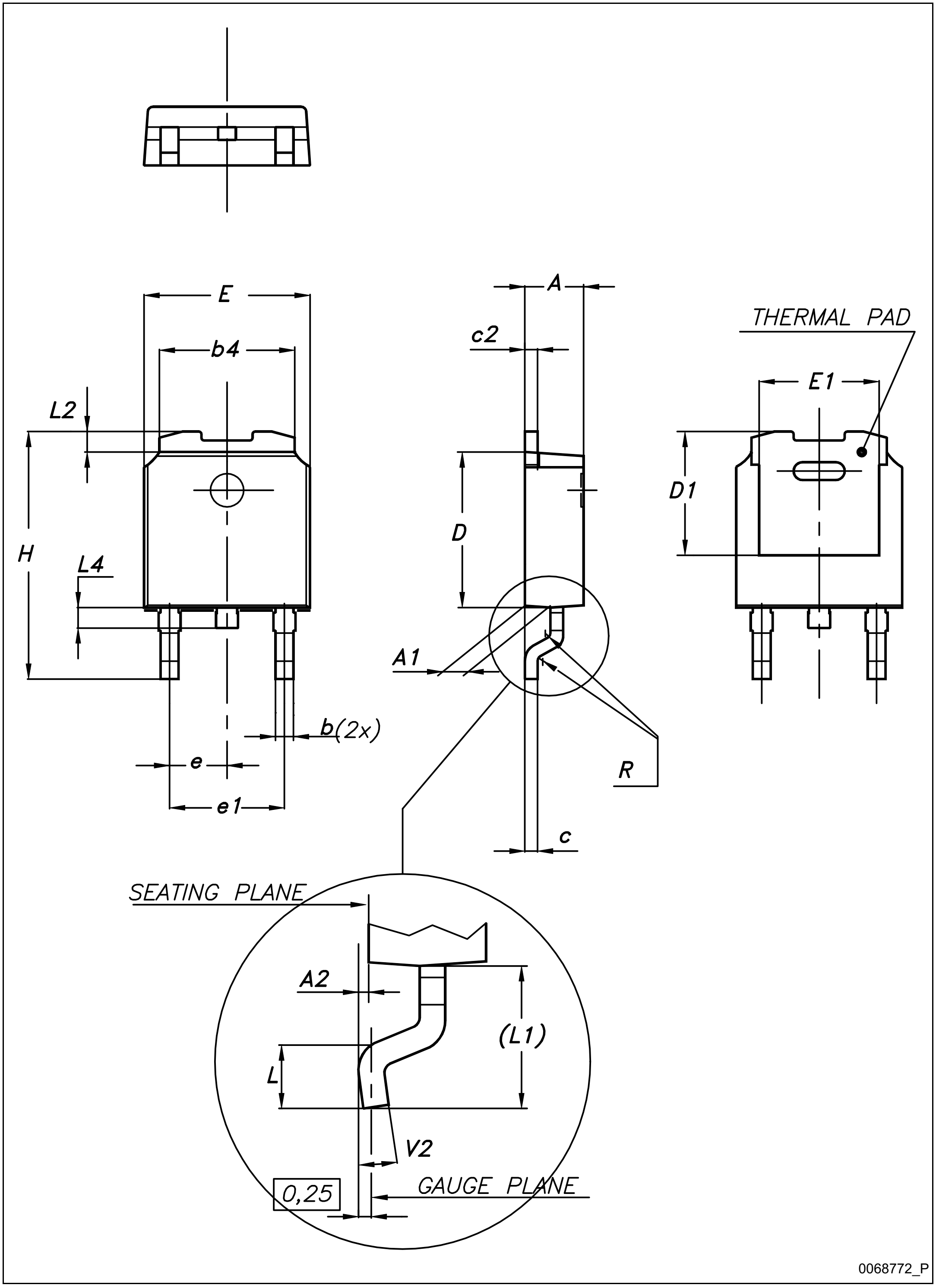
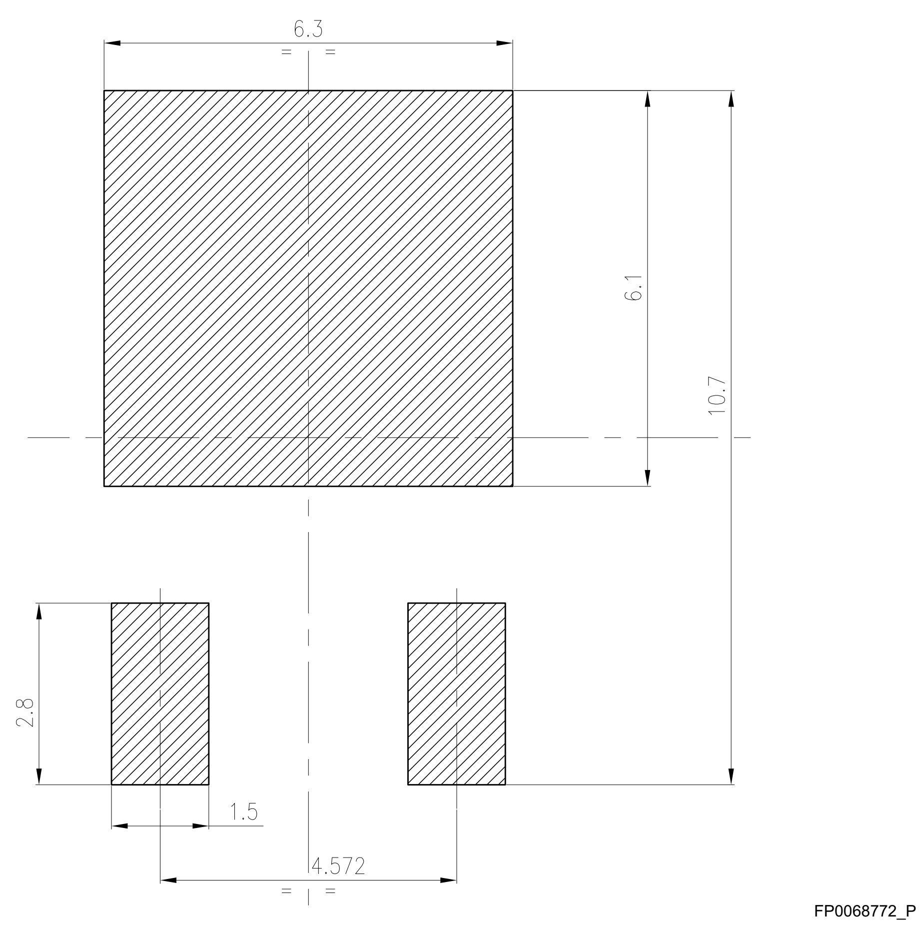


Table 9. DPAK (TO-252) type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
L1		2.80	
L2		0.80	
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 25. DPAK (TO-252) type A footprint [a]



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[a] All dimensions are in millimeters

4.2 TO-220FP, STF9N65M2

Figure 26. TO-220FP drawing

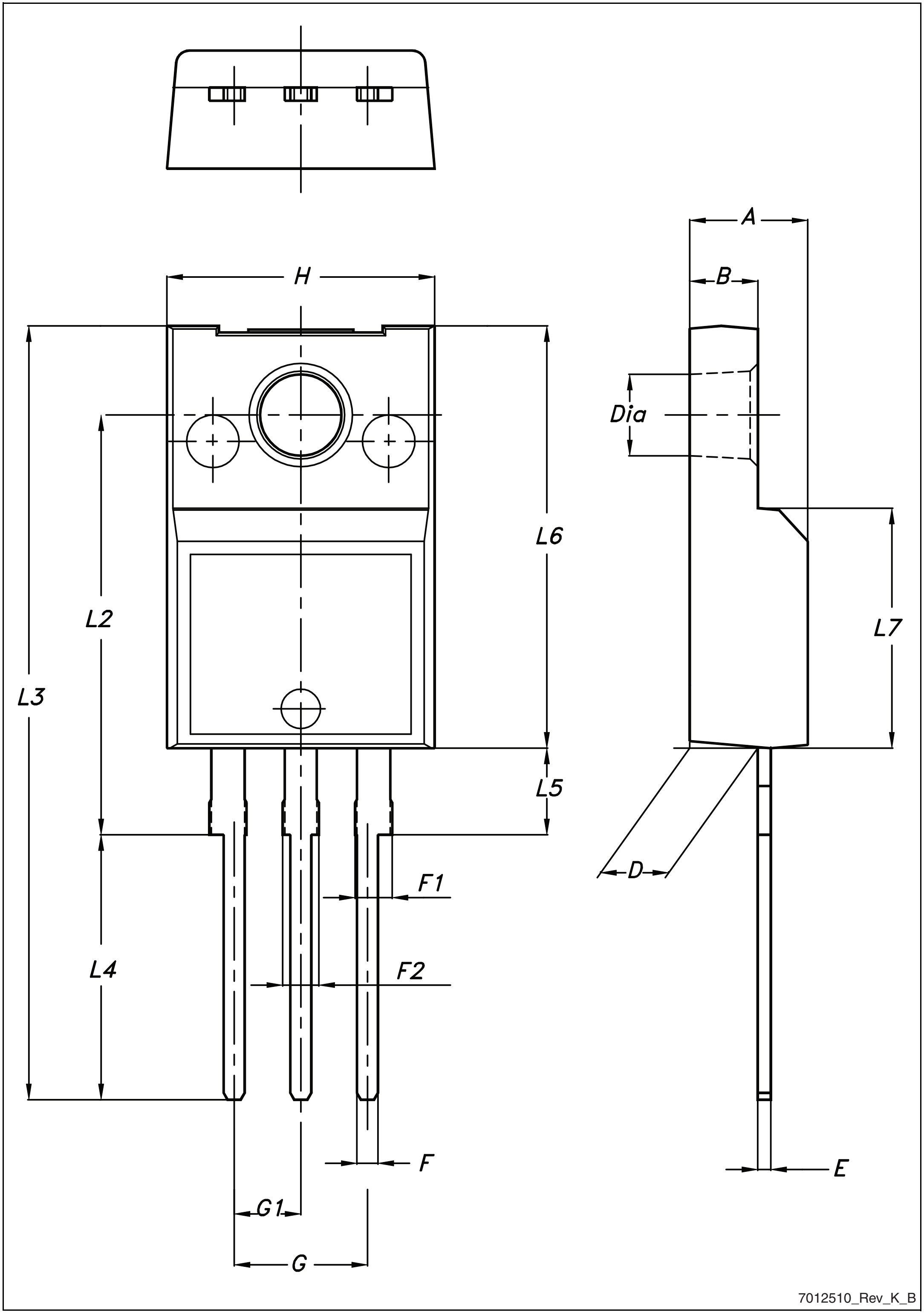

Table 10. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Ø	3		3.2

4.3 TO-220, STP9N65M2

Figure 27. TO-220 type A drawing

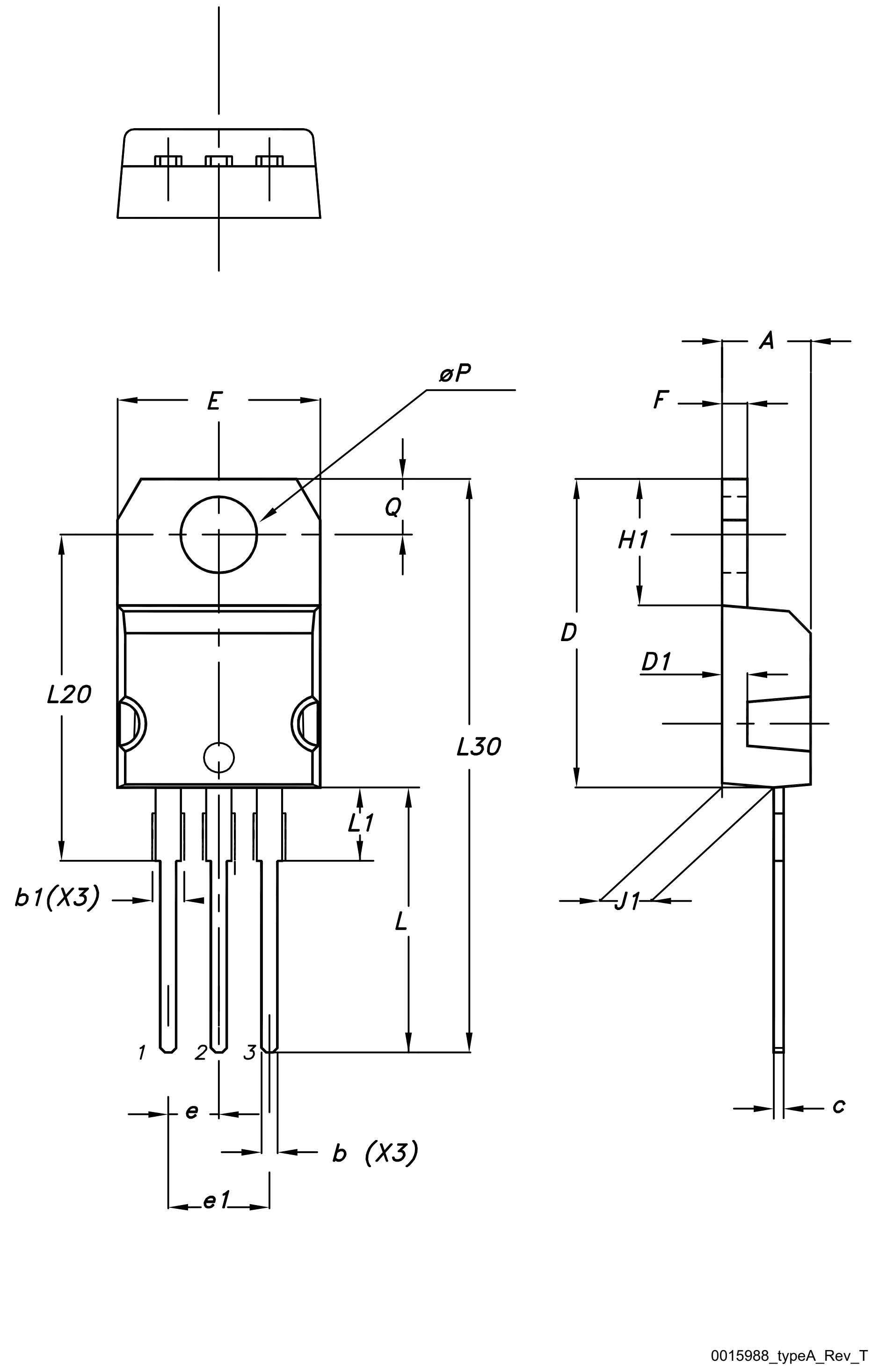

Table 11. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
∅P	3.75		3.85
Q	2.65		2.95

4.4 IPAK, STU9N65M2

Figure 28. IPAK (TO-251) drawing

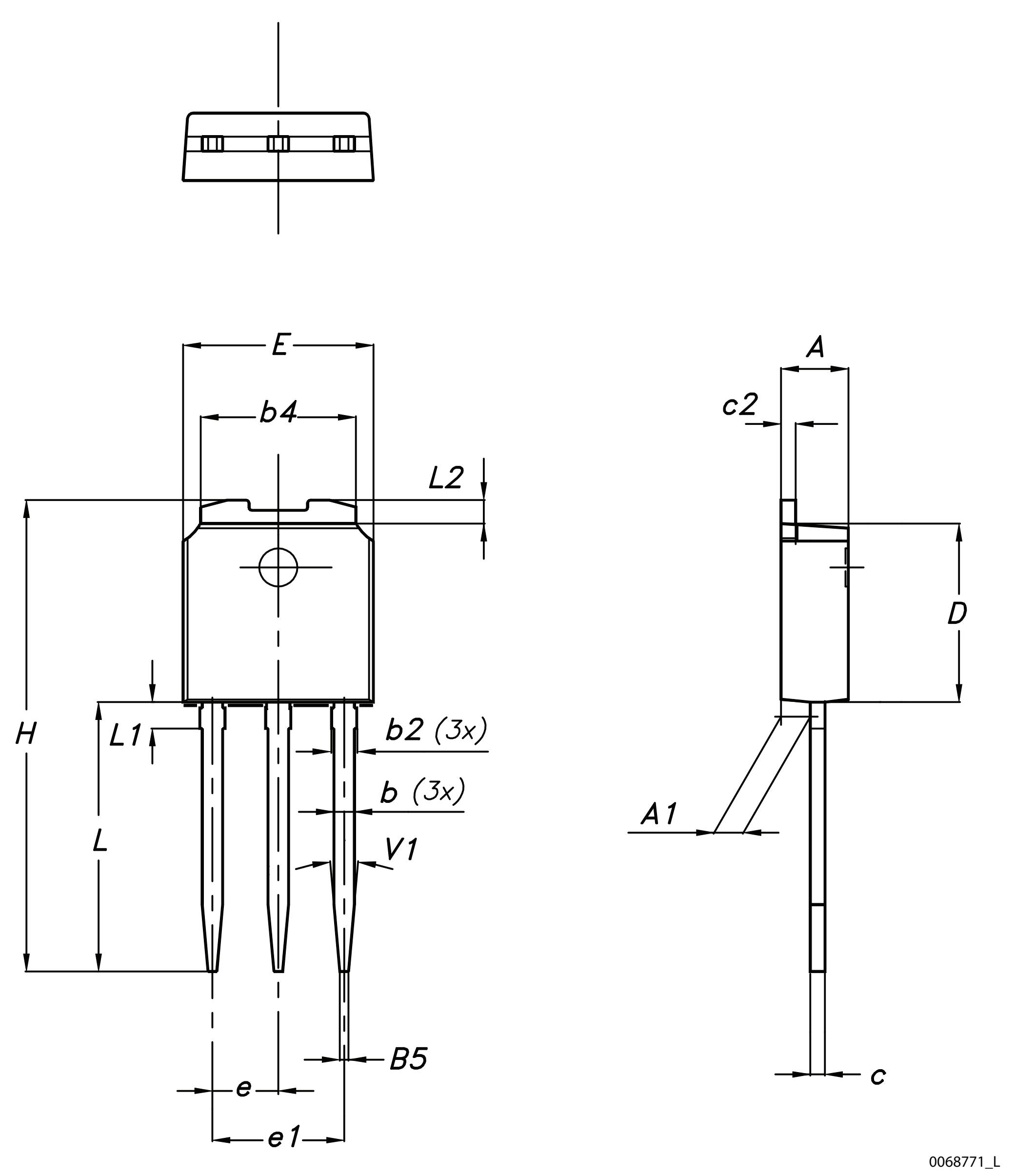

Table 12. IPAK (TO-251) mechanical data

DIM	mm.		
	min.	typ.	max.
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
B5		0.30	
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
E	6.40		6.60
e		2.28	
e1	4.40		4.60
H		16.10	
L	9.00		9.40
L1	0.80		1.20
L2		0.80	1.00
V1		10°	

5 Packaging mechanical data

Figure 29. Tape for DPAK (TO-252)

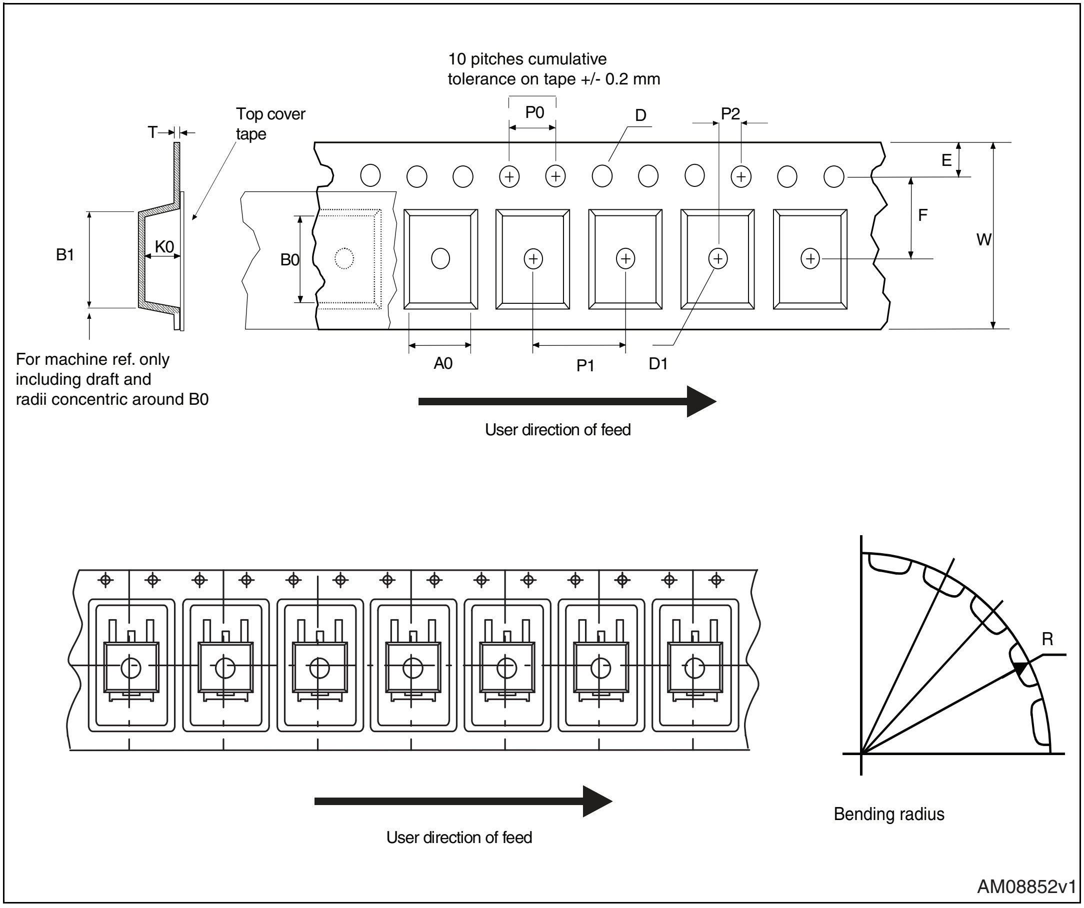

Figure 30. Reel for DPAK (TO-252)

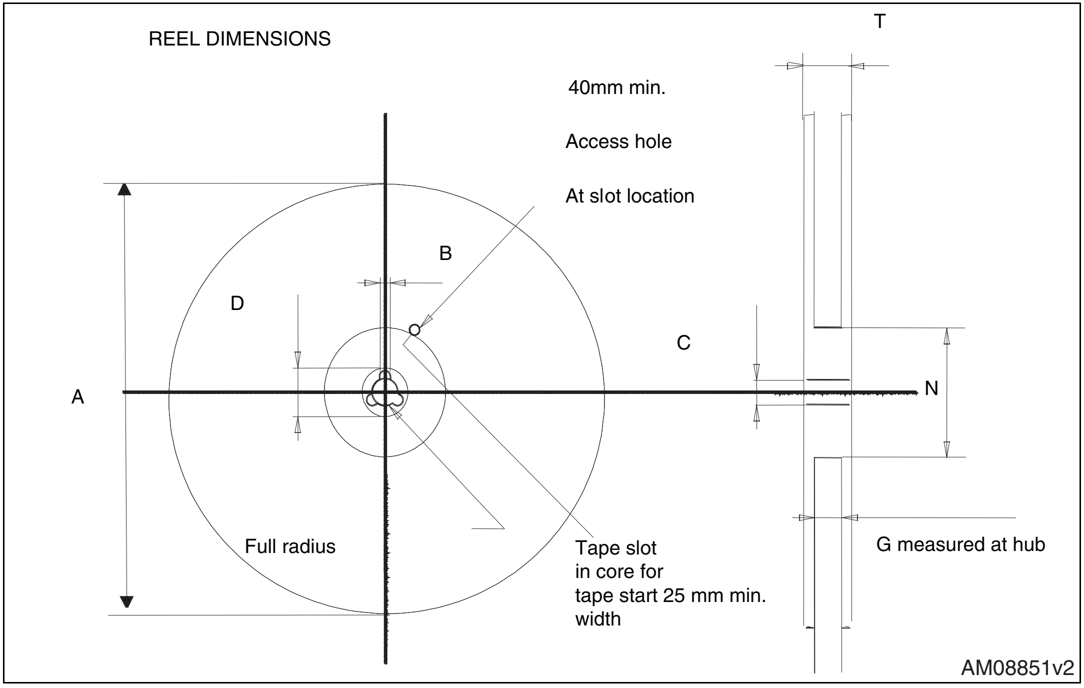

Table 13. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

6 Revision history

Table 14. Document revision history

Date	Revision	Changes
24-Feb-2014	1	First release.
15-Jul-2014	2	– Modified: title, *Features* and *Description* – Modified: *Figure 5* and *15* – Updated: *Figure 28* and *Table 12* – Minor text changes