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STPC® CONSUMER-II

X86 Core PC Compatible Information Appliance System-on-Chip

■ POWERFUL x86 PROCESSOR

■ 64-BIT SDRAM UMA CONTROLLER

■ VGA & SVGA CRT CONTROLLER

■ 135 MHz RAMDAC

■ 2D GRAPHICS ENGINE

■ VIDEO INPUT PORT

■ VIDEO PIPELINE
  - UP-SCALER
  - VIDEO COLOUR SPACE CONVERTER
  - CHROMA & COLOUR KEY SUPPORT

■ TV OUTPUT
  - THREE-LINE FLICKER FILTER
  - ITU-R 601/656 SCAN CONVERTER
  - NTSC / PAL COMPOSITE, RGB, S-VIDEO

■ PCI MASTER / SLAVE / ARBITER

■ ISA MASTER / SLAVE

■ OPTIONAL 16-BIT LOCAL BUS INTERFACE

■ EIDE CONTROLLER

■ I²C INTERFACE

■ IPC
  - DMA CONTROLLER
  - INTERRUPT CONTROLLER
  - TIMER / COUNTERS

■ POWER MANAGEMENT UNIT

■ JTAG IEEE1149.1

DESCRIPTION

The STPC Consumer-II integrates a standard 5th generation x86 core, a Synchronous DRAM controller, a graphics subsystem, a video pipeline, and support logic including PCI, ISA, and IDE controllers to provide a single consumer orientated PC compatible subsystem on a single device.

The device is based on a tightly coupled Unified Memory Architecture (UMA), sharing memory between the CPU, the graphics and the video.

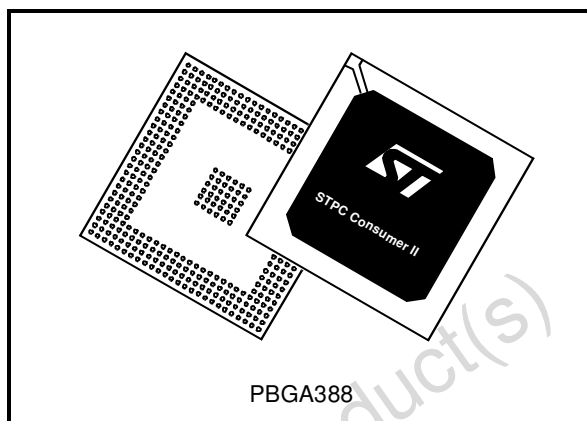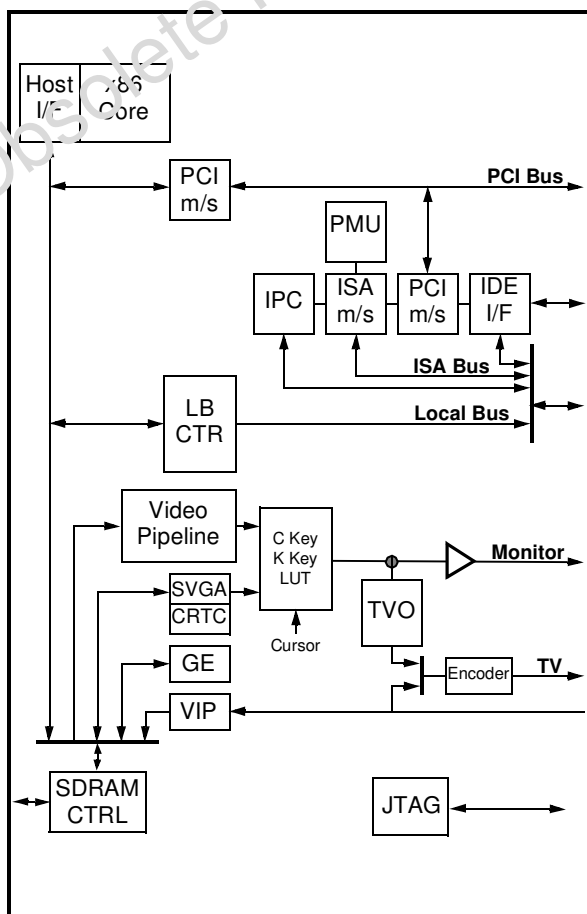The STPC Consumer-II is packaged in a 388 Plastic Ball Grid Array (PBGA).

PBGA388

Figure 0-1. Logic Diagram

■ **X86 Processor core**
■ Fully static 32-bit five-stage pipeline, x86 processor fully PC compatible.
■ Can access up to 4 GB of external memory.
■ 8 Kbyte unified instruction and data cache with write back and write through capability.
■ Parallel processing integral floating point unit, with automatic power down.
■ Runs up to 100 MHz (x1) or 133 MHz (x2).
■ Fully static design for dynamic clock control.
■ Low power and system management modes.
■ Optimized design for 2.5 V operation.

■ **SDRAM Controller**
■ 64-bit data bus.
■ Up to 100 MHz SDRAM clock speed.
■ Integrated system memory, graphic frame memory and video frame memory.
■ Supports 2 MB up to 128 MB system memory.
■ Supports 16-, 64-, and 128-Mbit SDRAMs.
■ Supports 8, 16, 32, 64, and 128 MB DIMMs.
■ Supports buffered, non buffered, and registered DIMMs
■ Four-line write buffers for CPU to SDRAM and PCI to SDRAM cycles.
■ Four-line read prefetch buffers for PCI masters.
■ Programmable latency
■ Programmable timing for SDRAM parameters.
■ Supports -8, -10, -12, -13, -15 memory parts
■ Supports memory hole between 1 MB and 8 MB for PCI/ISA busses.

■ **2D Graphics Controller**
■ 64-bit windows accelerator.
■ Backward compatibility to SVGA standards.
■ Hardware acceleration for text, bitblts, transparent blts and fills.
■ Up to 64 x 64 bit graphics hardware cursor.
■ Up to 4MB long linear frame buffer.
■ 8-, 16-, 24- and 32-bit pixels.
■ Drivers availables for various OSes.

■ **CRT Controller**
■ Integrated 135 MHz triple RAMDAC allowing for 1280 x 1024 x 75 Hz display.
■ Requires external frequency synthesizer and reference sources.
■ 8-bit, 16-bit, 24-bit pixels.
■ Interlaced or non-interlaced output.
■ Requires no external frequency synthesizer.
■ Requires only external reference source.

■ **Video Input port**
■ Accepts video inputs in ITU-R 601 mode.
■ Optional 2:1 decimator
■ Stores captured video in off setting area of the onboard frame buffer.
■ Video pass through to the TV output for full screen video images.
■ HSYNC and B/T generation or lock onto external video timing source.

■ **Video Pipeline**
■ Two-tap interpolative horizontal filter.
■ Two-tap interpolative vertical filter.
■ Colour space conversion (RGB to YUV and YUV to RGB).
■ Programmable window size.
■ Chroma and colour keying for integrated video overlay.

■ **Video Output**
■ NTSC-M; PAL-B, D, G, H, I, M, N encoding.
■ ITU-R 601 encoding with programmable colour subcarrier frequencies.
■ ITU-R 656 video output signal interface.
■ Four analog outputs in two configurations:
  - R,G,B + CVBS
  - C,YS,CVBS1 + CVBS2
■ Flicker-free interlaced output.
■ Programmable two tap filter with gamma correction or three tap flicker filter.
■ Interlaced or non-interlaced operation mode.
■ Progressive to interlaced scan converter.
■ Cross colour reduction by specific trap filtering on luma within CVBS flow.
■ Power down mode available on each DAC.

■ **PCI Controller**
■ Fully compliant with PCI 2.1 specification.
■ Integrated PCI arbitration interface. Up to 3 masters can connect directly. External PAL allows for greater than 3 masters.
■ Translation of PCI cycles to ISA bus.
■ Translation of ISA master initiated cycle to PCI.
■ Support for burst read/write from PCI master.
■ PCI clock is 1/2, 1/3 or 1/4 cpu bus clock.

■ **ISA master/slave**
■ Generates the ISA clock from either 14.318 MHz oscillator clock or PCI clock
■ Supports programmable extra wait state for ISA cycles
■ Supports I/O recovery time for back to back I/O cycles.
■ Fast Gate A20 and Fast reset.
■ Supports the single ROM that C, D, or E. blocks shares with F block BIOS ROM.
■ Supports flash ROM.
■ Supports ISA hidden refresh.
■ Buffered DMA & ISA master cycles to reduce bandwidth utilization of the PCI and Host bus.

■ **Local Bus interface**
■ Multiplexed with ISA/DMA interface.
■ Low latency asynchronous bus
■ 22-bit address bus.
■ 16-bit data bus with word steering capability.
■ Programmable timing (Host clock granularity)
■ Two Programmable Flash Chip Select.
■ Four Programmable I/O Chip Select.
■ Supports 32-bit Flash burst.
■ Two-level hardware key protection for Flash boot block protection.
■ Supports two banks of 16 MB flash devices with boot block shadowed to 0x000F0000.

■ **IDE Interface**
■ Supports PIO
■ Transfer Rates to 22 MBytes/sec
■ Supports up to 4 IDE devices
■ Concurrent channel operation (PIO modes) - 4 x 32-Bit Buffer FIFOs per channel
■ Support for PIO mode 3 & 4.
■ Individual drive timing for all four IDE devices
■ Supports both legacy & native IDE modes
■ Supports hard drives larger than 528MB
■ Support for CD-ROM and tape peripherals
■ Backward compatibility with IDE (ATA-1).
■ Drivers for Windows and other Operating Systems

■ **Integrated Peripheral Controller**
■ 2X8237/AT compatible 7-channel DMA controller.
■ 2X8259/AT compatible interrupt Controller. 16 interrupt inputs - ISA and PCI.
■ Three 8254 compatible Timer/Counters.
■ Co-processor error support logic.

■ **Power Management**
■ Four power saving modes: On, Doze, Standby, Suspend.
■ Programmable system activity detector
■ Supports Intel & Cyrix SMM and APM.
■ Supports STOPCLK.
■ Supports IO trap & restart.
■ Independent peripheral time-out timer to monitor hard disk, serial & parallel port.
■ 128K SM_RAM address space from 0xA0000 to 0xB0000

■ **JTAG**
■ Boundary Scan compatible IEEE1149.1.
■ Scan Chain control.
■ Bypass register compatible IEEE1149.1.
■ ID register compatible IEEE1149.1.
■ RAM BIST control.

The STPC Consumer-II has undergone an errata fix upgrade. The different versions can be differenciated by the part number. Both versions are pin to pin compatible and there are some software extensions that have been added to the upgraded parts. The parts labeled STPCC5 are the upgraded parts and the differences are identified in both the Datasheet and Programming Manual. All parts labeled STPCC4 do not support the new features outlined in the documentation. Where nor C4 nor C5 are specified, the information or feature applies to both versions.

Release 1.5 - January 29, 2002

1. GENERAL DESCRIPTION

At the heart of the STPC Consumer-II is an advanced 64-bit x86 processor block. It includes a 64-bit SDRAM controller, advanced 64-bit accelerated graphics and video controller, a high speed PCI local-bus controller and Industry standard PC chip set functions (Interrupt controller, DMA Controller, Interval timer and ISA bus).

The STPC Consumer-II has in addition, an EIDE Controller, I²C Interface, a Local Bus interface and a JTAG interface.

1.1. ARCHITECTURE

The STPC Consumer-II makes use of a tightly coupled Unified Memory Architecture (UMA), where the same memory array is used for CPU main memory and graphics frame-buffer. This means a reduction in total system memory for system performances that are equal to that of a comparable frame buffer and system memory based system, and generally much better, due to the higher memory bandwidth allowed by attaching the graphics engine directly to the 64-bit processor host interface running at the speed of the processor bus rather than the traditional PCI bus. The 64-bit wide memory array provides the system with 528MB/s peak bandwidth. This allows for higher resolution screens and greater color depth.

The 'standard' PC chipset functions (DMA, interrupt controller, timers, power management logic) are integrated together with the x86 processor core; additional functions such as communications ports are accessed by the STPC Consumer-II via internal ISA bus.

The PCI bus is the main data communication link to the STPC Consumer-II chip. The STPC Consumer-II translates appropriate host bus I/O and Memory cycles onto the PCI bus. It also supports generation of Configuration cycles on the PCI bus. The STPC Consumer-II, as a PCI bus agent (host bridge class), fully complies with PCI specification 2.1. The chip-set also implements the PCI mandatory header registers in Type 0 PCI configuration space for easy porting of PCI aware system BIOS. The device contains a PCI arbitration function for three external PCI devices.

The STPC Consumer-II has two functional blocks *sharing the same balls* : The ISA / IPC / IDE block and the Local Bus / IDE block (see Table 3). Any board with the STPC Consumer-II should be built using only one of these two configurations. The IDE pins are dynamically multiplexed in each of the blocks in ISA mode only.

Configuration is done by 'strap options'. It is a set of pull-up or pull-down resistors on the memory data bus, checked on reset, which auto-configure the STPC Consumer-II.

1.2. GRAPHICS FEATURES

Graphics functions are controlled through the on-chip SVGA controller and the monitor display is produced through the 2D graphics display engine.

This Graphics Engine is tuned to work with the host CPU to provide a balanced graphics system with a low silicon area cost. It performs limited graphics drawing operations which include hardware acceleration of text, bitblts, transparent blts and fills. The results of these operations change the contents of the on-screen or off-screen frame buffer areas of SDRAM memory. The frame buffer can occupy a space up to 4 Mbytes anywhere in the physical main memory.

The graphics resolution supported is a maximum of 1280x1024 in 16M colors and 16M colors at 75Hz refresh rate, VGA and SVGA compatible. Horizontal timing fields are VGA compatible while the vertical fields are extended by one bit to accommodate above display resolution.

1.3. VIDEO FUNCTIONS

The STPC Consumer-II provides several additional functions to handle MPEG or similar video streams. The Video Input Port accepts an encoded digital video stream in one of a number of industry standard formats, decodes it, optionally decimates it, and deposits it into an off screen area of the frame buffer. An interrupt request can be generated when an entire field or frame has been captured. The video output pipeline incorporates a video-scaler and color space converter function and provisions in the CRT controller to display a video window. While repainting the screen the CRT controller fetches both the video as well as the normal non-video frame buffer in two separate internal FIFOs. The video stream can be color-space converted (optionally) and smooth scaled. Smooth interpolative scaling in both horizontal and vertical direction are implemented. Color and Chroma key functions are also implemented to allow mixing video stream with non-video frame buffer.

The video output passes directly to the RAMDAC for monitor output or through another optional color space converter (RGB to 4:2:2 YCrCb) to the programmable anti-flicker filter. The flicker filter is configured as either a two line filter with gamma correction (primarily designed for DOS type text)

or a 3 line flicker filter (primarily designed for Windows type displays). The fliker filter is optional and can be software disabled for use with large screen area's of video.

The Video output pipeline of the STPC Consumer-II interfaces directly to the internal digital TV encoder. It takes a 24 bit RGB non-interlaced pixel stream and converts to a multiplexed 4:2:2 YCrCb 8 bit output stream, the logic includes a progressive to interlaced scan converter and logic to insert appropriate CCIR656 timing reference codes into the output stream. It facilitates the high quality display of VGA or full screen video streams received via the Video input port to standard NTSC or PAL televisions.

The digital PAL/NTSC encoder outputs interlaced or non-interlaced video in PAL-B,D,G,H,I PAL-N, PAL-M or NTSC-M standards and "NTSC- 4.43" is also possible.

The four frame (for PAL) or 2 frame (for NTSC) burst sequences are internally generated, subcarrier generation being performed numerically with CKREF as reference. Rise and fall times of synchronisation tips and burst envelope are internally controlled according to the relevant ITU-R and SMPTE recommendations.

Video output signals are directed to four analog output pins through internal D/A converters giving, simultaneous R,G,B and composite CVBS outputs.

1.4. MEMORY CONTROLLER

The STPC handles the memory data (DATA) bus directly, controlling from 2 to 128 MBytes. The SDRAM controller supports accesses to the Memory Banks to/from the CPU (via the host), from the VMI, to/from the CRTC, to the VIDEO & to/from the GE. (Banks 0 to 3) which can be populated with either single or double sided 72-bit (4 bit parity) DIMMs. Parity is not supported.

The SDRAM controller only supports 64 bit wide Memory Banks.

Four Memory Banks (if DIMMS are used; Single sided or two double-sided DIMMs) are supported in the following configurations (see Table 1-1)

Table 1-1. Memory configurations

Memory Bank size	Number	Organisation	Device Size
1Mx64	4	1Mx16	
2Mx64	8	2Mx8	16Mbits
4Mx64	16	4Mx4	

Table 1-1. Memory configurations

Memory Bank size	Number	Organisation	Device Size
4Mx64	4	2Mx16x2	
8Mx64	8	4Mx8x2	
16Mx64	16	8Mx4x2	
4Mx64	4	1Mx16x4	64Mbits
8Mx64	8	2Mx8x4	
32Mx64	16	4Mx4x4	
16Mx64	8	2Mx16x2	
32Mx64	16	4Mx8x4	128Mbits

The SDRAM Controller supports buffered or unbuffered SDRAM but not EDO or FPM modes. SDRAMs must support Full Page Mode Type access.

The STPC Memory Controller provides various programmable SDRAM parameters to allow the SDRAM interface to be optimized for different processor bus speeds SDRAM speed grades and CAS Latency.

1.5. IDE INTERFACE

An industry standard EIDE (ATA 2) controller is built into the STPC Consumer-II. The IDE port is capable of supporting a total of four devices.

1.6. POWER MANAGEMENT

The STPC Consumer-II core is compliant with the Advanced Power Management (APM) specification to provide a standard method by which the BIOS can control the power used by personal computers. The Power Management Unit module (PMU) controls the power consumption providing a comprehensive set of features that control the power usage and supports compliance with the United States Environmental Protection Agency's Energy Star Computer Program. The PMU provides following hardware structures to assist the software in managing the power consumption by the system.

- System Activity Detection.
- Three power down timers.
- Doze timer for detecting lack of system activity for short durations.
- Stand-by timer for detecting lack of system activity for medium durations
- Suspend timer for detecting lack of system activity for long durations.
- House-keeping activity detection.
- House-keeping timer to cope with short bursts of house-keeping activity while dozing or in stand-by state.

- Peripheral activity detection.
- Peripheral timer for detecting lack of peripheral activity
- SUSP# modulation to adjust the system performance in various power down states of the system including full power on state.
- Power control outputs to disable power from different planes of the board.

Lack of system activity for progressively longer period of times is detected by the three power down timers. These timers can generate SMI interrupts to CPU so that the SMM software can put the system in decreasing states of power consumption. Alternatively, system activity in a power down state can generate SMI interrupt to allow the software to bring the system back up to full power on state. The chip-set supports up to three power down states: Doze state, Stand-by state and Suspend mode. These correspond to decreasing levels of power savings.

Power down puts the STPC Consumer-II into suspend mode. The processor completes execution of the current instruction, any pending decoded instructions and associated bus cycles. During the suspend mode, internal clocks are stopped. Removing power down, the processor resumes instruction fetching and begins execution in the instruction stream at the point it had stopped. Because of the static nature of the core, no internal data is lost.

1.7. JTAG

JTAG stands for Joint Test Action Group and is the popular name for IEEE Std. 1149.1, Standard Test Access Port and Boundary-Scan Architec-ture. This built-in circuitry is used to assist in the test, maintenance and support of functional circuit blocks. The circuitry includes a standard interface through which instructions and test data are communicated. A set of test features is defined, including a boundary-scan register so that a component is able to respond to a minimum set of test instructions.

Figure 1-1. Functional description.
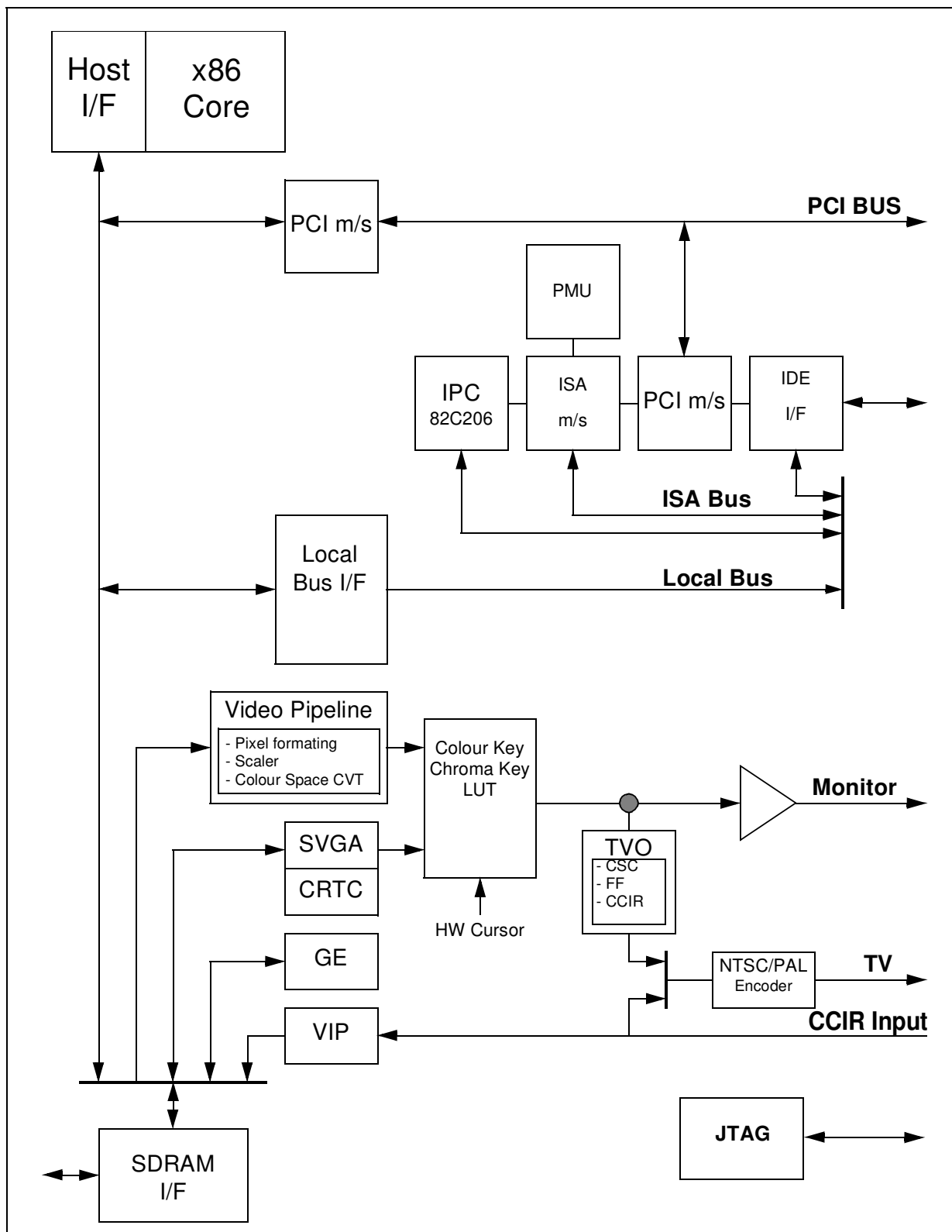
1.8. CLOCK TREE

The STPC Atlas integrates many features and generates all its clocks from a single 14MHz oscillator. This results in multiple clock domains as described in Figure 1-2.

The speed of the PLLs is either fixed (DEVCLK), either programmable by strap option (HCLK) either programmable by software (DCLK, MCLK). When in synchronized mode, MCLK speed is fixed to HCLKO speed and HCLKI is generated from MCLKI.

Figure 1-2. STPC Consumer-II clock architecture
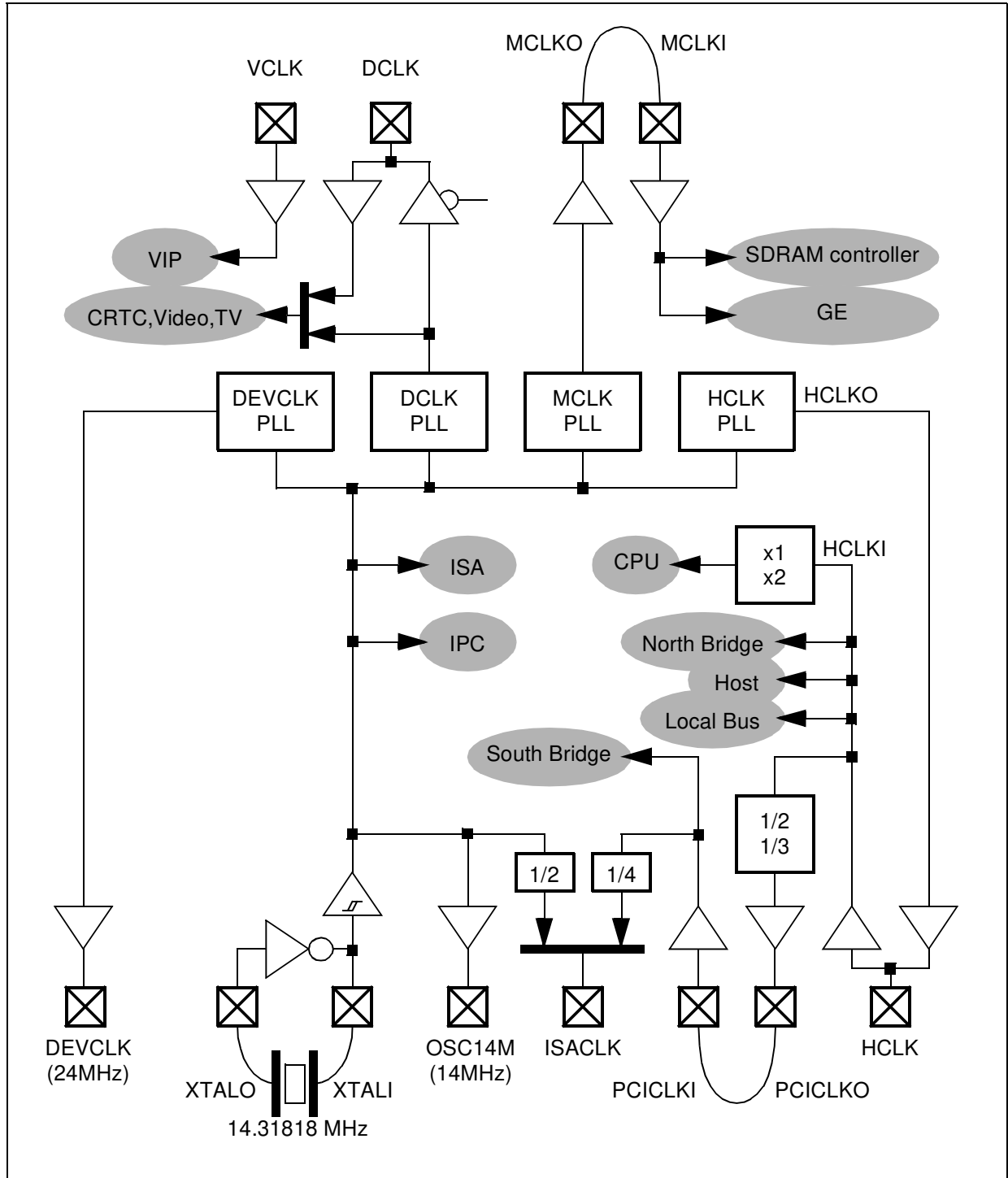
Figure 1-3. Typical ISA-based Application.
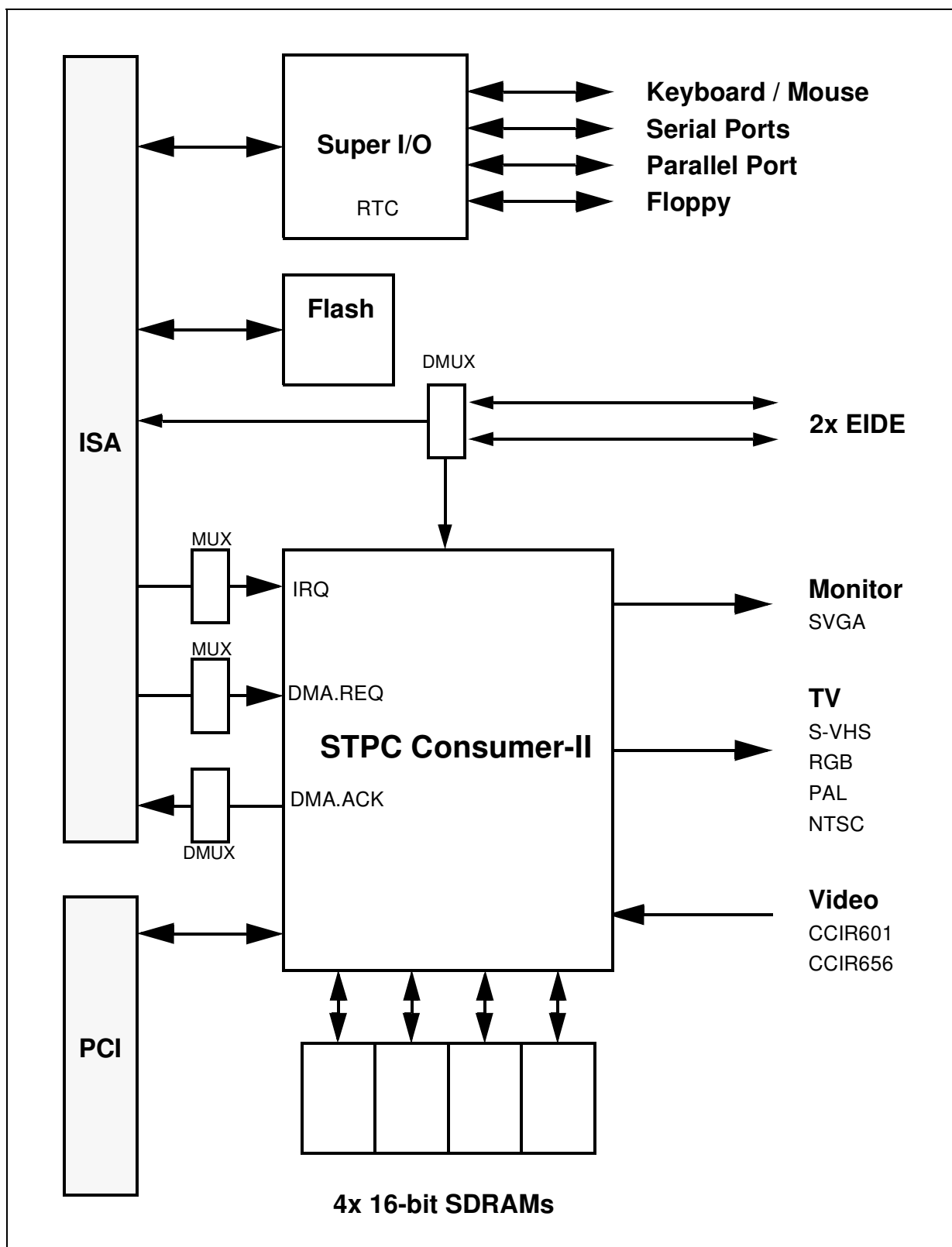
2. PIN DESCRIPTION

2.1. INTRODUCTION

The STPC Consumer-II integrates most of the functionality of the PC architecture. As a result, many of the traditional interconnections between the host PC microprocessor and the peripheral devices are totally internal to the STPC Consumer-II. This offers improved performance due to the tight coupling of the processor core and these peripherals. As a result, many of the external pin connections are made directly to the on-chip peripheral functions.

Figure 2-1 shows the STPC Consumer-II external interfaces. It defines the main buses and their functions. Table 2-1 describes the physical implementation, listing signal type and functionality. Table 2-2 provides a full pin listing and description of pins. Table 2-7 provides a full listing of pin locations of the STPC Consumer-II package by physical connection.

Table 2-1. Signal Description

Group name	Qty	
Basic Clocks reset & Xtal (SYS)		7
SDRAM Controller		95
PCI interface		56
ISA	79	
IDE	34	89
Local Bus	49	
Video Input		9
TV Output		12
VGA Monitor interface		8
Grounds		71
V_{DD}		26
Miscellaneous		9
Unconnected		6
Total Pin Count		388

Note: Several interface pins are multiplexed with other functions, refer to Table 2-4 and Table 2-5 for further details

Figure 2-1. STPC Consumer-II External Interfaces

Table 2-2. Definition of Signal Pins

Signal Name	Dir	Buffer Type[2]	Description	Qty
BASIC CLOCKS AND RESETS				
SYSRSETI#	I	SCHMITT_FT	System Power Good Input	1
SYSRSTO#	O	BD8STRP_FT	System Reset Output	1
XTALI	I	ANA	14.3 MHz Crystal Input- External Oscillator Input	1
XTALO	I/O	OSCI13B	14.3 MHz Crystal Output	1
HCLK	I/O	BD4STRP_FT	Host Clock (Test)	1
DEV_CLK	O	BT8TRP_TC	24 MHz Peripheral Clock (floppy drive)	1
DCLK	I/O	BD4STRP_FT	27-135 MHz Graphics Dot Clock	1
V_{DD}_xxx_PLL[1]		VDDCO	Power Supply for PLL Clocks	
SDRAM CONTROLLER				
MCLKI	I	TLCHT_TC	Memory Clock Input	1
MCLKO	O	BT8TRP_TC	Memory Clock Output	1
CS#[1:0]	O	BD8STRP_TC	DIMM Chip Select	2
CS2# / MA11	O	BD16STARUQP_TC	DIMM Chip Select / Memory Address	1
CS3# / MA12 / BA1	O	BD16STARUQP_TC	DIMM Chip Select / Memory Address / Bank Address	1
BA[0]	O	BD8STRP_TC	Bank Address	1
MA[10:0]	O	BD16STARUQP_TC	Memory Row & Column Address	12
MD[63:49]	I/O	BD8STRUP_FT	Memory Data	15
MD[48:1]	I/O	BD8TRP_TC	Memory Data	48
MD[0]	I/O	BD8STRUP_FT	Memory Data	1
RAS#[1:0]	O	BD16STARUQP_TC	Row Address Strobe	2
CAS#[1:0]	O	BD16STARUQP_TC	Column Address Strobe	2
MWE#	O	BD16STARUQP_TC	Write Enable	1
DQM[7:0]	O	BD8STRP_TC	Data Input/Output Mask	8
PCI CONTROLLER				
PCI_CLKI	I	TLCHT_FT	33 MHz PCI Input Clock	1
PCI_CLKO	O	BT8TRP_TC	33 MHz PCI O/P Clk (from internal PLL)	1
AD[31:0]	I/O	BD8PCIARP_FT	PCI Address / Data	32
CBE[3:0]	I/O	BD8PCIARP_FT	Bus Commands / Byte Enables	4
FRAME#	I/O	BD8PCIARP_FT	Cycle Frame	1
IRDY#	I/O	BD8PCIARP_FT	Initiator Ready	1
TRDY#	I/O	BD8PCIARP_FT	Target Ready	1
LOCK#	I	TLCHT_FT	PCI Lock	1
DEVSEL#	I/O	BD8PCIARP_FT	Device Select	1
STOP#	I/O	BD8PCIARP_FT	Stop Transaction	1
PAR	I/O	BD8PCIARP_FT	Parity Signal Transactions	1
SERR#	O	BD8PCIARP_FT	System Error	1
PCIREQ#[2:0]	I	BD8PCIARP_FT	PCI Request	3
PCIGNT#[2:0]	O	BD8PCIARP_FT	PCI Grant	3
PCI_INT#[3:0]	I	BD4STRUP_FT	PCI Interrupt Request	4

Note[1]: These pins are must be connected to the 2.5 V power supply. They **must not** be connected to the 3.3 V supply.
Note[2]: See Table 2-3 for buffer type descriptions

Table 2-2. Definition of Signal Pins

Signal Name	Dir	Buffer Type[2]	Description	Qty
ISA INTERFACE				
ISA_CLK	O	BT8TRP_TC	ISA Clock Output Multiplexer Select Line For IPC	1
ISA_CLK2X	O	BT8TRP_TC	ISA Clock x2 Output Multiplexer Select Line For IPC	1
OSC14M	O	BD8STRP_FT	ISA bus synchronisation clock	1
LA[23:17]	O	BD8STRUP_FT	Unlatched Address	7
SA[19:0]	I/O	BD8STRUP_FT	Latched Address	20
SD[15:0]	I/O	BD8STRP_FT	Data Bus	16
ALE	O	BD4STRP_FT	Address Latch Enable	1
MEMR#, MEMW#	I/O	BD8STRUP_FT	Memory Read and Write	2
SMEMR#, SMEMW#	O	BD8STRP_FT	System MemoryRead and Write	2
IOR#, IOW#	I/O	BD8STRUP_FT	I/O Read and Write	2
MCS16#, IOCS16#	I	BD4STRUP_FT	Memory and I/O ChipSelect16	2
BHE#	O	BD8STRUP_FT	System Bus High Enable	1
ZWS#	I	BD4STRP_FT	Zero Wait State	1
REF#	O	BD8STRP_FT	Refresh Cycle.	1
MASTER#	I	BD4STRUP_FT	Add On Card Owns Bus	1
AEN	O	BD8STRUP_FT	Address Enable	1
IOCHCK#	I	BD4STRUP_FT	I/O Channel Check.	1
IOCHRDY	I/O	BD8STRUP_FT	I/O Channel Read	1
ISAOE#	O	BD4STRP_FT	ISA/IDE Selection	1
GPIOCS#	I/O	BD4STRP_FT	General Purpose Chip Select	1
IRQ_MUX[3:0]	I	BD4STRP_FT	Time-Multiplexed Interrupt Request	4
DREQ_MUX[1:0]	I	BD4STRP_FT	Time-Multiplexed DMA Request	2
DACK_ENC[2:0]	O	BD4STRP_FT	Encoded DMA Acknowledge	3
TC	O	BD4STRP_FT	ISA Terminal Count	1
RTCAS	O	BD4STRP_FT	Real Time Clock Address Strobe	1
RMRTCCS#	I/O	BD4STRP_FT	ROM/RTC Chip Select	1
KBCS#	I/O	BD4STRP_FT	Keyboard Chip Select	1
RTCRW#	I/O	BD4STRP_FT	RTC Read/Write	1
RTCDS#	I/O	BD4STRP_FT	RTC Data Strobe	1
LOCAL BUS INTERFACE				
PA[23:0]	O	BD4STRP_FT	Address Bus	24
PD[15:0]	I/O	BD8STRP_FT	Data Bus	16
PRD1#,PRD0#	O	BD4STRUP_FT	Peripheral Read Control	2
PWR1#,PWR0#	O	BD4STRUP_FT	Peripheral Write Control	2
PRDY	I	BD8STRUP_FT	Data Ready	1
FCS1#, FCS0#	O	BD4STRP_FT	Flash Chip Select	2
IOCS#[3:0]	O	BD8STRUP_FT	I/O Chip Select	4
IDE CONTROLLER				
DA[2:0]	O	BD8STRUP_FT	Address Bus	3
DD[15:0]	I/O	BD8STRUP_FT	Data Bus	16

Note[1]: These pins are must be connected to the 2.5 V power supply. They **must not** be connected to the 3.3 V supply.
Note[2]: See Table 2-3 for buffer type descriptions

Table 2-2. Definition of Signal Pins

Signal Name	Dir	Buffer Type[2]	Description	Qty
PCS3#,PCS1#,SCS3#,SCS1#	O	BD8STRUP_FT	Primary & Secondary Chip Selects	4
DIORDY	O	BD8STRUP_FT	Data I/O Ready	1
PIRQ, SIRQ	I	BD4STRP_FT	Primary & Secondary Interrupt Request	2
PDRQ, SDRQ	I	BD4STRP_FT	Primary & Secondary DMA Request	2
PDACK#, SDACK#	O	BD8STRP_FT	Primary & Secondary DMA Acknowledge	2
PDIOR#, SDIOR#	O	BD8STRUP_FT	Primary & Secondary I/O Channel Read	2
PDIOW#, SDIOW#	O	BD8STRUP_FT	Primary & Secondary I/O Channel Write	2
VGA CONTROLLER				
RED, GREEN, BLUE	O	VDDCO	Analog Red, Green, Blue	3
VSYNC	O	BD4STRP_FT	Vertical Sync	1
HSYNC	O	BD4STRP_FT	Horizontal Sync	1
VREF_DAC[1]	I	ANA	DAC Voltage reference	1
RSET	I	ANA	Resistor Set	1
COMP	I	ANA	Compensation	1
COL_SEL	O	BD4STRP_FT	Colour Select	1
VIDEO INPUT PORT				
VCLK	I	BD8STRP_FT	27-33 MHz Video Input Port Clock	1
VIN[7:0]	I	BD4STRP_FT	CCIR 601 or 656 YUV Video Data Input	8
ANALOG TV OUTPUT PORT				
RED_TV, GREEN_TV, BLUE_TV	O	VDDCO	Analog RGB or S-VHS outputs	3
CVBS	O	VDDCO	Analog video composite output	1
IREF1_TV	I	ANA	Reference current of CVBS DAC	1
VREF1_TV	I	ANA	Reference voltage of CVBS DAC	1
IREF2_TV	I	ANA	Reference current of RGB DAC	1
VREF2_TV	I	ANA	Reference voltage of RGB DAC	1
VSSA_TV	I		Analog Vss for DAC	1
VDDA_TV	I	VDDCO	Analog Vdd for DAC	1
VCS	I/O	BD4STRP_FT	Composite Synchro Horizontal Line Synchro	1
ODD_EVEN	I/O	BD4STRP_FT	Frame Synchronisation	1
MISCELLANEOUS				
SPKRD	O	BD4STRP_FT	Speaker Device Output	1
SCL	I/O	BD4STRUP_FT	I²C Interface - Clock Can be used for VGA DDC[1] signal	1
SDA	I/O	BD4STRUP_FT	I²C Interface - Data Can be used for VGA DDC[0] signal	1
SCAN_ENABLE	I	TLCHTD_TC	Reserved (Test pin)	1
TCLK	I	TLCHT_FT	Test Clock	1
TDI	I	TLCHT_FT	Test Data Input	1
TMS	I	TLCHT_FT	Test Mode Set	1
TDO	O	BT8TRP_TC	Test Data output	1

Note[1]: These pins are must be connected to the 2.5 V power supply. They **must not** be connected to the 3.3 V supply.
Note[2]: See Table 2-3 for buffer type descriptions

Table 2-3. Buffer Type Descriptions

Buffer	Description
ANA	Analog pad buffer
OSCI13B	Oscillator, 13 MHz, HCMOS
BT8TRP_TC	Tri-State output buffer, 8 mA drive capability, Schmitt trigger with slew rate control and P, TC
BD4STRP_FT	LVTTL Bi-Directional, 4 mA drive capability, Schmitt trigger, 5V tolerant
BD4STRUP_FT	LVTTL Bi-Directional, 4 mA drive capability, Schmitt trigger, Pull-Up, 5V tolerant
BD8STRP_FT	LVTTL Bi-Directional, 8 mA drive capability, Schmitt trigger, 5V tolerant
BD8STRUP_FT	LVTTL Bi-Directional, 8 mA drive capability, Schmitt trigger, Pull-Up, 5V tolerant
BD8STRP_TC	LVTTL Bi-Directional, 8 mA drive capability, Schmitt trigger
BD8TRP_TC	LVTTL Bi-Directional, 8 mA drive capability, Schmitt trigger
BD8PCIARP_FT	LVTTL Bi-Directional, 8 mA drive capability, PCI compatible, 5V tolerant
BD16STARUQP_TC	LVTTL Bi-Directional, 16 mA drive capability, Schmitt trigger
SCHMITT_FT	LVTTL Input, Schmitt trigger, 5V tolerant
TLCHT_FT	LVTTL Input, 5V tolerant
TLCHT_TC	LVTTL Input
TLCHTD_TC	LVTTL Input, Pull-Down
VDDCO	Internal supply for core only power pad

2.2. SIGNAL DESCRIPTIONS

2.2.1. BASIC CLOCKS AND RESETS

SYSRSTI# *System Reset/Power good.* This input is low when the reset switch is depressed. Otherwise, it reflects the power supply power good signal. This input is asynchronous to all clocks, and acts as a negative active reset. The reset circuit initiates a hard reset on the rising edge of this signal.

SYSRSTO# *Reset Output to System.* This is the system reset signal and is used to reset the rest of the components (not on Host bus) in the system. The ISA bus reset is an externally inverted buffered version of this output and the PCI bus reset is an externally buffered version of this output.

XTALI *14.3 MHz Crystal Input*
XTALO *14.3 MHz Crystal Output.* These pins are provided for the connection of an external 14.318 MHz crystal to provide the reference clock for the internal frequency synthesizer, from which all other clock signals are generated.

The 14.318 MHz series-cut fundamental (not overtone) mode quartz crystal must have an Equivalent Series Resistance (ESR, sometimes referred to as Rm) of less then 50 Ohms (typically 8 Ohms) and a shunt capacitance (Co) of less than 7 pF. Balance capacitors of 16 pF should also be added, one connected to each pin.

In the event of an external oscillator providing the master clock signal to the STPC Consumer-II device, the LVTTL signal should be connected to XTALI.

HCLK *Host Clock.* This clock supplies the CPU and the host related blocks. This clock can be doubled inside the CPU and is intended to operate in the range of 25 MHz to 100 MHz. This clock is generated internally from a PLL but can be driven directly from the external system.

DEV_CLK *24 MHz Peripheral Clock.* This 24 MHz signal is provided as a convenience for the system integration of a Floppy Disk driver function in an external chip.

DCLK *135 MHz Dot Clock.* This is the dot clock, which drives graphics display cycles. Its frequency can go from 8 MHz (using internal PLL) up to 135 MHz, and it is required to have a worst case duty cycle of 60-40.
This signal is driven either by the internal pll (VGA) or by an external 27 MHz oscillator (when the composite video output is enabled). The direction can be controlled by a strap option or an internal register bit.

2.2.2. SDRAM CONTROLLER

MCLKO *Memory Clock Output.* This clock is driving the DIMMs on board and is generated from an internal PLL. The default value is 66 MHz.

MCLKI *Memory Clock Input.* This clock is driving the SDRAM controller, the graphics engine and display controller. This input should be a buffered version of the MCLKO signal with the track lengths between the buffer and the pin matched with the track lengths between the buffer and the DIMMs.

CS#[1:0] *Chip Select* These signals are used to disable or enable device operation by masking or enabling all SDRAM inputs except MCLK, CKE, and DQM.

CS#[2]/MA[11] *Chip Select/Bank Address* This pin is CS#[2] in the case when 16-Mbit devices are used. For all other densities, it becomes MA[11].

CS#[3]/MA[12]/BA[1] *Chip Select/Memory Address/Bank Address* This pin is CS#[3] in the case when 16-Mbit devices are used. For all other densities, it becomes MA[12] when two internal banks devices are used and BA[1] when four internal bank devices are used.

MA[10:0] *Memory Address.* Multiplexed row and column address lines.

BA[0] *Memory Bank Address.*

MD[63:0] *Memory Data.* This is the 64-bit memory data bus. MD[40-0] are read by the device strap option registers during rising edge of SYSRSTI#.

RAS#[1:0] *Row Address Strobe.* There are two active-low row address strobe output signals. The RAS# signals drive the memory devices directly without any external buffering.

CAS#[1:0] *Column Address Strobe.* There are two active-low column address strobe output signals. The CAS# signals drive the memory devices directly without any external buffering.

MWE# *Write Enable.* Write enable specifies whether the memory access is a read (MWE# = H) or a write (MWE# = L).

DQM#[7:0] *Data Mask.* Makes data output Hi-Z after the clock and masks the SDRAM outputs. Blocks SDRAM data input when DQM active.

2.2.3. PCI CONTROLLER

PCI_CLKI *33 MHz PCI Input Clock.* This signal is the PCI bus clock input and should be driven from the PCI_CLKO pin.

PCI_CLKO *33 MHz PCI Output Clock.* This is the master PCI bus clock output.

AD[31:0] *PCI Address/Data.* This is the 32-bit multiplexed address and data bus of the PCI. This bus is driven by the master during the address phase and the data phase of write transactions. It is driven by the target during the data phase of read transactions.

CBE#[3:0] *Bus Commands/Byte Enables.* These are the multiplexed command and byte enable signals of the PCI bus. During the address phase they define the command and during the data phase they carry the byte enable information. These pins are inputs when a PCI master other than the STPC Consumer-II owns the bus and outputs when the STPC Consumer-II owns the bus.

FRAME# *Cycle Frame.* This is the frame signal of the PCI bus. It is an input when a PCI master owns the bus and is an output when STPC Consumer-II owns the PCI bus.

IRDY# *Initiator Ready.* This is the initiator ready signal of the PCI bus. It is used as an output when the STPC Consumer-II initiates a bus cycle on the PCI bus. It is used as an input during the PCI cycles targeted to the STPC Consumer-II to determine when the current PCI master is ready to complete the current transaction.

TRDY# *Target Ready.* This is the target ready signal of the PCI bus. It is driven as an output when the STPC Consumer-II is the target of the current bus transaction. It is used as an input when STPC Consumer-II initiates a cycle on the PCI bus.

LOCK# *PCI Lock.* This is the lock signal of the PCI bus and is used to implement the exclusive bus operations when acting as a PCI target agent.

DEVSEL# *I/O Device Select.* This signal is used as an input when the STPC Consumer-II initiates a bus cycle on the PCI bus to determine if a PCI slave device has decoded itself to be the target of the current transaction. It is asserted as an output, either when the STPC Consumer-II is the target of the current PCI transaction, or when no other device asserts DEVSEL# prior to the subtractive decode phase of the current PCI transaction.

STOP# *Stop Transaction.* Stop is used to implement the disconnect, retry and abort protocol of the PCI bus. It is used as an input for the bus cycles initiated by the STPC Consumer-II and is used as an output when a PCI master cycle is targeted to the STPC Consumer-II.

PAR *Parity Signal Transactions.* This is the parity signal of the PCI bus. This signal is used to guarantee even parity across AD[31:0], CBE#[3:0], and PAR. This signal is driven by the master during the address phase and data phase of write transactions. It is driven by the target during data phase of read transactions (its assertion is identical to that of the AD bus delayed by one PCI clock cycle).

SERR# *System Error.* This is the system error signal of the PCI bus. It may, if enabled, be asserted for one PCI clock cycle if target aborts a STPC Consumer-II initiated PCI transaction. Its assertion by either the STPC Consumer-II or by another PCI bus agent will trigger the assertion of NMI to the host CPU. This is an open drain output.

PCIREQ#[2:0] *PCI Request.* These are the three external PCI master request pins. They indicates to the PCI arbiter that external agents desire use of the bus.

PCIGNT#[2:0] *PCI Grant.* These pins indicate that the PCI bus has been granted to the master requesting it on its PCIREQ#.

PCI_INT#[3:0] *PCI Interrupt Request.* These are the PCI bus interrupt signals.

2.2.4. ISA INTERFACE

ISA_CLK, ISA_CLKX2 *ISA Clock x1, x2.* These pins generate the Clock signal for the ISA bus and a Doubled Clock signal. They are also used as the multiplexer control lines for the Interrupt Controller Interrupt input lines. ISA_CLK is generated from either PCICLK/4 or OSC14M/ 2.

OSC14M *ISA bus synchronisation clock Output.* This is the buffered 14.318 MHz clock for the ISA bus.

LA[23:17] *Unlatched Address.* When the ISA bus is active, these pins are ISA Bus unlatched address for 16-bit devices. When ISA bus is accessed by any cycle initiated from PCI bus, these pins are in output mode. When an ISA bus master owns the bus, these pins are in input mode.

SA[19:0] *ISA Address Bus.* System address bus of ISA on 8-bit slot. These pins are used as an input when an ISA bus master owns the bus and are outputs at all other times.

SD[15:0] *I/O Data Bus.* These pins are the external data bus to the ISA bus.

ALE *Address Latch Enable.* This is the address latch enable output of the ISA bus and is asserted by the STPC Consumer-II to indicate that LA23-17, SA19-0, AEN and SBHE# signals are valid. The ALE is driven high during refresh, DMA

master or an ISA master cycles by the STPC Consumer-II. ALE is driven low after reset.

MEMR# *Memory Read.* This is the memory read command signal of the ISA bus. It is used as an input when an ISA master owns the bus and is an output at all other times.
The MEMR# signal is active during refresh.

MEMW# *Memory Write.* This is the memory write command signal of the ISA bus. It is used as an input when an ISA master owns the bus and is an output at all other times.

SMEMR# *System Memory Read.* The STPC Consumer-II generates SMEMR# signal of the ISA bus only when the address is below one megabyte or the cycle is a refresh cycle.

SMEMW# *System Memory Write.* The STPC Consumer-II generates the SMEMW# signal of the ISA bus only when the address is below one megabyte.

IOR# *I/O Read.* This is the IO read command signal of the ISA bus. It is an input when an ISA master owns the bus and is an output at all other times.

IOW# *I/O Write.* This is the IO write command signal of the ISA bus. It is an input when an ISA master owns the bus and is an output at all other times.

MCS16# *Memory Chip Select16.* This is the decode of LA23-17 address pins of the ISA address bus without any qualification of the command signal lines. MCS16# is always an input. The STPC Consumer-II ignores this signal during IO and refresh cycles.

IOCS16# *IO Chip Select16.* This signal is the decode of SA15-0 address pins of the ISA address bus without any qualification of the command signals. The STPC Consumer-II does not drive IOCS16# (similar to PC-AT design). An ISA master access to an internal register of the STPC Consumer-II is executed as an extended 8-bit IO cycle.

BHE# *System Bus High Enable.* This signal, when asserted, indicates that a data byte is being transferred on SD15-8 lines. It is used as an input when an ISA master owns the bus and is an output at all other times.

ZWS# *Zero Wait State.* This signal, when asserted by an addressed device, indicates that the current cycle can be shortened.

REF# *Refresh Cycle.* This is the refresh command signal of the ISA bus. It is driven as an output when the STPC Consumer-II performs a refresh cycle on the ISA bus. It is used as an input when

an ISA master owns the bus and is used to trigger a refresh cycle.
The STPC Consumer-II performs a pseudo hidden refresh. It requests the host bus for two host clocks to drive the refresh address and capture it in external buffers. The host bus is then relinquished while the refresh cycle continues on the ISA bus.

MASTER# *Add On Card Owns Bus.* This signal is active when an ISA device has been granted bus ownership.

AEN *Address Enable.* Address Enable is enabled when the DMA controller is the bus owner to indicate that a DMA transfer will occur. The enabling of the signal indicates to IO devices to ignore the IOR#/IOW# signal during DMA transfers.

IOCHCK# *IO Channel Check.* IO Channel Check is enabled by any ISA device to signal an error condition that can not be corrected. The NMI signal becomes active on seeing IOCHCK# active if the corresponding bit in Port B is enabled.

IOCHRDY *Channel Ready.* IOCHRDY is the IO channel ready signal of the ISA bus and is driven as an output in response to an ISA master cycle targeted to the host bus or an internal register of the STPC Consumer-II. The STPC Consumer-II monitors this signal as an input when performing an ISA cycle on behalf of the host CPU, DMA master or refresh.
ISA masters which do not monitor IOCHRDY are not guaranteed to work with the STPC Consumer-II since the access to the system memory can be considerably delayed due UMA architecture.

ISAOE# *Bidirectional OE Control.* This signal controls the OE signal of the external transceiver that connects the IDE DD bus and ISA SA bus.

GPIOCS# *I/O General Purpose Chip Select.* This output signal is used by the external latch on ISA bus to latch the data on the SD[7:0] bus. The latch can be use by PMU unit to control the external peripheral devices or any other desired function.

IRQ_MUX[3:0] *Multiplexed Interrupt Request.* These are the ISA bus interrupt signals. They have to be encoded before connection to the STPC Consumer-II using ISACLK and ISACLKX2 as the input selection strobes.
Note that IRQ8B, which by convention is connected to the RTC, is inverted before being sent to the interrupt controller, so that it may be connected directly to the IRQ pin of the RTC.

DREQ_MUX[1:0] *ISA Bus Multiplexed DMA Request.* These are the ISA bus DMA request signals. They are to be encoded before connection to the STPC Consumer-II using

ISACLK and ISACLKX2 as the input selection strobes.

DACK_ENC[2:0] *DMA Acknowledge.* These are the ISA bus DMA acknowledge signals. They are encoded by the STPC Consumer-II before output and should be decoded externally using ISACLK and ISACLKX2 as the control strobes.

TC *ISA Terminal Count.* This is the terminal count output of the DMA controller and is connected to the TC line of the ISA bus. It is asserted during the last DMA transfer, when the byte count expires.

RTCAS *Real time clock address strobe.* This signal is asserted for any I/O write to port 70H.

RMRTCCS# *ROM/Real Time clock chip select.* This signal is asserted if a ROM access is decoded during a memory cycle. It should be combined with MEMR# or MEMW# signals to properly access the ROM. During a IO cycle, this signal is asserted if access to the Real Time Clock (RTC) is decoded. It should be combined with IOR or IOW# signals to properly access the real time clock.

KBCS# *Keyboard Chip Select.* This signal is asserted if a keyboard access is decoded during a I/O cycle.

RTCRW# *Real Time Clock R$\overline{W}$.* This pin is a multi-function pin. When ISAOE# is active, this signal is used as RTCRW#. This signal is asserted for any I/O write to port 71H.

RTCDS# *Real Time Clock DS.* This pin is a multi-function pin. When ISAOE# is active, this signal is used as RTCDS#. This signal is asserted for any I/O read to port 71H. Its polarity complies with the DS pin of the MT48T86 RTC device when configured with Intel timings.

Note: RMRTCCS#, KBCS#, RTCRW# and RTCDS# signals must be ORed externally with ISAOE# and then connected to the external device. An LS244 or equivalent function can be used if OE# is connected to ISAOE# and the output is provided with a weak pull-up resistor as shown in Figure 6-10.

2.2.5. LOCAL BUS INTERFACE

PA[23:0] *Address Bus Output.*

PD[15:0] *Data Bus.* This is the 16-bit data bus. D[7:0] is the LSB and PD[15:8] is the MSB.

PRD#[1:0] *Read Control output.* PRD0# is used to read the LSB and PRD1# to read the MSB.

PWR#[1:0] *Write Control output.* PWR0# is used to write the LSB and PWR1# to write the MSB.

PRDY *Data Ready input.* This signal is used to create wait states on the bus. When high, it completes the current cycle.

FCS#[1:0] *Flash Chip Select output.* These are the Programmable Chip Select signals for up to two banks of Flash memory.

IOCS#[3:0] *I/O Chip Select output.* These are the Programmable Chip Select signals for up to four external I/O devices.

2.2.6. IDE INTERFACE

SCS1#, SCS3# *Secondary Chip Select.* These signals are used as the active high secondary master & slave IDE chip select signals. These signals must be externally ANDed with the ISAOE# signal before driving the IDE devices to guarantee it is active only when ISA bus is idle.

DA[2:0] *Address.* These signals are connected to DA[2:0] of IDE devices directly or through a buffer. If the toggling of signals are to be masked during ISA bus cycles, they can be externally ORed with ISAOE# before being connected to the IDE devices.

DD[15:0] *Databus.* When the IDE bus is active, they serve as IDE signals DD[11:0]. IDE devices are connected to SA[19:8] directly and ISA bus is connected to these pins through two LS245 transceivers as described in Figure 6-10.

PCS1#, PCS3# *Primary Chip Select.* These signals are used as the active high primary master & slave IDE chip select signals. These signals must be externally ANDed with the ISAOE# signal before driving the IDE devices to guarantee it is active only when ISA bus is idle.

DIORDY *Busy/Ready.* This pin serves as IDE signal DIORDY.

PIRQ *Primary Interrupt Request.*
SIRQ *Secondary Interrupt Request.*
Interrupt request from IDE channels.

PDRQ *Primary DMA Request.*
SDRQ *Secondary DMA Request.*
DMA request from IDE channels.

PDACK# *Primary DMA Acknowledge.*
SDACK# *Secondary DMA Acknowledge.*
DMA acknowledge to IDE channels.

PDIOR#, PDIOW# *Primary I/O Read & Write.*
SDIOR#, SDIOW# *Secondary I/O Read & Write.*
Primary & Secondary channel read & write.

2.2.7. VGA CONTROLLER

RED, GREEN, BLUE *RGB Video Outputs.* These are the three analog colour outputs from the RAMDACs. These signals are sensitive to interference, therefore they need to be properly shielded.

VSYNC *Vertical Synchronisation Pulse.* This is the vertical synchronization signal from the VGA controller.

HSYNC *Horizontal Synchronisation Pulse.* This is the horizontal synchronization signal from the VGA controller.

VREF_DAC *DAC Voltage reference.* An external voltage reference is connected to this pin to bias the DAC.

RSET *Resistor Current Set.* This reference current input to the RAMDAC is used to set the full-scale output of the RAMDAC.

COMP *Compensation.* This is the RAMDAC compensation pin. Normally, an external capacitor (typically 10nF) is connected between this pin and V_{DD} to damp oscillations.

2.2.8. VIDEO INPUT PORT

VCLK *Pixel Clock Input.* This signal is used to synchronise data being transferred from an external video device to either the frame buffer, or alternatively out the TV output in bypass mode. This pin can be sourced from STPC if no external VCLK is detected, or can be input from an external video clock source.

VIN[7:0] *YUV Video Data Input CCIR 601 or 656.* Time multiplexed 4:2:2 luminance and chrominance data as defined in ITU-R Rec601-2 and Rec656 (except for TTL input levels). This bus typically carries a stream of Cb,Y,Cr,Y digital video at VCLK frequency, clocked on the rising edge (by default) of VCLK.

2.2.9. ANALOG TV OUTPUT PORT

RED_TV / **C_TV** *Analog video outputs synchronized with CVBS.* This output is current-driven and must be connected to analog ground over a load resistor (R_{LOAD}). Following the load resistor, a simple analog low pass filter is recommended. In S-VHS mode, this is the Chrominance Output.

GREEN_TV / **Y_TV** *Analog video outputs synchronized with $\overline{CVBS}$.* This output is current-driven and must be connected to analog ground over a load resistor (R_{LOAD}). Following the load resistor, a simple analog low pass filter is

recommended. In S-VHS mode, this is the Luminance Output.

BLUE_TV / **CVBS** *Analog video outputs synchronized with CVBS.* This output is current-driven and must be connected to analog ground over a load resistor (R_{LOAD}). Following the load resistor, a simple analog low pass filter is recommended. In S-VHS mode, this is a second composite output.

CVBS *Analog video composite output (luminance/chrominance).* CVBS is current-driven and must be connected to analog ground over a load resistor (R_{LOAD}). Following the load resistor, a simple analog low pass filter is recommended.

IREF1_TV *Ref. current* for CVBS 10-bit DAC.

IREF2_TV *Reference current* for RGB 10-bit DAC.

VREF1_TV *Ref. voltage* for CVBS 10-bit DAC. Connect to analog ground.

VREF2_TV *Reference voltage* for RGB 10-bit DAC. Connect to analog ground.

VSSA_TV *Analog V_{SS}* for DACs.

VDDA_TV *Analog V_{DD}* for DACs.

JTAG Signals

VCS *Line synchronisation Output.* This pin is an input in ODDEV+HSYNC or VSYNC + HSYNC or VSYNC slave modes and an output in all other modes (master/slave)

ODD_EVEN *Frame Synchronisation Output.* This pin supports the Frame synchronisation signal. It is an input in slave modes, except when sync is extracted from YCrCbdata, and an output in master mode and when sync is extracted from YCrCb data
The signal is synchronous to rising edge of DCLK. The default polarity for this pin is:
- odd (not-top) field: LOW level
- even (bottom) field: HIGH level

2.2.10. MISCELLANEOUS

SPKRD *Speaker Drive.* This the output to the speaker. It is an AND of the counter 2 output with bit 1 of Port 61, and drives an external speaker driver. This output should be connected to 7407 type high voltage driver.

SCL, SDA *I²C Interface.* These bidirectional pins are connected to CRTC register 3Fh to implement DDC capabilities. They conform to I²C electrical specifications, they have open-collector output drivers which are internally connected to V_{DD} through pull-up resistors.

They can be used for the DDC1 (SCL) and DDC0 (SDA) lines of the VGA interface.

SCAN_ENABLE *Reserved*. The pin is reserved for Test and Miscellaneous functions.

COL_SEL *Colour Select.* Can be used for Picture in Picture function. Note however that this signal, brought out from the video pipeline, is not in sync with the VGA output signals, i.e. the VGA signals run four clock cycles after the Col_Sel signal.

VDD_CORE *2.5 V Power Supply.* These power pins are necessary to supply the core with 2.5 V.

TCLK *Test clock*

TDI *Test data input*

TMS *Test mode input*

TDO *Test data output*

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Table 2-4. ISA / IDE Dynamic Multiplexing

ISA BUS (ISAOE# = 0)	IDE (ISAOE# = 1)
RMRTCCS#	DD[15]
KBCS#	DD[14]
RTCRW#	DD[13]
RTCDS#	DD[12]
SA[19:8]	DD[11:0]
LA[23]	SCS3#
LA[22]	SCS1#
SA[21]	PCS3#
SA[20]	PCS1#
LA[19:17]	DA[2:0]
IOCHRDY	DIORDY

Table 2-5. ISA / Local Bus Pin Sharing

ISA / IPC	LOCAL BUS
SD[15:0]	PD[15:0]
DREQ_MUX[1:0]	PA[21:20]
SMEMR#	PA[19]
MEMW#	PA[18]
BHE#	PA[17]
AEN	PA[16]
ALE	PA[15]
MEMR#	PA[14]
IOR#	PA[13]
IOW#	PA[12]
REF#	PA[11]
IOCHCK#	PA[10]
GPIOCS#	PA[9]
ZWS#	PA[8]
SA[7:4]	PA[7:4]
TC, DACK_ENC[2:0]	PA[3:0]
SA[3]	PRDY
ISAOE#,SA[2:0]	IOCS#[3:0]
DEV_CLK, RTCAS	FCS#[1:0]
IOCS16#, MASTER#	PRD#[1:0]
SMEMW#, MCS16#	PWR#[1:0]

Table 2-6. Signal value on Reset

Signal Name	SYSRSTI# active	SYSRSTI# inactive SYSRSTO# active	release of SYSRSTO#
BASIC CLOCKS AND RESETS			
XTALO	14MHz		
ISA_CLK	Low	7MHz	
ISA_CLK2X	14MHz		
OSC14M	14MHz		
DEV_CLK	24MHz		
HCLK	Oscillating at the speed defined by the strap options.		
PCI_CLKO	HCLK divided by 2 or 3, depending on the strap options.		
DCLK	17MHz		
MEMORY CONTROLLER			
MCLKO	66MHz if asynchonous mode, HCLK speed if synchronized mode.		
CS#[3:1]	High		
CS#[0]	High		SDRAM init sequence: Write Cycles
MA[10:0], BA[0]	0x00		
RAS#[1:0], CAS#[1:0]	High		
MWE#, DQM[7:0]	High		
MD[63:0]	Input		
PCI INTERFACE			
AD[31:0]	0x0000		First prefetch cycles when not in Local Bus mode.
CBE[3:0], PAR	Low		
FRAME#, TRDY#, IRDY#	Input		
STOP#, DEVSEL#	Input		
PERR#, SERR#	Input		

Table 2-6. Signal value on Reset

Signal Name	SYSRSTI# active	SYSRSTI# inactive SYSRSTO# active	release of SYSRSTO#
PCI_GNT#[2:0]	High		
ISA BUS INTERFACE			
ISAOE#	High		Low
RMRTCCS#	Hi-Z		
LA[23:17]	Unknown	0x00	First prefetch cycles
SA[19:0]	0xFFFXX	0xFFF03	when in ISA or PCMCIA mode.
SD[15:0]	Unknown	0xFF	Address start is 0xFFFFF0
BHE#, MEMR#	Unknown	High	
MEMW#, SMEMR#, SMEMW#, IOR#, IOW#	Unknown	High	
REF#	Unknown	High	
ALE, AEN	Low		
DACK_ENC[2:0]	Input		0x04
TC	Input		Low
GPIOCS#	Hi-Z		High
RTCDS#, RTCRW#, KBCS#	Hi-Z		
RTCAS	Unknown	Low	
LOCAL BUS INTERFACE			
PA[24:0]	Unknown		
PD[15:0]	Unknown	0xFF	First prefetch cycles
PRD#	Unknown	High	
PBE#[1:0], FCS0#, FCS_0H#	High		
FCS_0L#, FCS1#, FCS_1H#, FCS_1L#	High		
PWR#, IOCS#[7:0]	High		
IDE CONTROLLER			
DD[15:0]	0xFF		
DA[2:0]	Unknown	Low	
PCS1, PCS3, SCS1, SCS3	Unknown	Low	
PDACK#, SDACK#	High		
PDIOR#, PDIOW#, SDIOR#, SDIOW#	High		
VGA CONTROLLER			
RED, GREEN, BLUE	Black		
VSYNC, HSYNC	Low		
COL_SEL	Unknown		
TV OUTPUT			
RED_TV, GREEN_TV, BLUE_TV	Black		
CVBS	Black		
VCS	Low		
ODD_EVEN	Low		
I2C INTERFACE			
SCL / DDC[1]	Input		
SDA / DDC[0]	Input		
JTAG			
TDO	High		
MISCELLANEOUS			
SPKRD	Low		

PIN DESCRIPTION

Table 2-7. Pinout.

Pin #	Pin name
AF3	SYSRSETI#
AE4	SYSRSETO#
A3	XTALI
C4	XTALO
G23	HCLK
H24	DEV_CLK
AD11	DCLK
AF15	MCLKI
AB23	MCLKO
AE16	MA[0]
AD15	MA[1]
AF16	MA[2]
AE17	MA[3]
AD16	MA[4]
AF17	MA[5]
AE18	MA[6]
AD17	MA[7]
AF18	MA[8][3]
AE19	MA[9][3]
AE20	MA[10]
AC19	MA[11]/BA[0]
AF22	CS#[0]
AD21	CS#[1]
AE24	CS#[2]/MA[11]
AD23	CS#[3]/MA[12]/BA[1]
AF23	RAS#[0]
AD22	RAS#[1]
AE21	CAS#[0]
AC20	CAS#[1]
AF20	DQM#[0]
AD19	DQM#[1]
AF21	DQM#[2]
AD20	DQM#[3]
AE22	DQM#[4]
AE23	DQM#[5]
AF19	DQM#[6]
AD18	DQM#[7]
AC22	MWE#
R1	MD[0][3]
T2	MD[1][3]
R3	MD[2]
T1	MD[3]
R4	MD[4]
U2	MD[5]
T3	MD[6]
U1	MD[7]
U4	MD[8]
V2	MD[9]

Pin #	Pin name
U3	MD[10]
V1	MD[11]
W2	MD[12]
V3	MD[13]
Y2	MD[14]
W4	MD[15]
Y1	MD[16]
W3	MD[17]
AA2	MD[18]
Y4	MD[19]
AA1	MD[20]
Y3	MD[21]
AB2	MD[22]
AB1	MD[23]
AA3	MD[24]
AB4	MD[25]
AC1	MD[26]
AB3	MD[27]
AD2	MD[28]
AC3	MD[29]
AD1	MD[30]
AF2	MD[31]
AF24	MD[32]
AE26	MD[33]
AD25	MD[34]
AD26	MD[35]
AC25	MD[36]
AC24	MD[37]
AC26	MD[38]
AB25	MD[39]
AB24	MD[40]
AB26	MD[41]
AA25	MD[42]
Y23	MD[43]
AA24	MD[44]
AA26	MD[45]
Y25	MD[46]
Y26	MD[47]
Y24	MD[48]
W25	MD[49][3]
V23	MD[50][3]
W26	MD[51][3]
W24	MD[52][3]
V25	MD[53][3]
V26	MD[54][3]
U25	MD[55][3]
V24	MD[56][3]
U26	MD[57][3]
U23	MD[58][3]

Pin #	Pin name
T25	MD[59][3]
U24	MD[60][3]
T26	MD[61][3]
R25	MD[62][3]
R26	MD[63][3]
F24	PCI_CLKI
D25	PCI_CLKO
B20	AD[0]
C20	AD[1]
B19	AD[2]
A19	AD[3]
C19	AD[4]
B18	AD[5]
A18	AD[6]
B17	AD[7]
C18	AD[8]
A17	AD[9]
D17	AD[10]
B16	AD[11]
C17	AD[12]
B15	AD[13]
A15	AD[14]
C16	AD[15]
B14	AD[16]
D15	AD[17]
A14	AD[18]
B13	AD[19]
D13	AD[20]
A13	AD[21]
C14	AD[22]
B12	AD[23]
C13	AD[24]
A12	AD[25]
C12	AD[26]
A11	AD[27]
D12	AD[28]
B10	AD[29]
C11	AD[30]
A10	AD[31]
D10	CBE[0]
C10	CBE[1]
A9	CBE[2]
B8	CBE[3]
A8	FRAME#
B7	TRDY#
D8	IRDY#
A7	STOP#
C8	DEVSEL#
B6	PAR

Pin #	Pin name
D7	SERR#
A6	LOCK#
D20	PCI_REQ#[0]
C21	PCI_REQ#[1]
A21	PCI_REQ#[2]
C22	PCI_GNT#[0]
A22	PCI_GNT#[1]
B21	PCI_GNT#[2]
A5	PCI_INT#[0]
C6	PCI_INT#[1]
B4	PCI_INT#[2]
D5	PCI_INT#[3]
F2	LA[17]/DA[0[
G4	LA[18]/DA[1]
F3	LA[19]/DA[2]
F1	LA[20]/PCS1#
G2	LA[21]/PCS3#
G1	LA[22]/SCS1#
H2	LA[23]/SCS3#
J4	SA[0]
H1	SA[1]
H3	SA[2]
J2	SA[3]
J1	SA[4]
K2	SA[5]
J3	SA[6]
K1	SA[7]
K4	SA[8]
L2	SA[9]
K3	SA[10]
L1	SA[11]
M2	SA[12]
M1	SA[13]
L3	SA[14]
N2	SA[15]
M4	SA[16]
M3	SA[17]
P2	SA[18]
P4	SA[19]
K25	SD[0]
L24	SD[1]
K26	SD[2]
K23	SD[3]
J25	SD[4]
K24	SD[5]
J26	SD[6]
H25	SD[7]
H26	SD[8]

Pin #	Pin name
J24	SD[9]
G25	SD[10]
H23	SD[11]
D24	SD[12]
C26	SD[13]
A25	SD[14]
B24	SD[15]
AD4	ISA_CLK
AF4	ISA_CLK2X
C9	OSC14M
P25	ALE
AE8	ZWS#
R23	BHE#
P26	MEMR#
R24	MEMW#
N25	SMEMR#
N23	SMEMW#
N26	IOR#
P24	IOW#
N24	MCS16#
M26	IOCS16#
M25	MASTER#
L25	REF#
M24	AEN
L26	IOCHCK#
T24	IOCHRDY
M23	ISAOE#
A4	RTCAS
P3	RTCDS#
R2	RTCRW#
P1	RMRTCCS#
AE3	GPIOCS#
G26	PA[22][3]
A20	PA[23][3]
B1	PIRQ
C2	SIRQ
C1	PDRQ
D2	SDRQ
D3	PDACK#
D1	SDACK#
E2	PDIOR#
E4	PDIOW#
E3	SDIOR#
E1	SDIOW#
E23	IRQ_MUX[0]
D26	IRQ_MUX[1]

Pin #	Pin name
E24	IRQ_MUX[2]
C25	IRQ_MUX[3]
A24	DREQ_MUX[0]
B23	DREQ_MUX[1]
C23	DACK_ENC[0]
A23	DACK_ENC[1]
B22	DACK_ENC[2]
D22	TC
N3	KBCS#
AF9	RED
AE9	GREEN
AD8	BLUE
AC5	VSYNC
AE5	HSYNC
AC10	VREF_DAC
AE10	RSET
AD7	COMP
AE15	VCLK
AD5	VIN[0]
AF7	VIN[1]
AF5	VIN[2]
AE6	VIN[3]
AC7	VIN[4]
AD6	VIN[5]
AF6	VIN[6]
AE7	VIN[7]
AD10	RED_TV
AF11	GREEN_TV
AE12	BLUE_TV
AE13	VCS
AC12	ODD_EVEN
AF14	CVBS
AE11	IREF1_TV
AF12	VREF1_TV
AE14	IREF2_TV
AC14	VREF2_TV
C5	SPKRD
B5	SCL
C7	SDA
B3	SCAN_ENABLE
C15	COL_SEL
G3	TCLK
N1	TMS
W1	TDI