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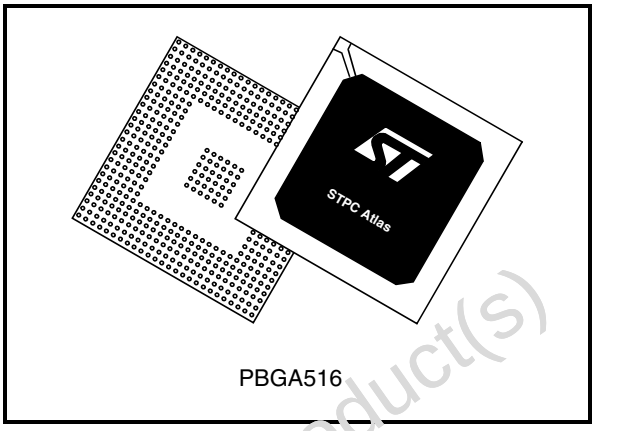
STPC® ATLAS

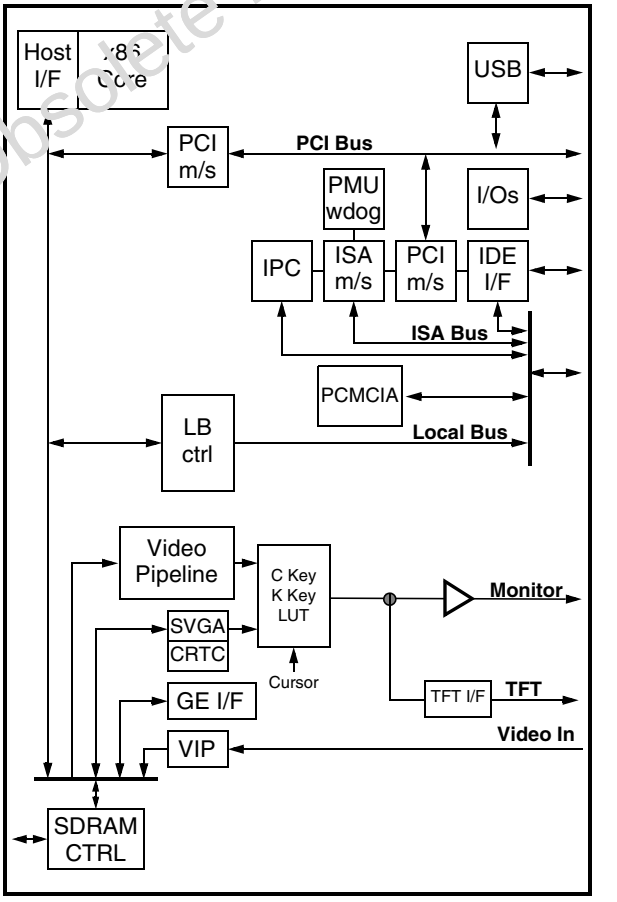
X86 CORE PC COMPATIBLE SYSTEM-ON-CHIP FOR TERMINALS

- POWERFUL x86 PROCESSOR
- 64-BIT SDRAM UMA CONTROLLER
- GRAPHICS CONTROLLER
  - VGA & SVGA CRT CONTROLLER
  - 135MHz RAMDAC
  - ENHANCED 2D GRAPHICS ENGINE
- VIDEO INPUT PORT
- VIDEO PIPELINE
  - UP-SCALER
  - VIDEO COLOUR SPACE CONVERTER
  - CHROMA & COLOUR KEY SUPPORT
- TFT DISPLAY CONTROLLER
- PCI 2.1 MASTER / SLAVE / ARBITER
- ISA MASTER / SLAVE CONTROLLER
- 16-BIT LOCAL BUS INTERFACE
- PCMCIA INTERFACE CONTROLLER
- EIDE CONTROLLER
- 2 USB HOST HUB INTERFACES
- I/O FEATURES
  - PC/AT+ KEYBOARD CONTROLLER
  - PS/2 MOUSE CONTROLLER
  - 2 SERIAL PORTS
  - 1 PARALLEL PORT
  - 16 GENERAL PURPOSE I/Os
  - I²C INTERFACE
- INTEGRATED PERIPHERAL CONTROLLER
  - DMA CONTROLLER
  - INTERRUPT CONTROLLER
  - TIMER / COUNTERS
- POWER MANAGEMENT UNIT
- WATCHDOG
- JTAG IEEE1149.1



PBGA516

Logic Diagram



Rev. 3

DESCRIPTION

The STPC Atlas integrates a standard 5th generation x86 core along with a powerful UMA graphics/video chipset, support logic including PCI, ISA, Local Bus, USB, EIDE controllers and combines them with standard I/O interfaces to provide a single PC compatible subsystem on a single device, suitable for all kinds of terminal and industrial appliances.

- **X86 Processor core**
- Fully static 32-bit 5-stage pipeline, x86 processor fully PC compatible.
- Can access up to 4GB of external memory.
- 8Kbyte unified instruction and data cache with write back and write through capability.
- Parallel processing integral floating point unit, with automatic power down.
- Runs up to 133 MHz (X2).
- Fully static design for dynamic clock control.
- Low power and system management modes.
- Optimized design for 2.5V operation.

- **SDRAM Controller**
- 64-bit data bus.
- Up to 90MHz SDRAM clock speed.
- Integrated system memory, graphic frame memory and video frame memory.
- Supports 8MB up to 128 MB system memory.
- Supports 16-Mbit, 64-Mbit and 128-Mbit SDRAMs.
- Supports 8, 16, 32, 64, and 128 MB DIMMs.
- Supports buffered, non buffered, and registered DIMMs
- 4-line write buffers for CPU to DRAM and PCI to DRAM cycles.
- 4-line read prefetch buffers for PCI masters.
- Programmable latency
- Programmable timing for SDRAM parameters.
- Supports -8, -10, -12, -13, -15 memory parts
- Supports memory hole between 1MB and 8MB for PCI/ISA busses.
- 32-bit access, Autoprecharge & Power-down are not supported.

- **Enhanced 2D Graphics Controller**
- Supports pixel depths of 8, 16, 24 and 32 bit.
- Full BitBLT implementation for all 256 raster operations defined for Windows.
- Supports 4 transparent BLT modes - Bitmap Transparency, Pattern Transparency, Source Transparency and Destination Transparency.
- Hardware clipping
- Fast line draw engine with anti-aliasing.
- Supports 4-bit alpha blended font for anti-aliased text display.
- Complete double buffered registers for pipelined operation.
- 64-bit wide pipelined architecture running at 90 MHz. Hardware clipping

- **CRT Controller**
- Integrated 135MHz triple RAMDAC allowing for 1280 x 1024 x 75Hz display.
- 8-, 16-, 24-bit pixels.
- Interlaced or non-interlaced output.

- **Video Input port**
- Accepts video inputs in CCIR 601/656 mode.
- Optional 2:1 decimator
- Stores captured video in off setting area of the onboard frame buffer.
- HSYNC and B/T generation or lock onto external video timing source.

- **Video Pipeline**
- Two-tap interpolative horizontal filter.
- Two-tap interpolative vertical filter.
- Color space conversion (RGB to YUV and YUV to RGB).
- Programmable window size.
- Chroma and color keying for integrated video overlay.

- **TFT Interface**
- Programmable panel size up to 1024 by 1024 pixels.
- Support for VGA and SVGA active matrix TFT flat panels with 9, 12, 18-bit interface (1 pixel per clock).
- Support for XGA and SXGA active matrix TFT flat panels with 2 x 9-bit interface (2 pixels per clock).
- Programmable image positionning.
- Programmable blank space insertion in text mode.
- Programmable horizontal and vertical image expansion in graphic mode.
- One fully programmable PWM (Pulse Width Modulator) signals to adjust the flat panel brightness and contrast.
- Supports **PanelLink**™ high speed serial transmitter externally for high resolution panel interface.

- **PCI Controller**
- Compatible with PCI 2.1 specification.
- Integrated PCI arbitration interface. Up to 3 masters can connect directly. External logic allows for greater than 3 masters.
- Translation of PCI cycles to ISA bus.
- Translation of ISA master initiated cycle to PCI.
- Support for burst read/write from PCI master.
- PCI clock is 1/2, 1/3 or 1/4 Host bus clock.

- **ISA master/slave**
- Generates the ISA clock from either 14.318MHz oscillator clock or PCI clock
- Supports programmable extra wait state for ISA cycles
- Supports I/O recovery time for back to back I/O cycles.
- Fast Gate A20 and Fast reset.
- Supports the single ROM that C, D, or E. blocks shares with F block BIOS ROM.
- Supports flash ROM.
- Supports ISA hidden refresh.
- Buffered DMA & ISA master cycles to reduce bandwidth utilization of the PCI and Host bus.

- **Local Bus interface**
- Multiplexed with ISA/DMA interface.
- Low latency asynchronous bus
- 16-bit data bus with word steering capability.
- Programmable timing (Host clock granularity)
- 4 Programmable Flash Chip Select.
- 8 Programmable I/O Chip Select.
- I/O device timing (setup & recovery time) programmable
- Supports 32-bit Flash burst.
- 2-level hardware key protection for Flash boot block protection.
- Supports 2 banks of 32MB flash devices with boot block shadowed to 0x000F0000.
- Reallocatable Memory space Windows

- **EIDE Interface**
- Supports PIO
- Transfer Rates to 22 MBytes/sec
- Supports up to 4 IDE devices
- Concurrent channel operation (PIO modes) - 4 x 32-Bit Buffer FIFOs per channel
- Support for PIO mode 3 & 4.
- Individual drive timing for all four IDE devices
- Supports both legacy & native IDE modes
- Supports hard drives larger than 528MB
- Support for CD-ROM and tape peripherals
- Backward compatibility with IDE (ATA-1).

- **Integrated Peripheral Controller**
- 2X8237/AT compatible 7-channel DMA controller.
- 2X8259/AT compatible interrupt Controller. 16 interrupt inputs - ISA and PCI.
- Three 8254 compatible Timer/Counters.
- Co-processor error support logic.
- Supports external RTC (Not in Local Bus Mode).

- **PCMCIA interface**
- Support one PCMCIA 68-pin standard PC Card Socket.
- Power Management support.
- Support PCMCIA/ATA specifications.
- Support I/O PC Card with pulse-mode interrupts.

- **USB Interface**
- USB 1.1 compatible.
- Open HCI 1.0 compliant.
- User configurable RootHub.
- Support for both LowSpeed and HighSpeed USB devices.
- No bi-directionnal or Tri-state busses.
- No level sensitive latches.
- System Management Interrupt pin support
- Hooks for legacy device support.

- **Keyboard interface**
- Fully PC/AT+ compatible

- **Mouse interface**
- Fully PS/2 compatible

- **Serial interface**
- 16550 compatible
- Programmable word length, stop bits, parity.
- 16-bit programmable baud rate generator.
- Interrupt generator.
- Loop-back mode.
- 8-bit scratch register.
- Two 16-bit FIFOs.
- Two DMA handshake lines.

Parallel port

- All IEEE Standard 1284 protocols supported: Compatibility, Nibble, Byte, EPP, and ECP modes.
- 16 bytes FIFO for ECP.

- **Power Management**
- Four power saving modes: On, Doze, Standby, Suspend.
- Programmable system activity detector
- Supports Intel & Cyrix SMM and APM.
- Supports STOPCLK.
- Supports IO trap & restart.
- Independent peripheral time-out timer to monitor hard disk, serial & parallel port.
- 128K SM_RAM address space from 0xA0000 to 0xB0000

- **JTAG**
- Boundary Scan compatible IEEE1149.1.
- Scan Chain control.
- Bypass register compatible IEEE1149.1.
- ID register compatible IEEE1149.1.
- RAM BIST control.

ExCA is a trademark of PCMCIA / JEIDA.

PanelLink is a trademark of SiliconImage, Inc

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1 GENERAL DESCRIPTION

At the heart of the STPC Atlas is an advanced processor block that includes a powerful x86 processor core along with a 64-bit SDRAM controller, advanced 64-bit accelerated graphics and video controller, a high speed PCI bus controller and industry standard PC chip set functions (Interrupt controller, DMA Controller, Interval timer and ISA bus).

The STPC Atlas has in addition, a TFT output, a Video Input, an EIDE controller, a Local Bus interface, PCMCIA and super I/O features including USB host hub.

1.1. ARCHITECTURE

The STPC Atlas makes use of a tightly coupled Unified Memory Architecture (UMA), where the same memory array is used for CPU main memory and graphics frame-buffer. This means a reduction in total system memory for system performances that are equal to that of a comparable frame buffer and system memory based system, and generally much better, due to the higher memory bandwidth allowed by attaching the graphics engine directly to the 64-bit processor host interface running at the speed of the processor bus rather than the traditional PCI bus.

The 64-bit wide memory array provides the system with an 800MB/s peak bandwidth. This allows for higher resolution screens and greater color depth. The processor bus runs at 133 MHz, further increasing “standard” bandwidth by at least a factor of two.

The ‘standard’ PC chipset functions (DMA, interrupt controller, timers, power management logic) are integrated together with the x86 processor core; additional low bandwidth functions such as communication ports are accessed by the STPC Atlas via an internal ISA bus.

The PCI bus is the main data communication link to the STPC Atlas chip. The STPC Atlas translates appropriate host bus I/O and Memory cycles onto the PCI bus. It also supports the generation of Configuration cycles on the PCI bus. The STPC Atlas, as a PCI bus agent (host bridge class), is compatible with PCI specification 2.1. The chip-set also implements the PCI mandatory header registers in Type 0 PCI configuration space for easy porting of PCI aware system BIOS. The device contains a PCI arbitration function for three external PCI devices.

Figure 1-1 describes this architecture.

1.2. GRAPHICS FEATURES

Graphics functions are controlled through the on-chip SVGA controller and the monitor display is produced through the 2D graphics display engine.

This Graphics Engine is tuned to work with the host CPU to provide a balanced graphics system with a low silicon area cost. It performs limited graphics drawing operations which include hardware acceleration of text, bitblts, transparent blts and fills. The results of these operations change the contents of the on-screen or off-screen frame buffer areas of SDRAM memory. The frame buffer can occupy a space up to 4 Mbytes anywhere in the physical main memory.

The maximum graphics resolution supported is 1280 x 1024 in 16 Million colours at 75 Hz refresh rate and is VGA and SVGA compatible. Horizontal timing fields are VGA compatible while the vertical fields are extended by one bit to accommodate above display resolution.

To generate the TFT output, the STPC Atlas extracts the digital video stream before the RAMDAC and reformats it to the TFT format. The height and width of the flat panel are programmable.

1.3. INTERFACES

An industry standard EIDE (ATA 2) controller is built in to the STPC Atlas and connected internally via the PCI bus.

The STPC Atlas integrates two USB ports. Universal Serial Bus (USB) is a general purpose communications interface for connecting peripherals to a PC. The USB Open Host Controller Interface (Open HCI) Specification, revision 1.1, supports speeds of up to 12 MB/s. USB is royalty free and is likely to replace low-speed legacy serial, parallel, keyboard, mouse and floppy drive interfaces. USB Revision 1.1 is fully supported under Microsoft Windows 98 and Windows 2000.

The STPC Atlas PCMCIA controller has been specifically designed to provide the interface with PCMCIA cards which contain additional memory or I/O

The power management control facilities include socket power control, insertion/removal capability, power saving with Windows inactivity, NCS controlled Chip Power Down, together with further

controls for 3.3V suspend with Modem Ring Resume Detection.

The STPC Atlas implements a multi-function parallel port. The standard PC/AT compatible logical address assignments for LPT1, LPT2 and LPT3 are supported. It can be configured for any of the following three modes and supports the IEEE Standard 1284 parallel interface protocol standards, as follows:
- Compatibility Mode (Forward channel, standard)
- Nibble Mode (Reverse channel, PC compatible)
- Byte Mode (Reverse channel, PS/2 compatible)

The General Purpose Input/Output (GPIO) interface provides a 16-bit I/O facility, using 16 dedicated device pins. It is organised using two blocks of 8-bit Registers, one for lines 0 to 7, the other for lines 8 to 15.
Each GPIO port can be configured as an input or an output simply by programming the associated port direction control register. All GPIO ports are configured as inputs at reset, which also latches the input levels into the Strap Registers. The input states of the ports are thus recorded automatically at reset, and this can be used as a strap register anywhere in the system.

1.4. FEATURE MULTIPLEXING

The STPC Atlas BGA package has 516 balls. This however is not sufficient for all of the integrated functions available; some features therefore share the same balls and cannot thus be used at the same time. The STPC Atlas configuration is done by ‘strap options’. This is a set of pull-up or pull-down resistors on the memory data bus, checked on reset, which auto-configure the STPC Atlas.

There 3 multiplexed functions are the external ISA bus, the Local Bus and the PCMCIA interface.

1.5. POWER MANAGEMENT

The STPC Atlas core is compliant with the Advanced Power Management (APM) specification to provide a standard method by which the BIOS can control the power used by personal computers. The Power Management Unit (PMU) module controls the power consumption, providing a comprehensive set of features that controls the power usage and supports compliance with the United States Environmental Protection Agency's Energy Star Computer Program. The PMU provides the following hardware structures to assist the software in managing the system power consumption:

- System Activity Detection.

- 3 power-down timers detecting system inactivity:
  - Doze timer (short durations).
  - Stand-by timer (medium durations).
  - Suspend timer (long durations).

- House-keeping activity detection.

- House-keeping timer to cope with short bursts of house-keeping activity while dozing or in stand-by state.

- Peripheral activity detection.

- Peripheral timer detecting peripheral inactivity

- SUSP# modulation to adjust the system performance in various power down states of the system including full power-on state.

- Power control outputs to disable power from different planes of the board.

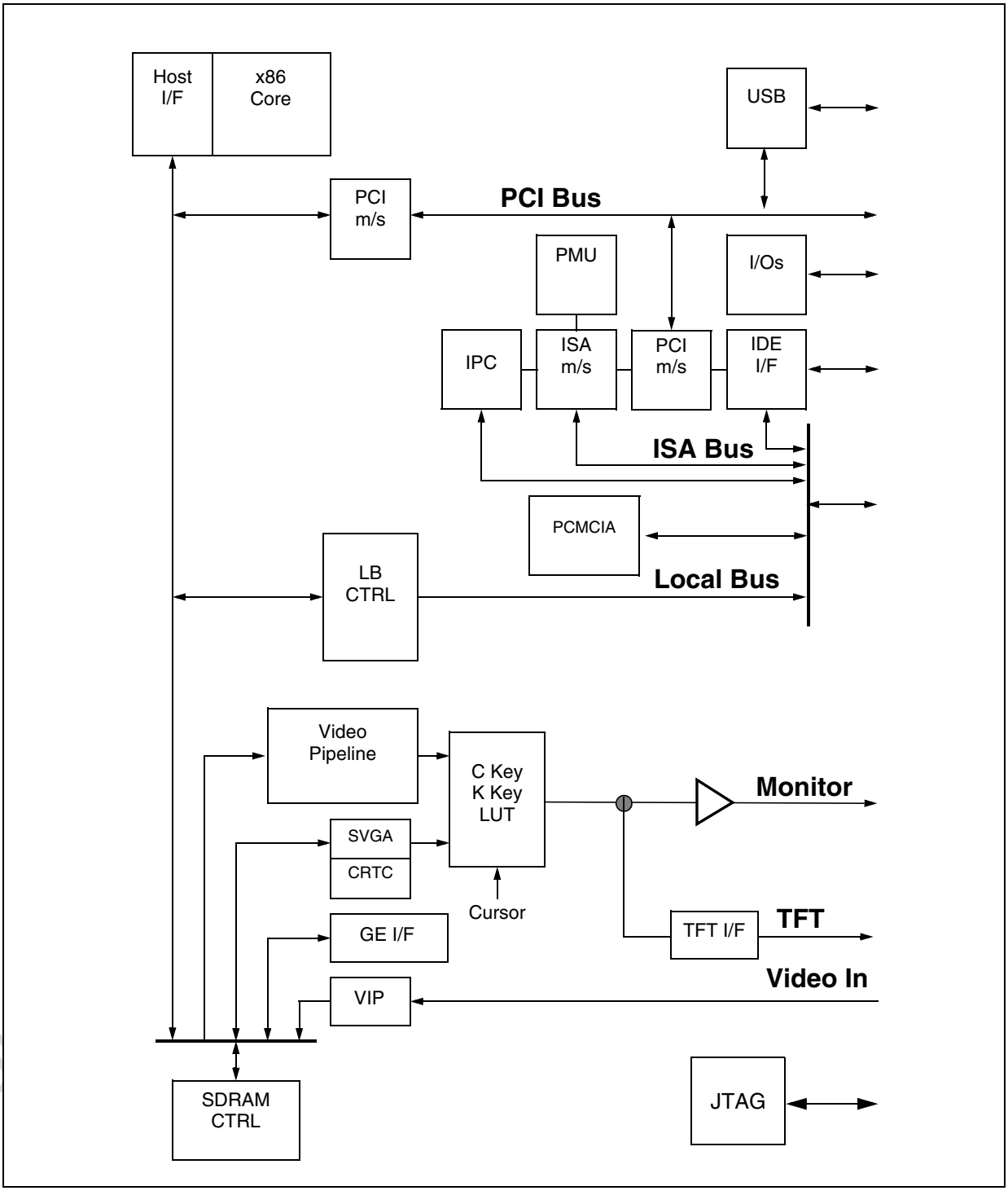
Lack of system activity for progressively longer periods of time is detected by the three power down timers. These timers can generate SMI interrupts to CPU so that the SMM software can put the system in decreasing states of power consumption. Alternatively, system activity in a power down state can generate an SMI interrupt to allow the software to bring the system back up to full power-on state. The chip-set supports up to three power down states described above; these correspond to decreasing levels of power savings.

Power down puts the STPC Atlas into suspend mode. The processor completes execution of the current instruction, any pending decoded instructions and associated bus cycles. During the suspend mode, internal clocks are stopped. Removing power-down, the processor resumes instruction fetching and begins execution in the instruction stream at the point it had stopped. Because of the static nature of the core, no internal data is lost.

1.6. JTAG

JTAG stands for Joint Test Action Group and is the popular name for IEEE Std. 1149.1, Standard Test Access Port and Boundary-Scan Architec-ture. This built-in circuitry is used to assist in the test, maintenance and support of functional circuit blocks. The circuitry includes a standard interface through which instructions and test data are communicated. A set of test features is defined, including a boundary-scan register so that a component is able to respond to a minimum set of test instructions.

Figure 1-1. Functional description.



1.7. CLOCK TREE

The STPC Atlas integrates many features and generates all its clocks from a single 14MHz oscillator. This results in multiple clock domains as described in Figure 1-2.

The speed of the PLLs is either fixed (DEVCLK), either programmable by strap option (HCLK) either programmable by software (DCLK, MCLK). When in synchronized mode, MCLK speed is fixed to HCLKO speed and HCLKI is generated from MCLKI.

Figure 1-2. STPC Atlas clock architecture

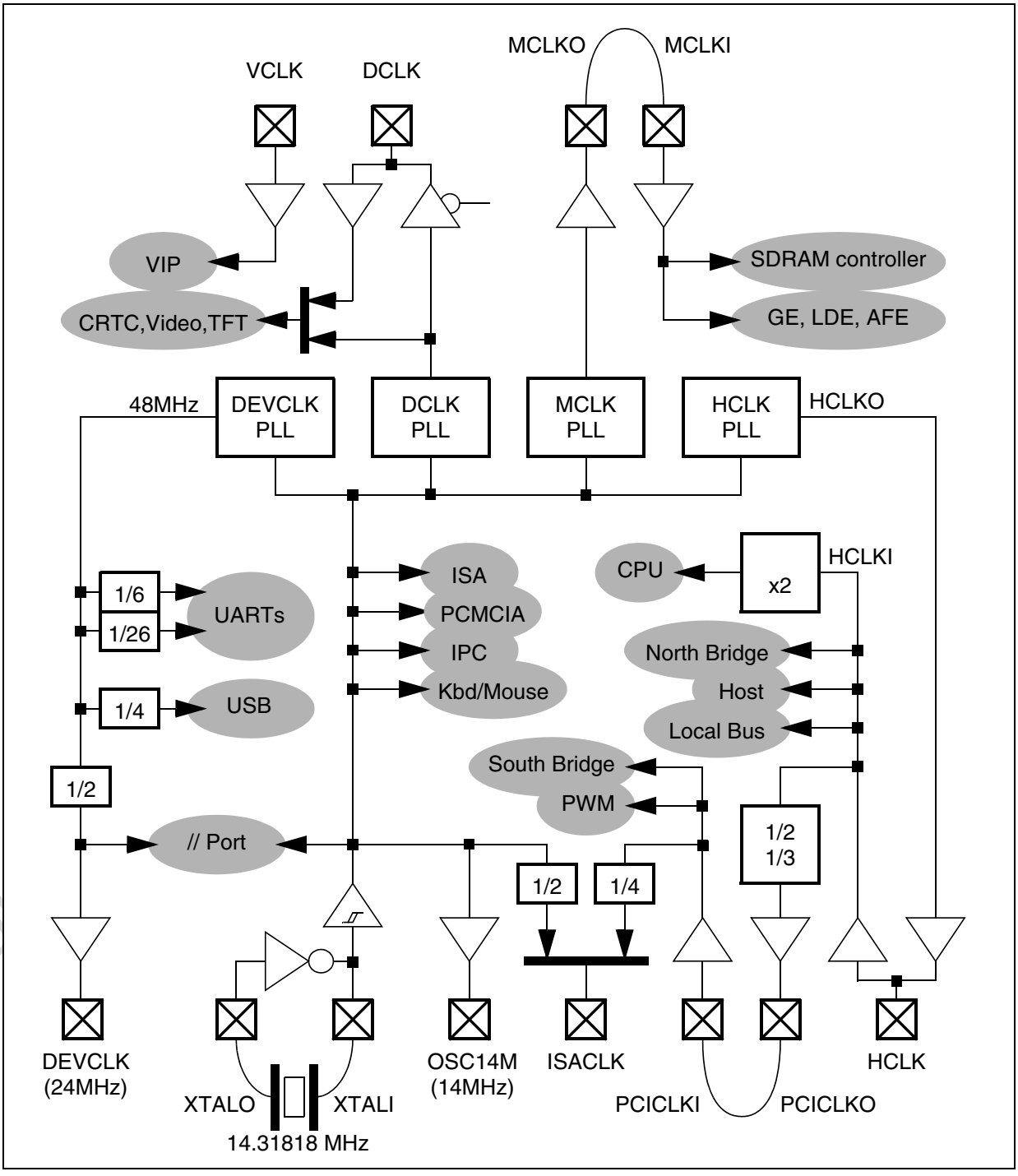


Figure 1-3. Typical ISA-based Application.

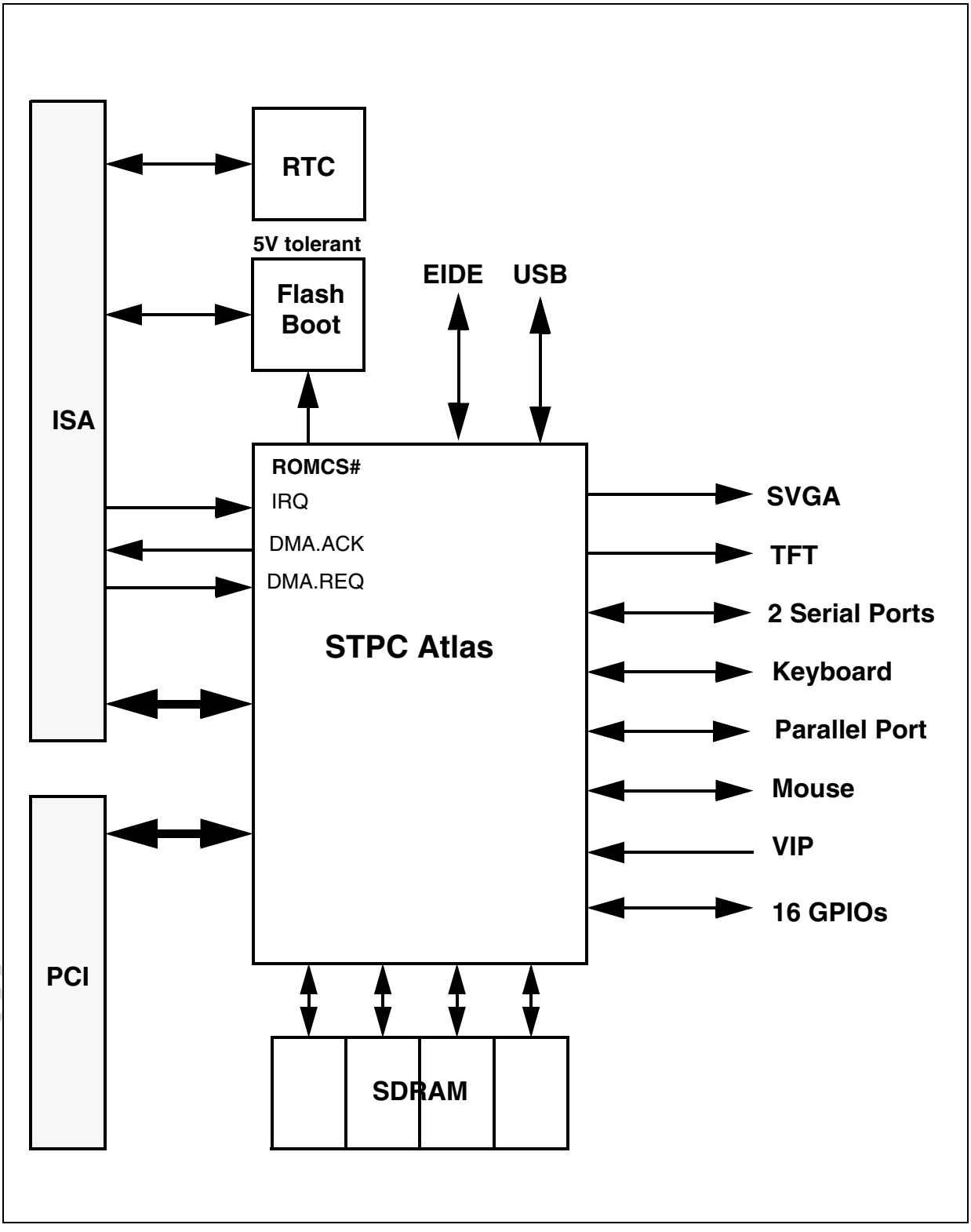


Figure 1-4. Typical PCMCIA-based Application.

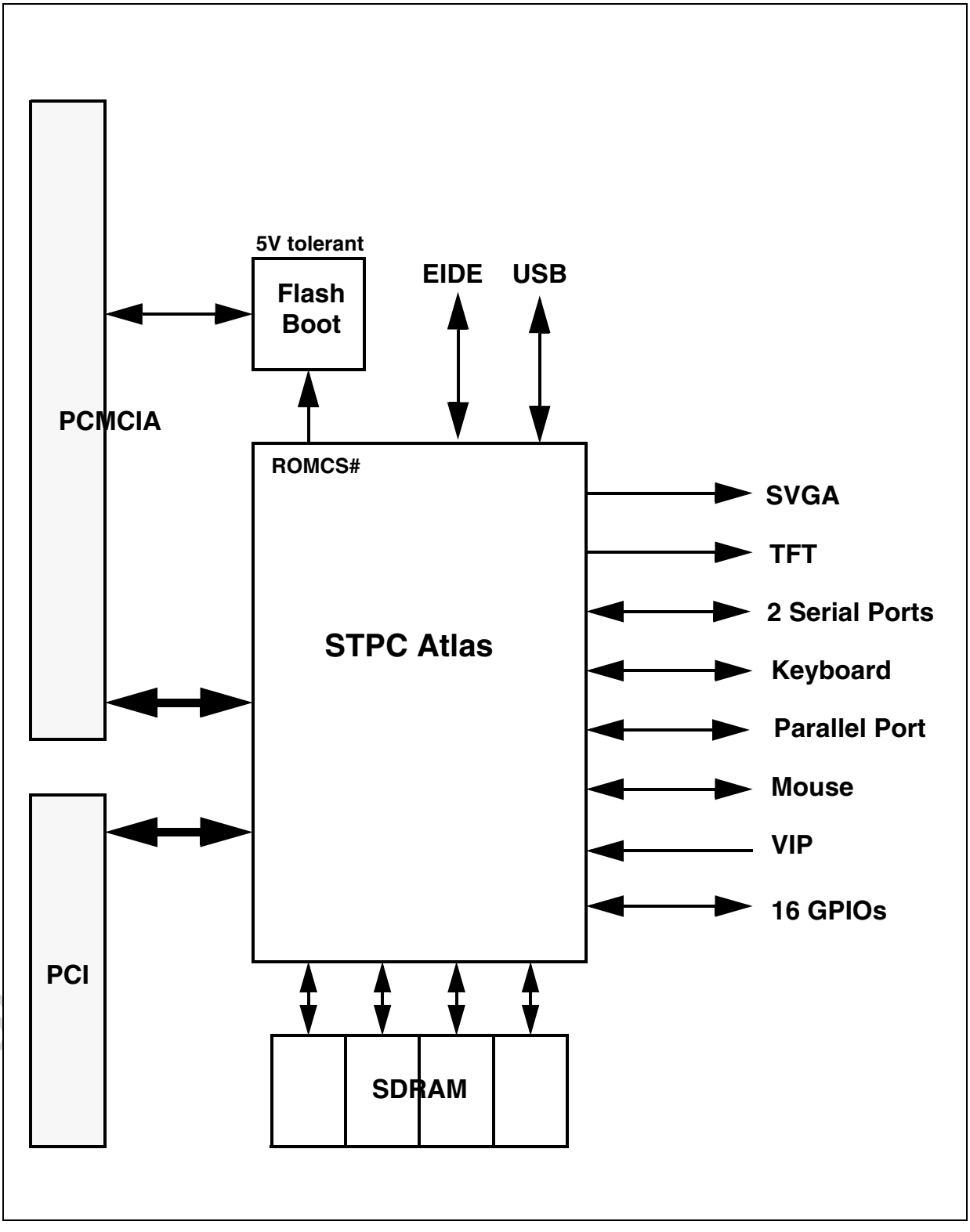
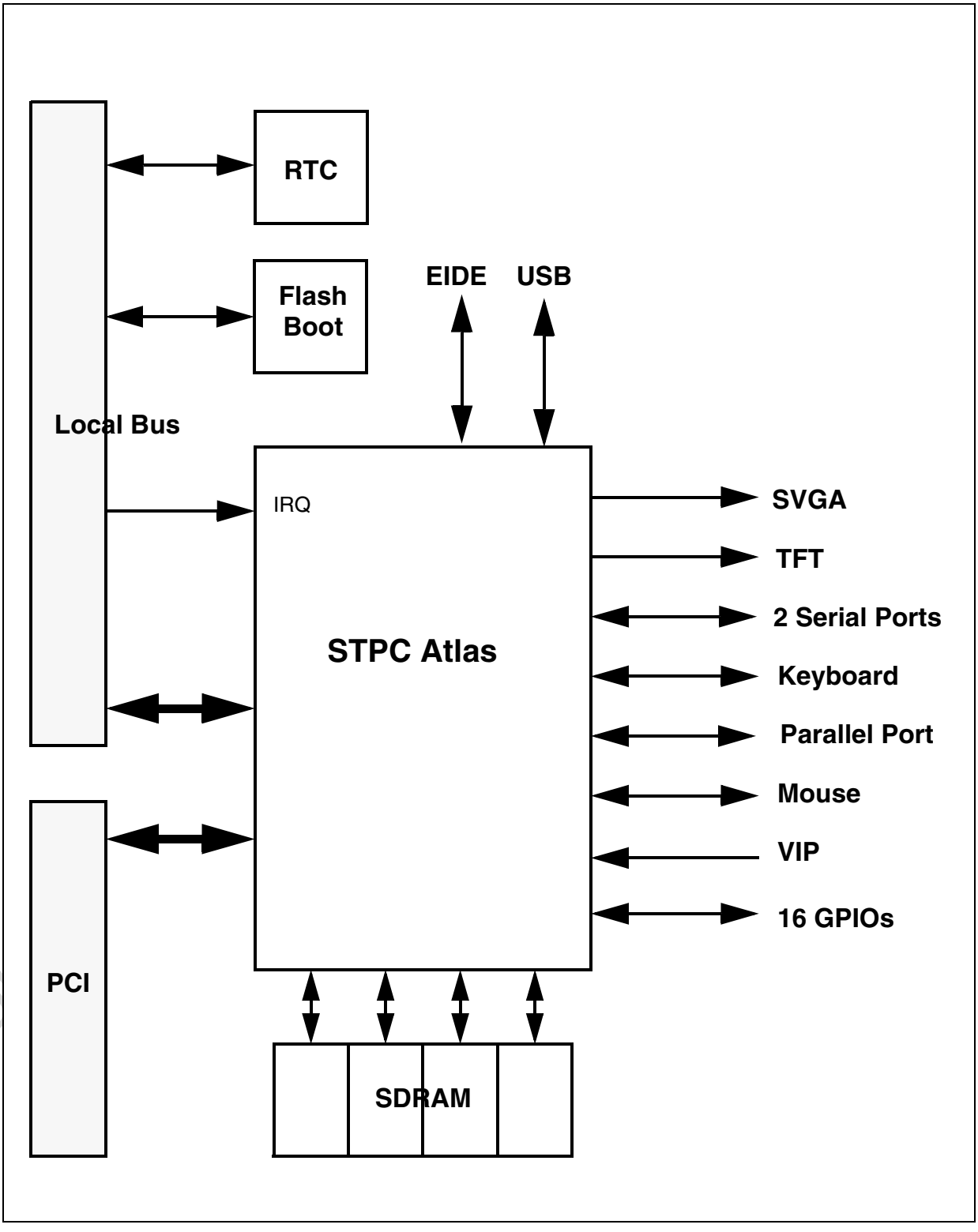


Figure 1-5. Typical Local-Bus-based Application.



2 PIN DESCRIPTION

2.1. INTRODUCTION

The STPC Atlas integrates most of the functionalities of the PC architecture. Therefore, many of the traditional interconnections between the host PC microprocessor and the peripheral devices are totally internal to the STPC Atlas. This offers improved performance due to the tight coupling of the processor core and it's peripherals. As a result many of the external pin connections are made directly to the on-chip peripheral functions.

Table 2-1 describes the physical implementation listing signal types and their functionalities. Table 2-2 provides a full pin listing and description.

Table 2-6 provides a full listing of the STPC Atlas package pin location physical connection. Please refer to the pin allocation drawing for reference.

Due to the number of pins available for the package, and the number of functional I/Os, some pins have several functions, selectable by strap option on Reset. Table 2-4 provides a summary of these pins and their functions.

Non multi-functional pins associated with a particular function are not available for use elsewhere when that function is disabled. For example, when in the ISA mode, the Local Bus is disabled totally and Local Bus pins are set to the tri-state (high-impedance) condition.

Table 2-1. Signal Description

Group name	Qty	
Basic Clocks, Reset & Xtal (SYS)		19
SDRAM Controller (SDRAM)		95
PCI Controller		51
ISA Controller	80	100
Local Bus I/F	67	
PCMCIA Controller	62	
IDE Controller	34	
VGA Controller (VGA) / I^2C		10
Video Input Port		11
TFT output		24
USB Controller		6
Serial Interface		16
Keyboard/Mouse Controller		4
Parallel Port		18
GPIO Signals		16
JTAG Signals		5
Miscellaneous		5
Grounds		96
V_{DD} 3.3 V/2.5 V		36
Reserved		4
Total Pin Count		516

Table 2-2. Definition of Signal Pins

Signal Name	Dir	Buffer Type[1]	Description	Qty
BASIC CLOCKS AND RESETS				
SYSRSTI#	I	SCHMITT_FT	System Reset / Power good	1
SYSRSTO#	O	BD8STRP_FT	Reset Output to System	1
XTALI	I	OSCI13B	14.31818 MHz Crystal Input External Oscillator Input	1
XTALO	O		14.31818 MHz Crystal Output	1
PCI_CLKI	I	TLCHT_FT	33 MHz PCI Input Clock	1
PCI_CLKO	O	BT8TRP_TC	33 MHz PCI Output Clock	1
ISA_CLK, ISA_CLK2X	O	BT8TRP_TC	ISA Clock x1 and x2 Multiplexer Select Line for IPC	2
OSC14M	O	BD8STRP_FT	ISA bus synchronisation clock	1
HCLK	I/O	BD4STRP_FT	66 MHz Host Clock (Test pin)	1
DEV_CLK	O	BT8TRP_TC	24 MHz Peripheral Clock	1
DCLK	I/O	BD4STRP_FT	135 MHz Dot Clock	1
V_{DD}_xxx_PLL			2.5V Power Supply for PLL Clocks	7
MEMORY CONTROLLER				
MCLKI	I	TLCHT_TC	Memory Clock Input	1
MCLKO	O	BT8TRP_TC	Memory Clock Output	1
Note[1]; See Table 2-3 for buffer type descriptions				

Table 2-2. Definition of Signal Pins

Signal Name	Dir	Buffer Type[1]	Description	Qty
CS#[1:0]	O	BD8STRP_TC	DIMM Chip Select	2
CS#[3]/MA[12]/BA[1]	O	BD16STARUQP_TC	DIMM Chip Select Memory Address Bank Address	1
CS#[2]/MA[11]	O	BD16STARUQP_TC	DIMM Chip Select Memory Address	1
MA[10:0]	O	BD16STARUQP_TC	Memory Row & Column Address	11
BA[0]	O	BD16STARUQP_TC	Bank Address	1
RAS#[1:0]	O	BD16STARUQP_TC	Row Address Strobe	2
CAS#[1:0]	O	BD16STARUQP_TC	Column Address Strobe	2
MWE#	O	BD16STARUQP_TC	Write Enable	1
MD[0]	I/O	BD8STRUP_FT	Memory Data	1
MD[53:1]	I/O	BD8TRP_TC	Memory Data	53
MD[63:54]	I/O	BD8STRUP_FT	Memory Data	10
DQM[7:0]	O	BD8STRP_TC	Data Input/Ouput Mask	8
PCI INTERFACE				
AD[31:0]	I/O	BD8PCIARP_FT	Address / Data	32
CBE[3:0]	I/O	BD8PCIARP_FT	Bus Commands / Byte Enables	4
FRAME#	I/O	BD8PCIARP_FT	Cycle Frame	1
TRDY#	I/O	BD8PCIARP_FT	Target Ready	1
IRDY#	I/O	BD8PCIARP_FT	Initiator Ready	1
STOP#	I/O	BD8PCIARP_FT	Stop Transaction	1
DEVSEL#	I/O	BD8PCIARP_FT	Device Select	1
PAR	I/O	BD8PCIARP_FT	Parity Signal Transactions	1
PERR#	I/O	BD8PCIARP_FT	Parity Error	1
SERR#	O	BD8PCIARP_FT	System Error	1
LOCK#	I	TLCHT_FT	PCI Lock	1
PCI_REQ#[2:0]	I	BD8PCIARP_FT	PCI Request	3
PCI_GNT#[2:0]	O	BD8PCIARP_FT	PCI Grant	3
PCI_INT#[3:0]	I	BD4STRUP_FT	PCI Interrupt Request	4
ISA BUS INTERFACE				
LA[23:17]	O	BD8STRUP_FT	Unlatched Address Bus	7
SA[19:0]	O	BD8STRUP_FT	Latched Address Bus	20
SD[15:0]	I/O	BD8STRP_FT	Data Bus	16
IOCHRDY	I	BD8STRUP_FT	I/O Channel Ready	1
ALE	O	BD4STRP_FT	Address Latch Enable	1
BHE#	O	BD8STRUP_FT	System Bus High Enable	1
MEMR#, MEMW#	I/O	BD8STRUP_FT	Memory Read & Write	2
SMEMR#, SMEMW#	O	BD8STRP_FT	System Memory Read and Write	2
IOR#, IOW#	I/O	BD8STRUP_FT	I/O Read and Write	2
MASTER#	I	BD4STRUP_FT	Add On Card Owns Bus	1
MCS16#	I	BD4STRUP_FT	Memory Chip Select 16	1
IOCS16#	I	BD4STRUP_FT	I/O Chip Select 16	1
REF#	I	BD8STRP_FT	Refresh Cycle	1
AEN	O	BD8STRUP_FT	Address Enable	1
IOCHCK#	I	BD4STRUP_FT	I/O Channel Check (ISA)	1
RTCRW#	O	BD4STRP_FT	RTC Read / Write#	1
Note[1]; See Table 2-3 for buffer type descriptions				

Table 2-2. Definition of Signal Pins

Signal Name	Dir	Buffer Type[1]	Description	Qty
RTCDS#	O	BD4STRP_FT	RTC Data Strobe	1
RTCAS	O	BD4STRP_FT	RTC Address Strobe	1
RMRTCCS#	O	BD4STRP_FT	ROM / RTC Chip Select	1
GPIOCS#	I/O	BD4STRP_FT	General Purpose Chip Select	1
IRQ_MUX[3:0]	I	BD4STRP_FT	Multiplexed Interrupt Request	4
DACK_ENC[2:0]	O	BD4STRP_FT	DMA Acknowledge	3
DREQ_MUX[1:0]	I	BD4STRP_FT	Multiplexed DMA Request	2
TC	O	BD4STRP_FT	ISA Terminal Count	1
ISAOE#	I	BD4STRP_FT	ISA (0) / IDE (1) SELECTION	1
KBCS#	I/O	BD4STRP_FT	External Keyboard CHIP SELECT	1
ZWS#	I	BD4STRP_FT	ZERO WAIT STATE	1
PCMCIA INTERFACE				
RESET	O	BD8STRP_FT	Reset	1
A[23:0]	O	BD8STRUP_FT	Address Bus	24
D[15:0]	I/O	BD8STRP_FT	Data Bus	16
IORD#, IOWR#	O	BD8STRUP_FT	I/O Read and Write	2
WP / IOIS16#	I	BD4STRUP_FT	DMA Request // Write Protect I/O Size is 16 bit	1
BVD2, BVD1	I	BD4STRUP_FT	Battery Voltage Detect	2
READY# / IREQ#	I	BD4STRUP_FT	Busy / Ready# // Interrupt Request	1
WAIT#	I	BD8STRUP_FT	Wait	1
OE#	O	BD8STRUP_FT	Output Enable // DMA Terminal Count	1
WE#	O	BD4STRP_FT	Write Enable // DMA Terminal Count	1
REG#	O	BD4STRUP_FT	DMA Acknowledge // Register	1
CD2#, CD1#	I	BD4STRUP_FT	Card Detect	2
CE2#, CE1#	O	BD4STRP_FT	Card Enable	2
VCC5_EN	O	BD4STRP_FT	Power Switch control: 5 V power	1
VCC3_EN	O	BD8STRP_FT	Power Switch control: 3.3 V power	1
VPP_PGM	O	BD8STRP_FT	Power Switch control: Program power	1
VPP_VCC	O	BD4STRP_FT	Power Switch control: VCC power	1
GPI#	I	BD4STRP_FT	General Purpose Input	1
LOCAL BUS INTERFACE				
PA[24:20,15,9:8,3:0]	O	BD4STRP_FT	Address Bus [24:20], [15], [9:8], [3:0]	12
PA[19,11]	O	BD8STRP_FT	Address Bus [19], [11]	2
PA[18:16,14:12,7:4]	O	BD8STRUP_FT	Address Bus [18:16], [14:12], [7:4]	10
PA[10]	O	BD4STRUP_FT	Address Bus [10]	1
PD[15:0]	I/O	BD8STRP_FT	Data Bus [15:0]	16
PRD#	O	BD4STRUP_FT	Memory and I/O Read signal	1
PWR#	O	BD4STRUP_FT	Memory and I/O Write signal	1
PRDY	I	BD8STRUP_FT	Data Ready	1
IOCS#[7:4]	O	BD4STRUP_FT	I/O Chip Select	4
IOCS#[3]	O	BD4STRP_FT	I/O Chip Select	1
IOCS#[2:0]	O	BD8STRUP_FT	I/O Chip Select	3
PBE#[1]	O	BD8STRP_FT	Upper Byte Enable (PD[15:8])	1
PBE#[0]	O	BD4STRUP_FT	Lower Byte Enable (PD[7:0])	1
FCS0#	O	BD4STRP_FT	Flash Bank 0 Chip Select	1
FCS1#	O	BT8TRP_TC	Flash Bank 1 Chip Select	1
Note[1]; See Table 2-3 for buffer type descriptions				

Table 2-2. Definition of Signal Pins

Signal Name	Dir	Buffer Type[1]	Description	Qty
FCS_0H#	O	BD8STRP_FT	Upper half Bank 0 Flash Chip Select	1
FCS_0L#	O	BD8STRP_FT	Lower half Bank 0 Flash Chip Select	1
FCS_1H#	O	BD8STRP_FT	Upper half Bank 1 Flash Chip Select	1
FCS_1L#	O	BD8STRP_FT	Lower half Bank 1 Flash Chip Select	1
IRQ_MUX[3:0][1]	I/O	BD4STRP_FT	Muxed Interrupt Lines	4
IDE CONTROLLER				
DD[15:12]	I/O	BD4STRP_FT	Data Bus	4
DD[11:0]	I/O	BD8STRUP_FT	Data Bus	12
DA[2:0]	O	BD8STRUP_FT	Address Bus	3
PCS1, PCS3	O	BD8STRUP_FT	Primary Chip Selects	2
SCS1, SCS3	O	BD8STRUP_FT	Secondary Chip Selects	2
DIORDY	O	BD8STRUP_FT	Data I/O Ready	1
PIRQ/SIRQ	I	BD4STRP_FT	Primary / Secondary Interrupt Request	2
PDRQ/SDRQ	I	BD4STRP_FT	Primary / Secondary DMA Request	2
PDACK#/SDACK#	O	BD8STRP_FT	Primary / Secondary DMA Acknowledge	2
PDIOR#/SDIOR#	O	BD8STRUP_FT	Primary / Secondary IO Read	2
PDIOW#/SDIOW#	O	BD8STRP_FT	Primary / Secondary IO Write	2
VGA CONTROLLER				
RED, GREEN, BLUE	O	VDDCO	Red, Green, Blue	3
VSYNC, HSYNC	I/O	BD4STRP_FT	Vertical & Horizontal Synchronisations	2
VREF_DAC	I	ANA	DAC Voltage reference	1
RSET	I	ANA	Resistor Set	1
COMP	I	ANA	Compensation	1
COL_SEL	O	BD4STRP_FT	Colour Select	1
I2C INTERFACE				
SCL / DDC[1]	I/O	BD4STRUP_FT	I²C Interface - Clock / VGA DDC[1]	1
SDA / DDC[0]	I/O	BD4STRUP_FT	I²C Interface - Data / VGA DDC[0]	1
TFT INTERFACE				
TFTR[5:2]	O	BD4STRP_TC	Red	4
TFTR[1:0]	O	BD4STRP_FT	Red	2
TFTG[5:2]	O	BD4STRP_TC	Green	4
,TFTG[1:0]	O	BD4STRP_FT	Green	2
TFTB[5:2]	O	BD4STRP_TC	Blue	4
TFTB[1:0]	O	BD4STRP_FT	Blue	2
TFTLINE	O	BD8STRP_TC	Horizontal Sync	1
TFTFRAME	O	BD4STRP_TC	Vertical Sync	1
TFTDE	O	BD4STRP_TC	Data Enable	1
TFTENVDD, TFTENVCC	O	BD4STRP_TC	Enable Vdd & Vcc of flat panel	2
TFTPWM	O	BD8STRP_TC	PWM back-light control	1
TFTDCLK	O	BT8TRP_TC	Dot clock for Flat Panel	1
VIDEO INPUT PORT				
VCLK	I/O	BD8STRP_FT	27-33 MHz Video Input Port Clock	1
VIN[7:0]	I	BD4STRP_FT	Video Input Data Bus	8
ODD_EVEN#	I/O	BD4STRP_FT	Video Input Odd/even Field	1
VCS	I/O	BD4STRP_FT	Video Input Horizontal Sync	1
Note[1]; See Table 2-3 for buffer type descriptions				

Table 2-2. Definition of Signal Pins

Signal Name	Dir	Buffer Type[1]	Description	Qty
USB INTERFACE				
OC	I	TLCHTU_TC	Over Current Detect	1
USBDPLS[0][1] USBDMNS[0][1]	I/O	USBDS_2V5	Universal Serial Bus Port 0	2
USBDPLS[1][1] USBDMNS[1][1]	I/O	USBDS_2V5	Universal Serial Bus Port 1	2
POWERON[1]	O	BT4CRP	USB power supply lines	1
SERIAL CONTROLLER				
CTS0#, CTS1#	I	TLCHT_FT	Clear to send, MSR[4] status bit	2
DCD0#, DCD1#	I	TLCHT_FT	Data Carrier detect, MSR[7] status bit	2
DSR0#, DSR1#	I	TLCHT_FT	Data set ready, MSR[5] status bit.	2
DTR0#, DTR1#	O	BD4STRP_TC	Data terminal ready, MSR[0] status bit	2
RI0#, RI1#	I	TLCHT_FT	Ring indicator, MSR[6] status bit	2
RTS0#, RTS1#	O	BD4STRP_TC	Request to send, MSR[1] status bit	2
RXD0, RXD1	I	TLCHT_FT	Receive data, Input Serial Input	2
TXD0, TXD1	O	BD4STRP_TC	Transmit data, Serial Output	2
KEYBOARD & MOUSE INTERFACE				
KBCLK	I/O	BD4STRP_TC	Keyboard Clock Line	1
KBDATA	I/O	BD4STRP_TC	Keyboard Data Line	1
MCLK	I/O	BD4STRP_TC	Mouse Clock Line	1
MDATA	I/O	BD4STRP_TC	Mouse Data Line	1
PARALLEL PORT				
PE	I	BD14STARP_FT	Paper End	1
SLCT	I	BD14STARP_FT	SELECT	1
BUSY#	I	BD14STARP_FT	BUSY	1
ERR#	I	BD14STARP_FT	ERROR	1
ACK#	I	BD14STARP_FT	Acknowledge	1
PDIR#	O	BD14STARP_FT	Parallel Device Direction	1
STROBE#	O	BD14STARP_FT	PCS / STROBE#	1
INIT#	O	BD14STARP_FT	INIT	1
AUTOFD#	O	BD14STARP_FT	Automatic Line Feed	1
SLCTIN#	O	BD14STARP_FT	SELECT IN	1
PPD[7:0]	I/O	BD14STARP_FT	Data Bus	8
GPIO SIGNALS				
GPIO[15:0]	I/O	BD4STRP_FT	General Purpose IOs	16
JTAG				
TCLK	I	TLCHT_FT	Test Clock	1
TRST	I	TLCHT_FT	Test Reset	1
TDI	I	TLCHTD_FT	Test Data Input	
TMS	I	TLCHT_FT	Test Mode Set	1
TDO	O	BT8TRP_TC	Test Data output	1
MISCELLANEOUS				
SCAN_ENABLE	I	TLCHTD_FT	Test Pin - Reserved	1
Note[1]; See Table 2-3 for buffer type descriptions				

Table 2-2. Definition of Signal Pins

Signal Name	Dir	Buffer Type[1]	Description	Qty
SPKRD	O	BD4STRP_FT	Speaker Device Output	1
Note[1]; See Table 2-3 for buffer type descriptions				

Table 2-3. Buffer Type Descriptions

Buffer	Description
ANA	Analog pad buffer
OSCI13B	Oscillator, 13 MHz, HCMOS
BT4CRP	LVTTL Output, 4 mA drive capability, Tri-State Control
BT8TRP_TC	LVTTL Output, 8 mA drive capability, Tri-State Control, Schmitt trigger
BD4STRP_FT	LVTTL Bi-Directional, 4 mA drive capability, Schmitt trigger, 5V tolerant
BD4STRUP_FT	LVTTL Bi-Directional, 4 mA drive capability, Schmitt trigger, Pull-Up, 5V tolerant
BD4STRP_TC	LVTTL Bi-Directional, 4 mA drive capability, Schmitt trigger
BD8STRP_FT	LVTTL Bi-Directional, 8 mA drive capability, Schmitt trigger, 5V tolerant
BD8STRUP_FT	LVTTL Bi-Directional, 8 mA drive capability, Schmitt trigger, Pull-Up, 5V tolerant
BD8STRP_TC	LVTTL Bi-Directional, 8 mA drive capability, Schmitt trigger
BD8TRP_TC	LVTTL Bi-Directional, 8 mA drive capability, Schmitt trigger
BD8PCIARP_FT	LVTTL Bi-Directional, 8 mA drive capability, PCI compatible, 5V tolerant
BD14STARP_FT	LVTTL Bi-Directional, 14 mA drive capability, Schmitt trigger, IEEE1284 compliant, 5V tolerant
BD16STARUQP_TC	LVTTL Bi-Directional, 16 mA drive capability, Schmitt trigger
SCHMITT_FT	LVTTL Input, Schmitt trigger, 5V tolerant
TLCHT_FT	LVTTL Input, 5V tolerant
TLCHT_TC	LVTTL Input
TLCHTD_TC	LVTTL Input, Pull-Down
TLCHTU_TC	LVTTL Input, Pull-Up
USBDS_2V5	USB 1.1 compliant pad buffer
VDDCO	Analog output pad

2.2. SIGNAL DESCRIPTIONS

2.2.1. BASIC CLOCKS AND RESETS

SYSRSTI# *System Reset/Power good.* This input is low when the reset switch is depressed. Otherwise, it reflects the power supply's power good signal. PWGD is asynchronous to all clocks, and acts as a negative active reset. The reset circuit initiates a hard reset on the rising edge of PWGD.

Note that while Reset is being asserted, the signals on the device pins are in an unknown state.

SYSRSTO# *Reset Output to System.* This is the system reset signal and is used to reset the rest of the components (not on Host bus) in the system. The ISA bus reset is an externally inverted buffered version of this output and the PCI bus reset is an externally buffered version of this output.

XTALI *14.3 MHz Crystal Input*
XTALO *14.3 MHz Crystal Output.* These pins are provided for the connection of an external 14.318 MHz crystal to provide the reference clock for the internal frequency synthesizer, from which the HCLK and CLK24M signals are generated.

PCI_CLKI *33 MHz PCI Input Clock.* This signal must be connected to a clock generator and is usually connected to PCI_CLKO.

PCI_CLKO *33 MHz PCI Output Clock.* This is the master PCI bus clock output.

ISA_CLK *ISA Clock Output (also Multiplexer Select Line For IPC).* This pin produces the Clock signal for the ISA bus. It is also used with ISA_CLK2X as the multiplexer control lines for the Interrupt Controller Interrupt input lines. This is a divided down version of the PCICLK or OSC14M.

ISA_CLKX2 *ISA Clock Output (also Multiplexer Select Line For IPC).* This pin produces a signal at twice the frequency of the ISA bus Clock signal. It is also used with ISA_CLK as the multiplexer control lines for the Interrupt Controller Interrupt input lines.

CLK14M *ISA bus synchronisation clock.* This is the buffered 14.318 MHz clock to the ISA bus.

HCLK *Host Clock.* This is the host clock. Its frequency can vary from 25 to 66 MHz. All host transactions and PCI transactions are synchronized to this clock. Host transactions executed by the DRAM controller are also driven by this clock.

DEV_CLK *24 MHz Peripheral Clock (floppy drive).* This 24 MHz signal is provided as a convenience for the system integration of a Floppy Disk driver function in an external chip. This clock signal is not available in Local Bus mode.

DCLK *135 MHz Dot Clock.* This is the dot clock, which drives graphics display cycles. Its frequency can be as high as 135 MHz, and it is required to have a worst case duty cycle of 60-40. For further details, refer to Section 3.1.4. bit 4.

2.2.2. MEMORY INTERFACE

MCLKI *Memory Clock Input.* This clock is driving the SDRAM controller, the graphics engine and display controller. This input should be a buffered version of the MCLKO signal with the track lengths between the buffer and the pin matched with the track lengths between the buffer and the Memory Banks.

MCLKO *Memory Clock Output.* This clock drives the Memory Banks on board and is generated from an internal PLL.

The STPC Atlas MClock signal can run up to 100MHz reliably, but PCB layout is so critical that the maximum guaranteed speed is 90MHz

CS#[1:0] *Chip Select* These signals are used to disable or enable device operation by masking or enabling all SDRAM inputs except MCLK, CKE, and DQM.

CS#[2]/MA[11] *Chip Select/Bank Address* This pin is CS#[2] in the case when 16-Mbit devices are used. For all other densities, it becomes MA[11].

CS#[3]/MA[12]/BA[1] *Chip Select/ Memory Address/ Bank Address* This pin is CS#[3] in the case when 16 Mbit devices are used. For all other densities, it becomes MA[12] when 2 internal banks devices are used and BA[1] when 4 internal bank devices are used.

MA[10:0] *Memory Address.* Multiplexed row and column address lines.

BA[0] *Bank Address.* Internal bank address line.

MD[63:0] *Memory Data.* This is the 64-bit memory data bus. This bus is also used as input at the rising edge of SYSRSTI# to latch in power-up configuration information into the ADPC strap registers.

RAS#[1:0] *Row Address Strobe.* There are two active-low row address strobe output signals. The RAS# signals drive the memory devices directly without any external buffering.

CAS#[1:0] *Column Address Strobe.* There are two active-low column address strobe output signals. The CAS# signals drive the memory devices directly without any external buffering.

MWE# *Write Enable.* Write enable specifies whether the memory access is a read (MWE# = H) or a write (MWE# = L). This single write enable controls all DRAMs. The MWE# signals drive the memory devices directly without any external buffering.

2.2.3. PCI INTERFACE

AD[31:0] *PCI Address/Data.* This is the 32-bit multiplexed address and data bus of the PCI. This bus is driven by the master during the address phase and data phase of write transactions. It is driven by the target during data phase of read transactions.

PBE[3:0]# *Bus Commands/Byte Enables.* These are the multiplexed command and Byte enable signals of the PCI bus. During the address phase they define the command and during the data phase they carry the Byte enable information. These pins are inputs when a PCI master other than the STPC Atlas owns the bus and outputs when the STPC Atlas owns the bus.

FRAME# *Cycle Frame.* This is the frame signal of the PCI bus. It is an input when a PCI master owns the bus and is an output when STPC Atlas owns the PCI bus.

TRDY# *Target Ready.* This is the target ready signal of the PCI bus. It is driven as an output when the STPC Atlas is the target of the current bus transaction. It is used as an input when STPC Atlas initiates a cycle on the PCI bus.

IRDY# *Initiator Ready.* This is the initiator ready signal of the PCI bus. It is used as an output when the STPC Atlas initiates a bus cycle on the PCI bus. It is used as an input during the PCI cycles targeted to the STPC Atlas to determine when the current PCI master is ready to complete the current transaction.

STOP# *Stop Transaction.* STOP# is used to implement the disconnect, retry and abort protocol of the PCI bus. It is used as an input for the bus cycles initiated by the STPC Atlas and is used as an output when a PCI master cycle is targeted to the STPC Atlas.

DEVSEL# *Device Select.* This signal is used as an input when the STPC Atlas initiates a bus cycle on the PCI bus to determine if a PCI slave device has decoded itself to be the target of the current transaction. It is asserted as an output either when the STPC Atlas is the target of the current PCI transaction or when no other device asserts DEVSEL# prior to the subtractive decode phase of the current PCI transaction.

PAR *Parity Signal Transactions.* This is the parity signal of the PCI bus. This signal is used to guarantee even parity across AD[31:0], CBE[3:0]#, and PAR. This signal is driven by the master during the address phase and data phase of write transactions. It is driven by the target during data phase of read transactions. (Its assertion is identical to that of the AD bus delayed by one PCI clock cycle)

PERR# *Parity Error*

SERR# *System Error.* This is the system error signal of the PCI bus. It may, if enabled, be asserted for one PCI clock cycle if target aborts a STPC Atlas initiated PCI transaction. Its assertion by either the STPC Atlas or by another PCI bus agent will trigger the assertion of NMI to the host CPU. This is an open drain output.

LOCK# *PCI Lock.* This is the lock signal of the PCI bus and is used to implement the exclusive bus operations when acting as a PCI target agent.

PCI_REQ#[2:0] *PCI Request.* These pins are the three external PCI master request pins. They indicates to the PCI arbiter that the external agents desire use of the bus.

PCI_GNT#[2:0] *PCI Grant.* These pins indicate that the PCI bus has been granted to the master requesting it on its PCI_REQ#.

PCI_INT#[3:0] *PCI Interrupt Request.* These are the PCI bus interrupt signals. They are to be encoded before connection to the STPC Atlas using ISACLK and ISACLKX2 as the input selection strobes.

2.2.4. ISA BUS INTERFACE

LA[23:17] *Unlatched Address.* These unlatched ISA Bus pins address bits 23-17 on 16-bit devices. When the ISA bus is accessed by any cycle initiated from the PCI bus, these pins are in output mode. When an ISA bus master owns the bus, these pins are tristated.

SA[19:0] *Unlatched Address.* These are the 20 low bits of the system address bus of ISA. These pins are used as an input when an ISA bus master owns the bus and are outputs at all other times.

SD[15:0] *I/O Data Bus (ISA).* These are the external ISA databus pins.

IOCHRDY *IO Channel Ready.* IOCHRDY is the IO channel ready signal of the ISA bus and is driven as an output in response to an ISA master cycle targeted to the host bus or an internal register of the STPC Atlas. The STPC Atlas monitors this signal as an input when performing an ISA cycle on behalf of the host CPU, DMA master or refresh. ISA masters which do not monitor IOCHRDY are not guaranteed to work with the STPC Atlas since the access to the system memory can be considerably delayed due to CRT refresh or a write back cycle.

ALE *Address Latch Enable.* This is the address latch enable output of the ISA bus and is asserted by the STPC Atlas to indicate that LA23-17, SA19-0, AEN and SBHE# signals are valid. The ALE is driven high during refresh, DMA master or an ISA master cycles by the STPC Atlas.
ALE is driven low after reset.

BHE# *System Bus High Enable.* This signal, when asserted, indicates that a data Byte is being transferred on SD15-8 lines. It is used as an input when an ISA master owns the bus and is an output at all other times.

MEMR# *Memory Read.* This is the memory read command signal of the ISA bus. It is used as an input when an ISA master owns the bus and is an output at all other times.
The MEMR# signal is active during refresh.

MEMW# *Memory Write.* This is the memory write command signal of the ISA bus. It is used as an input when an ISA master owns the bus and is an output at all other times.

SMEMR# *System Memory Read.* The STPC Atlas generates SMEMR# signal of the ISA bus only when the address is below one MByte or the cycle is a refresh cycle.

SMEMW# *System Memory Write.* The STPC Atlas generates SMEMW# signal of the ISA bus only when the address is below one MByte.

IOR# *I/O Read.* This is the IO read command signal of the ISA bus. It is an input when an ISA master owns the bus and is an output at all other times.

IOW# *I/O Write.* This is the IO write command signal of the ISA bus. It is an input when an ISA master owns the bus and is an output at all other times.

MASTER# *Add On Card Owns Bus.* This signal is active when an ISA device has been granted bus ownership.

MCS16# *Memory Chip Select16.* This is the decode of LA23-17 address pins of the ISA address bus without any qualification of the command signal lines. MCS16# is always an input. The STPC Atlas ignores this signal during IO and refresh cycles.

IOCS16# *IO Chip Select16.* This signal is the decode of SA15-0 address pins of the ISA address bus without any qualification of the command signals. The STPC Atlas does not drive IOCS16# (similar to PC-AT design). An ISA master access to an internal register of the STPC Atlas is executed as an extended 8-bit IO cycle.

REF# *Refresh Cycle.* This is the refresh command signal of the ISA bus. It is driven as an output when the STPC Atlas performs a refresh cycle on the ISA bus. It is used as an input when an ISA master owns the bus and is used to trigger a refresh cycle.
The STPC Atlas performs a pseudo hidden refresh. It requests the host bus for two host clocks to drive the refresh address and capture it in external buffers. The host bus is then relinquished while the refresh cycle continues on the ISA bus.

AEN *Address Enable.* Address Enable is enabled when the DMA controller is the bus owner to indicate that a DMA transfer will occur. The enabling of the signal indicates to IO devices to ignore the IOR#/IOW# signal during DMA transfers.

IOCHCK# *IO Channel Check.* IO Channel Check is enabled by any ISA device to signal an error condition that can not be corrected. NMI signal becomes active upon seeing IOCHCK# active if the corresponding bit in Port B is enabled.

GPIOCS# *I/O General Purpose Chip Select 1.* This output signal is used by the external latch on ISA bus to latch the data on the SD[7:0] bus. The latch can be use by PMU unit to control the external peripheral devices to power down or any other desired function.

RTCRW# *Real Time Clock RW#.* This pin is used as RTCRW#. This signal is asserted for any I/O write to port 71h.

RTCDS# *Real Time Clock DS*. This pin is used as RTCDS#. This signal is asserted for any I/O read to port 71h. Its polarity complies with the DS pin of the MT48T86 RTC device when configured with Intel timings.

RTCAS *Real time clock address strobe.* This signal is asserted for any I/O write to port 70h.

RMRTCCS# *ROM/Real Time clock chip select.* This pin is a multi-function pin. This signal is asserted if a ROM access is decoded during a memory cycle. It should be combined with MEMR# or MEMW# signals to properly access the ROM. During an IO cycle, this signal is asserted if access to the Real Time Clock (RTC) is decoded. It should be combined with IOR# or IOW# signals to properly access the real time clock.

IRQ_MUX[3:0] *Multiplexed Interrupt Request.* These are the ISA bus interrupt signals. They are to be encoded before connection to the STPC Atlas using ISACLK and ISACLKX2 as the input selection strobes.
Note that IRQ8B, which by convention is connected to the RTC, is inverted before being sent to the interrupt controller, so that it may be connected directly to the IRQ# pin of the RTC.

ISAOE# *Bidirectional OE Control.* This signal controls the OE signal of the external transceiver that connects the IDE DD bus and ISA SA bus.

KBCS# *Keyboard Chip Select.* This signal is asserted if a keyboard access is decoded during a I/O cycle.

ZWS# *Zero Wait State.* This signal, when asserted by addressed device, indicates that current cycle can be shortened.

DACK_ENC[2:0] *DMA Acknowledge.* These are the ISA bus DMA acknowledge signals. They are encoded by the STPC Atlas before output and should be decoded externally using ISACLK and ISACLKX2 as the control strobes.

DREQ_MUX[1:0] *ISA Bus Multiplexed DMA Request.* These are the ISA bus DMA request signals. They are to be encoded before connection to the STPC Atlas using ISACLK and ISACLKX2 as the input selection strobes.

TC *ISA Terminal Count.* This is the terminal count output of the DMA controller and is connected to the TC line of the ISA bus. It is asserted during the last DMA transfer, when the Byte count expires.

2.2.5. PCMCIA INTERFACE

RESET *Card Reset.* This output forces a hard reset to a PC Card.

A[25:0] *Address Bus.* These are the 25 low bits of the system address bus of the PCMCIA bus. These pins are used as an input when an PCMCIA bus owns the bus and are outputs at all other times.

D[15:0] *I/O Data Bus (PCMCIA).* These are the external PCMCIA databus pins.

IORD# *I/O Read.* This output is used with REG# to gate I/O read data from the PC Card, (only when REG# is asserted).

IOWR# *I/O Write.* This output is used with REG# to gate I/O write data from the PC Card, (only when REG# is asserted).

WP *Write Protect.* This input indicates the status of the Write Protect switch (if fitted) on memory PC Cards (asserted when the switch is set to write protect).

BVD1, BVD2 *Battery Voltage Detect.* These inputs will be generated by memory PC Cards that include batteries and are an indication of the condition of the batteries. BVD1 and BVD2 are kept asserted high when the battery is in good condition.

READY#/BUSY#/IREQ# *Ready/busy/Interrupt request.* This input is driven low by memory PC Cards to signal that their circuits are busy processing a previous write command.

WAIT# *Bus Cycle Wait.* This input is driven by the PC Card to delay completion of the memory or I/O cycle in progress.

OE# *Output Enable.* OE# is an active low output which is driven to the PC Card to gate Memory Read data from memory PC Cards.

WE#/PRGM# *Write Enable.* This output is used by the host for gating Memory Write data. WE# is also used for memory PC Cards that have programmable memory.

REG# *Attribute Memory Select.* This output is inactive (high) for all normal accesses to the Main Memory of the PC Card. I/O PC Cards will only respond to IORD# or IOWR# when REG# is active (low). Also see Section 2.2.7.

CD1#, CD2# *Card Detect.* These inputs provide for the detection of correct card insertion. CD#1 and CD#2 are positioned at opposite ends of the connector to assist in the detection process. These inputs are internally grounded on the PC Card therefore they will be forced low whenever a card is inserted in a socket.

CE1#, CE2# *Card Enable.* These are active low output signals provided from the PCIC. CE#1 enables even Bytes, CE#2 odd Bytes.

ENABLE# *Enable.* This output is used to activate/ select a PC Card socket. ENABLE# controls the external address buffer logic.C card has been detected (CD#1 and CD#2 = '0').

ENIF# *ENIF*. This output is used to activate/select a PC Card socket.

EXT_DIR *EXternal Transceiver Direction Control.* This output is high during a read and low during a write. The default power up condition is write (low). Used for both Low and High Bytes of the Data Bus.

VCC_EN#, VPP1_EN0, VPP1_EN1, VPP 2_EN0, VPP2_EN1 *Power Control*. Five output signals used to control voltages (VPP1, VPP2 and VCC) to a PC Card socket.

GPI# *General Purpose Input. This signal is hardwired to 1.*

2.2.6. LOCAL BUS

PA[24:0] *Address Bus Output.*

PD[15:0] *Data Bus.* This is the 16-bit data bus. D[7:0] is the LSB and PD[15:8] is the MSB.

PRD#[1:0] *Read Control output*. These are memory and I/O Read signals. PRD0# is used to read the LSB and PRD1# to read the MSB.

PWR#[1:0] *Write Control output.* These are memory and I/O Write signals. PWR0# is used to write the LSB and PWR1# to write the MSB.

PRDY *Data Ready input.* This signal is used to create wait states on the bus. When high, it completes the current cycle.

FCS#[1:0] *Two Flash Memory Chip Select outputs.* These are the Programmable Chip Select signals for Flash memory.

IOCS#[7:0] *I/O Chip Select output.* These are the Programmable Chip Select signals for up to 4 external I/O devices.

PBE#[1:0] *Byte Enable.* These are the Byte enables that identifies on which databus the date is valid. PBE#[0] corresponds to PD[7:0] and PBE#[1] corresponds to PD[15:8]. These are normally used when 8 bit transfers are transfered across the 16 bit bus.

IRQ_MUX#[3:0] *Multiplexed Interrupt Lines.*

2.2.7. IPC

DACK_ENC[2:0] *DMA Acknowledge.* These are the ISA bus DMA acknowledge signals. They are encoded by the STPC Industrial before output and should be decoded externally using ISACLK and ISACLKX2 as the control strobes.

DREQ_MUX[1:0] *ISA Bus Multiplexed DMA Request.* These are the ISA bus DMA request signals. They are to be encoded before connection to the STPC Industrial using ISACLK and ISACLKX2 as the input selection strobes.

TC *ISA Terminal Count.* This is the terminal count output of the DMA controller and is connected to the TC line of the ISA bus. It is asserted during the last DMA transfer, when the Byte count expires.

2.2.8. IDE INTERFACE

DA[2:0] *Address.* These signals are connected to DA[2:0] of IDE devices directly or through a buffer. If the toggling of signals are to be masked during ISA bus cycles, they can be externally ORed with ISAOE# before being connected to the IDE devices.

DD[15:0] *Databus.* When the IDE bus is active, they serve as IDE signals DD[11:0]. IDE devices are connected to SA[19:8] directly and ISA bus is connected to these pins through two LS245 transceivers.

PCS1, PCS3, SCS1, SCS3 *Primary & Secondary Chip Selects.* These signals are used as the active high primary and secondary master & slave IDE chip select signals. These signals must be externally NANDed with the ISAOE# signal before driving the IDE devices to guarantee it is active only when ISA bus is idle. In Local Bus mode, they just need to be inverted.

DIORDY *Busy/Ready.* This pin serves as IDE signal DIORDY.

PIRQ *Primary Interrupt Request.*
SIRQ *Secondary Interrupt Request.*
Interrupt request from IDE channels.

PDRQ *Primary DMA Request.*
SDRQ *Secondary DMA Request.*
DMA request from IDE channels.

PDACK# *Primary DMA Acknowledge.*
SDACK# *Secondary DMA Acknowledge.*
DMA acknowledge to IDE channels.

PDIOR#, PDIOW# *Primary I/O Read & Write.*
SDIOR#, SDIOW# *Secondary I/O Read & Write*.
Primary & Secondary channel read & write.

2.2.9. MONITOR INTERFACE

RED, GREEN, BLUE *RGB Video Outputs.* These are the 3 analog colour outputs from the RAMDACs. These signals are sensitive to interference, therefore they need to be properly shielded.