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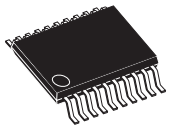
STPM01

Programmable single phase energy metering IC with tamper detection

Features

- Active, reactive, apparent energies and RMS values
- Ripple free active energy pulsed output
- Live and neutral monitoring for tamper detection
- Easy and fast digital calibration in only one point over the whole current range
- OTP for calibration and configuration
- Integrated linear VREGs for digital and analog supply
- Selectable RC or crystal oscillator
- Support 50 ÷ 60 Hz – IEC62052-11, IEC62053-2x specification
- Less than 0.1 % error
- Precision voltage reference: 1.23 V and 30 ppm/°C max



TSSOP20

Description

The STPM01 is designed for effective measurement of active, reactive and apparent energy in a power line system using Rogowski coil, current transformer and shunt sensors. This device can be implemented as a single chip monophase energy meter or as a peripheral measurement in a microcontroller based monophase or 3-phase energy meter. The STPM01 consists, essentially, of two parts: the analog part and the digital part. The former, is composed by preamplifier and 1st order $\Delta\sum$ A/D converter blocks, band gap voltage reference, low drop voltage regulator, the latter, is composed by system control, oscillator, hard wired DSP and SPI interface. There is also an OTP block, which is controlled through the SPI by means of a dedicated command set. The configured bits are used for testing, configuration and calibration purpose. From a pair of $\Delta\sum$ output signals coming from analog section, a DSP unit computes the amount of consummated active, reactive and apparent energy, RMS and instantaneous values of voltage and current. The results of computation are available as pulse frequency and states on the digital outputs of the device or as data bits in a data stream, which can be read from the device by means of SPI interface. This system bus interface is used also during production testing of the device and/or for temporary or permanent programming of bits of internal OTP. In the STPM01 an output signal with pulse frequency proportional to energy is generated, this signal is used in the calibration phase of the energy meter application allowing a very easy approach. When the device is fully configured and calibrated, a dedicated bit of OTP block can be written permanently in order to prevent accidental entering into some test mode or changing any configuration bit.

Table 1. Device summary

Order code	Temperature range	Package	Packaging
STPM01FTR	- 40 to 85 °C	TSSOP20 (tape and reel)	2500 parts per reel

Contents

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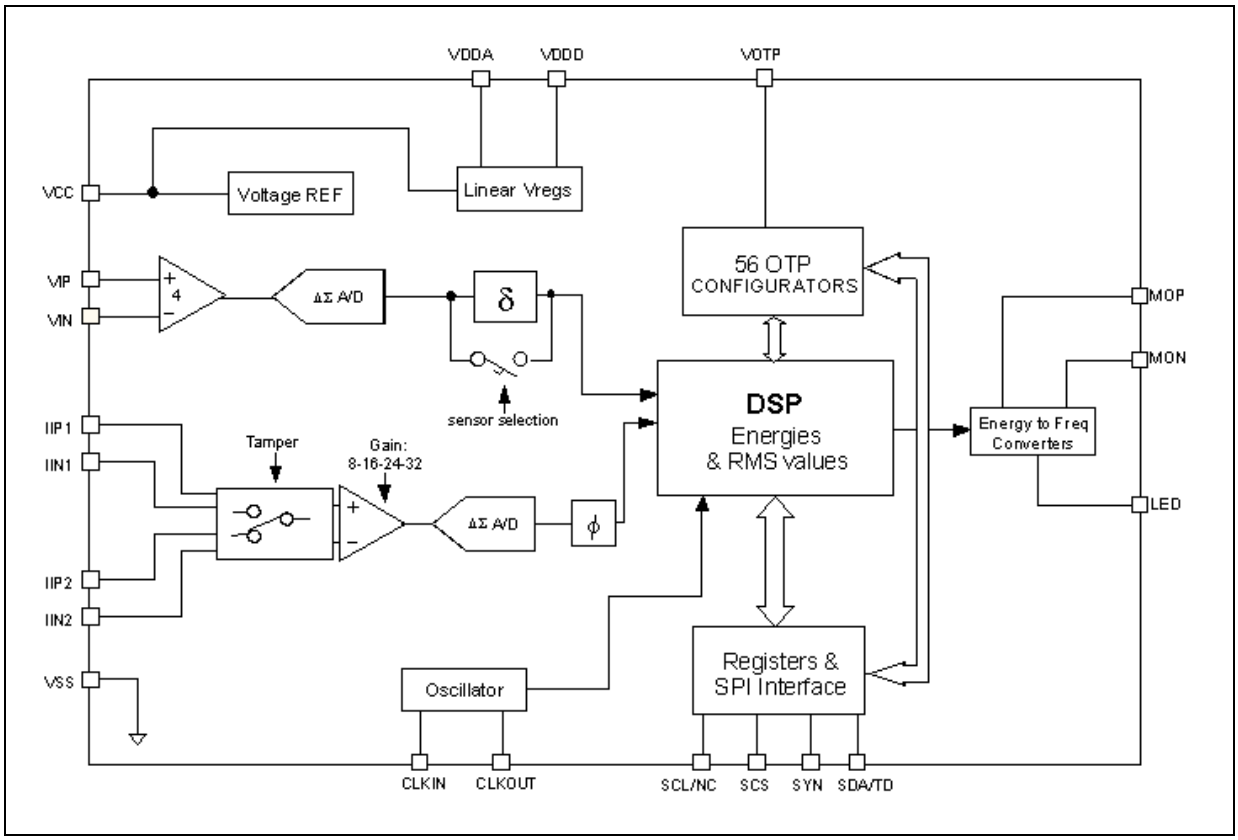
1 Schematic diagram

Figure 1. Block diagram



2 Pin configuration

Figure 2. Pin connections (top view)

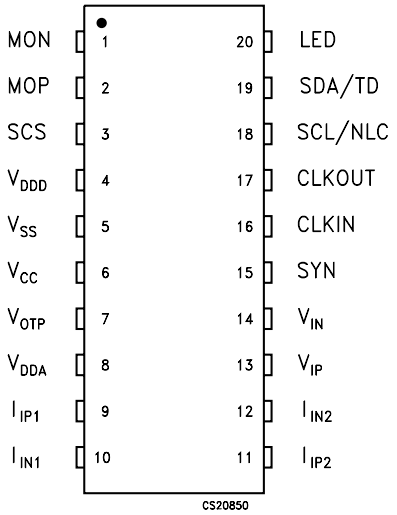


Table 2. Pin description

Pin n°	Symbol	Type (1)	Name and function
1	MON	P O	Programmable output pin, see *Table 5*
2	MOP	P O	Programmable output pin, see *Table 5*
3	SCS	D IN	Digital input/output pin, see *Table 5*
4	V_{DDD}	A OUT	1.5 V Output of internal low drop regulator which supplies the digital core
5	V_{SS}	GND	Ground
6	V_{CC}	P IN	Supply voltage
7	V_{OTP}	P INr	Supply voltage for OTP cells
8	V_{DDA}	A OUT	3 V Output of internal low drop regulator which supplies the analog part
9	I_{IP1}	A IN	Positive input of primary current channel
10	I_{IN1}	A IN	Negative input of primary current channel
11	I_{IP2}	A IN	Positive input of secondary current channel
12	I_{IN2}	A IN	Negative input of secondary current channel
13	V_{IP}	A IN	Positive input of voltage channel
14	V_{IN}	A IN	Negative input of voltage channel
15	SYN	D I/O	Programmable input/output pin, see *Table 5*
16	CLKIN	A IN	Crystal oscillator input or resistor connection if RC oscillator is selected
17	CLKOUT	A OUT	Oscillator Output (RC or crystal)
18	SCL/NLC	D I/O	Programmable input/output pin, see *Table 5*
19	SDA/TD	D I/O	Programmable input/output pin, see *Table 5*
20	LED	D O	Programmable output pin, see *Table 5*

1. A: Analog, D: Digital, P: Power

3 Maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC Input voltage	-0.3 to 6	V
I_{PIN}	Current on any pin (sink/source)	± 150	mA
V_{ID}	Input voltage at digital pins (SCS, MOP, MON, SYN, SDATD, SCLNLC, LED)	-0.3 to V_{CC} + 0.3	V
V_{IA}	Input voltage at analog pins (I_{IP1}, I_{IN1}, I_{IP2}, I_{IN2}, V_{IP}, V_{IN})	-0.7 to 0.7	V
V_{OTP}	Input voltage at OTP pin	-0.3 to 25	V
ESD	Human body model (all pins)	± 3.5	kV
T_{OP}	Operating ambient temperature	- 40 to 85	°C
T_J	Junction temperature	- 40 to 150	°C
T_{STG}	Storage temperature range	- 55 to 150	°C

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

Table 4. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction-ambient	114.5 (1)	°C/W

1. This value is referred to single-layer PCB, JEDEC standard test board.

4 Functions

Table 5. Programmable pin functions

Programmable pin	Stand-alone mode (APL register=2 or 3)	Peripheral mode (APL register=0 or 1)
MON	Output for Stepper's node (MB)	If APL=0 then Watchdog signal. If APL=1 then $\Delta\Sigma$ signal of current channel
MOP	Output for Stepper's node (MA)	If APL=0 then ZCR If APL=1 then $\Delta\Sigma$ signal of voltage channel
LED	If APL=2 then LED provides high frequency pulses proportional to Active Energy with 50% duty cycle. If APL=3 then LED provides pulses proportional to Active Energy (internal signal AW). The number of pulses per kWh can be selected according to the value of KMOT configuration bit.	If APL=0 then LED can provide Active, Reactive or Apparent Energy according to value of KMOT configuration bit. If APL=1 then LED is connected to the MUX signal generated from the tamper detection circuit. When LED=low then the primary current channel is selected, if LED=high the secondary current channel is selected.
SCLNLC	No-load indicator: when low, a no-load condition is detected	Used for SPI interface (see SPI interface section for details)
SDATD	Tamper indicator: when low tamper condition is detected	
SYN	Negative active power indicator: when low a negative active power condition is detected	
SCS	Must be high to activate SCLNLC, SDATAD and SYN indications	

Table 6. Internal signal description

Symbol	Name	Description
ZCR	Zero crossing signal	Provides positive pulse every time the line voltage crosses zero
AW	Active energy	Pulse frequency signal proportional to active energy
RW	Reactive energy	Pulse frequency signal proportional to reactive energy
SW	Apparent energy	Pulse frequency signal proportional to apparent energy
LIN	Line frequency signal	This signal is high when the voltage channel value is rising and it is low when the voltage channel is falling. Basically this signal is the sign of dv/dt.
BFR	Base frequency range	This signal is high when either the voltage line frequency is outside the nominal band or the voltage register is below 64. It is cleared when the voltage line frequency is inside the nominal band and the voltage register goes above 128.
MA	Stepper motor signals	Signal available in MOP and MON to drive a stepper motor
MB		
BIT	Tamper flag	This signal provides the information on the tamper status. If low no tamper is detected, when high a tamper condition has been detected. This signal is part of the status register but is also available on the SDATD pin when in standalone mode.
BIL	No load condition	Provides information on the load condition. This signal is part of the status register but is also available on the SCLNLC pin when in standalone mode. BIL=1 no load condition, BIL=0 normal operation.

5 Electrical characteristics

V_{CC} = 5 V, T_A = 25 °C, 100 nF to 1 uF between V_{DDA} and V_{SS}, 100 nF to 1 uF between V_{DDD} and V_{SS}, 100 nF to 1 uF between V_{CC} and V_{SS} unless otherwise specified.

Table 7. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Energy measurement accuracy						
f_{BW}	Effective bandwidth	Limited by digital filtering	5		400	Hz
e_{AW}	Accuracy of active power	Over 1 to 1000 of dynamic range		0.1		%
e_{RW}	Accuracy of reactive power	Over 1 to 1000 of dynamic range		0.1		%
e_{SW}	Accuracy of apparent power	Over 1 to 500 of dynamic range		0.1		%
SNR	Signal to noise ratio	Over the entire bandwidth		52		db
$PSRR_{DC}$	Power supply DC rejection	Voltage signal: 200 mV_{rms}/50Hz Current signal: 10 mV_{rms}/50Hz f_{CLK}= 4.194 MHz V_{CC}=3.3V±10%, 5V±10%			0.2	%
$PSRR_{AC}$	Power supply AC rejection	Voltage signal: 200 mV_{rms}/50Hz Current signal: 10 mV_{rms}/50Hz f_{CLK}= 4.194 MHz V_{CC}=3.3V+0.2V_{rms}1@100Hz V_{CC}=5.0V+0.2V_{rms}1@100Hz			0.1	%
General section						
V_{CC}	Operating supply voltage		3.165		5.5	V
I_{CC}	Supply current configuration registers cleared or device locked (TSTD=1)	4 MHz, V_{CC} = 5V		3	4	mA
		8 MHz, V_{CC} = 5V		5	6	
ΔI_{CC}	Increase of supply current per configuration bit, during programming	4 MHz, V_{CC} = 5V		120		µA/bit
	Increase of supply current per configuration bit with device locked	4 MHz, V_{CC} = 5V		2		
POR	Power on reset on V_{CC}			2.5		V
V_{DDA}	Analog supply voltage		2.85	3.0	3.15	V
V_{DDD}	Digital supply voltage		1.425	1.50	1.575	V
f_{CLK}	Oscillator clock frequency	MDIV bit = 0	4.000		4.194	MHz
		MDIV bit = 1	8.000		8.192	MHz
f_{LINE}	Nominal line frequency		45		65	Hz
V_{OTP}	OTP programming voltage		14		20	V

Table 7. Electrical characteristics (continued)

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
I_{OTP}	OTP programming current per bit				2.5		mA
t_{OTP}	OTP programming time per bit			100		300	µs
I_{LATCH}	Current injection latch-up immunity					300	mA
Analog Inputs (I_{IP1}, I_{IN1}, I_{IP2}, I_{IN2}, V_{IP}, V_{IN})							
V_{MAX}	Maximum input signal levels	Voltage channel		-0.3		0.3	V
		Current channels	Gain 8X	-0.15		0.15	V
			Gain 16X	-0.075		0.075	
			Gain 24X	-0.05		0.05	
			Gain 32X	-0.035		0.035	
f_{ADC}	A/D Converter bandwidth				10		kHz
f_{SPL}	A/D Sampling frequency				$F_{CLK}/4$		Hz
V_{OFF}	Amplifier offset					±20	mV
Z_{IP}	V_{IP}, V_{IN} Impedance	Over the total operating voltage range		100		400	kΩ
Z_{IN}	V_{IP1}, V_{IN1}, V_{IP2}, V_{IN2} Impedance	Over the total operating voltage range			100		kΩ
G_{ERR}	Current channels gain error				±10		%
I_{VL}	Voltage channel leakage current			-1		1	µA
I_{LEAK}	Current channel leakage current	Channel disabled (PST=0 to 3; CH2 disabled if C_{SEL}=0; CH1 disabled if C_{SEL}=1) or device off		-1		1	µA
		Input enabled		-10		10	
Digital I/O Characteristics (SDA, CLKIN, CLKOUT, SCS, SYN, LED)							
V_{IH}	Input high voltage	SDA, SCS, SYN, LED		$0.75V_{CC}$			V
		CLKIN		1.5			
V_{IL}	Input low voltage	SDA, SCS, SYN, LED				$0.25V_{CC}$	V
		CLKIN				0.8	
V_{OH}	Output high voltage	I_O = -2mA		V_{CC}-0.4			V
V_{OL}	Output low voltage	I_O = +2mA				0.4	V
I_{UP}	Pull up current				15		µA
t_{TR}	Transition time	C_{LOAD} = 50pF			10		ns
Power I/O Characteristics (MOP, MON)							
V_{OH}	Output high voltage	I_O = -14mA		V_{CC}-0.5			V
V_{OL}	Output low voltage	I_O = +14mA				0.5	V
t_{TR}	Transition time	C_{LOAD} = 50pF		5	10		ns

Table 7. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Crystal oscillator (see circuit *Figure 20*)						
I_I	Input current on CLKIN				1	µA
R_P	External resistor		1		4	MΩ
C_P	External capacitors			22		pF
f_{CLK}	Nominal output frequency		4	4.194		MHz
			8	8.192		
RC oscillator (see circuit *Figure 20*)						
I_{CLKIN}	Settling current	f_{CLK}= 4 MHz	40		60	µA
R_{SET}	Settling resistor			12		kΩ
t_{JIT}	Frequency jitter			1		ns
On chip reference voltage						
V_{REF}	Reference voltage			1.23		V
	Reference accuracy			±1		%
T_C	Temperature coefficient	After calibration		30	50	ppm/ °C
SPI interface timing						
F_{SCLKr}	Data read speed				32	MHz
F_{SCLKw}	Data write speed				100	kHz
t_{DS}	Data setup time		20			ns
t_{DH}	Data hold time		0			ns
t_{ON}	Data driver on time				20	ns
t_{OFF}	Data driver off time				20	ns
t_{SYN}	SYN active width		$2/f_{CLK}$			s

6 Terminology

6.1 Measurement error

The error associated with the energy measurement made by the STPM01 is defined as:

Percentage error = [STPM01 (reading) - true energy] / true energy

6.2 ADC offset error

This is the error due to the DC component associated with the analog inputs of the A/D converters. Due to the internal automatic DC offset cancellation the STPM01 measurement is not affected by DC components in voltage and current channel. The DC offset cancellation is implemented in the DSP.

6.3 Gain error

The gain error is gain due to the signal channel gain amplifiers. This is the difference between the measured ADC code and the ideal output code. The difference is expressed as percentage of the ideal code.

6.4 Power supply DC and AC rejection

This parameter quantifies the STPM01 measurement error as a percentage of reading when the power supplies are varied. For the PSRRAC measurement, a reading at two nominal supplies voltages (3.3 and 5 V) is taken. A second reading is obtained with the same input signal levels when an ac (200 mV_{RMS}/100 Hz) signal is introduced onto the supplies. Any error introduced by this ac signal is expressed as a percentage of reading.

For the PSRRDC measurement, a reading at two nominal supplies voltages (3.3 and 5V) is taken. A second reading is obtained with the same input signal levels when the supplies are varied ± 10 %. Any error introduced is again expressed as a percentage of the reading.

6.5 Conventions

The lowest analog and digital power supply voltage is named V_{SS} which represent the system ground (GND). All voltage specifications for digital input/output pins are referred to GND.

Positive currents flow into a pin. Sinking current means that the current is flowing into the pin and then it is positive. Sourcing current means that the current is flowing out of the pin and then it is negative.

Timing specifications of signal treated by a digital control part are relative to CLKOUT. This signal is provided from the crystal oscillator of 4.194 MHz nominal frequency or from the internal RC oscillator, eventually an external source of 4.194 MHz or 8.192 MHz can be used.

Timing specifications of signals of the SPI interface are relative to the SCLNLC, there is no direct relationship between the clock (SCLNLC) of the SPI interface and the clock of the DSP block. A positive logic convention is used in all equations.

7 Typical performance characteristics

Figure 3. Supply current vs. supply voltage, T_A = 25 °C

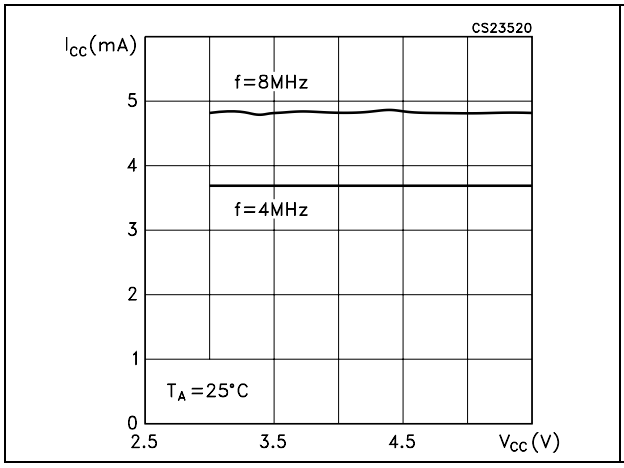


Figure 4. RC oscillator frequency vs. V_{CC}, R = 12 kΩ, T_A = 25 °C

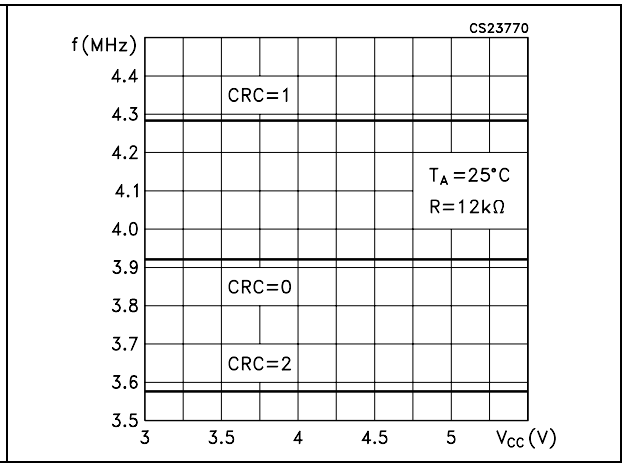


Figure 5. RC oscillator: frequency jitter vs. temperature

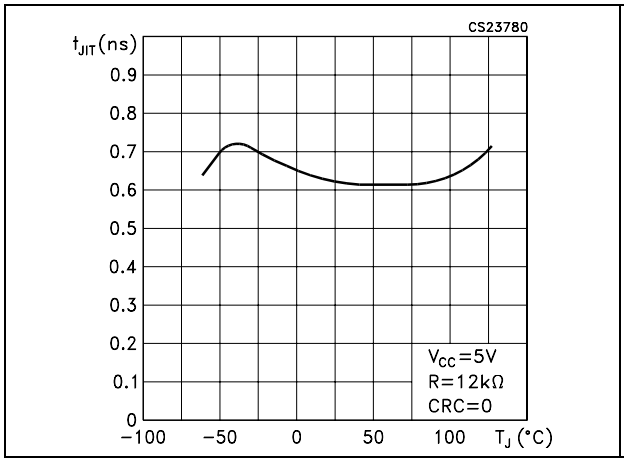


Figure 6. Analog voltage regulator: line - load regulation

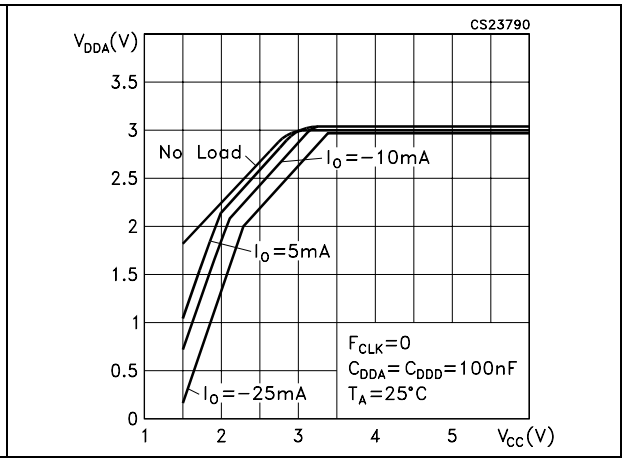


Figure 7. Digital voltage regulator: line - load regulation

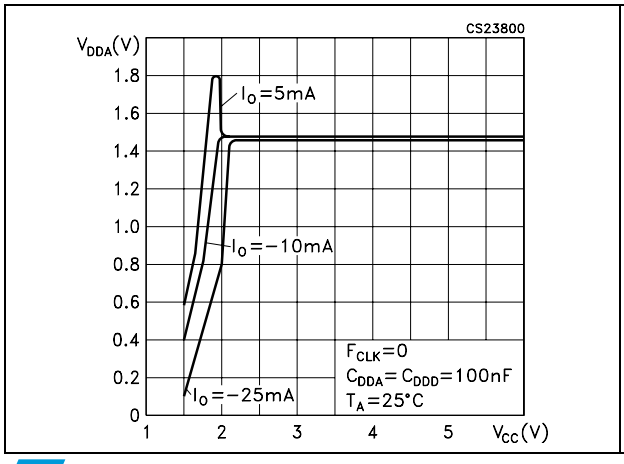


Figure 8. Voltage channel linearity at different V_{CC} voltages

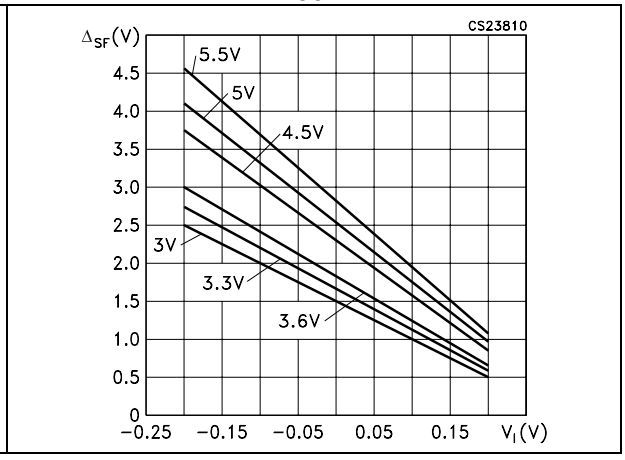


Figure 9. Power supply AC rejection vs. V_{CC}

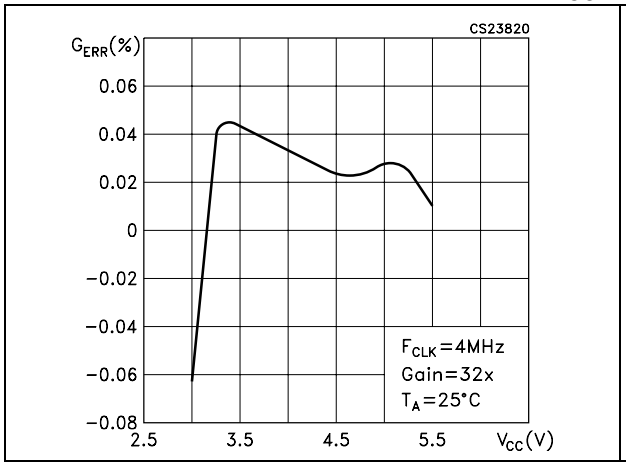


Figure 10. Power supply DC rejection vs. V_{CC}

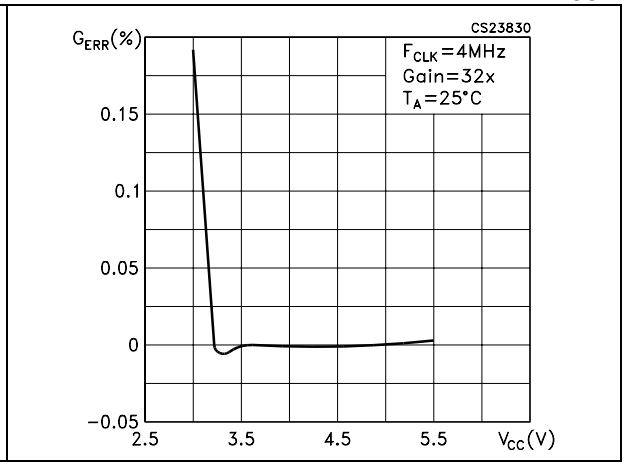


Figure 11. Error over dynamic range gain dependence

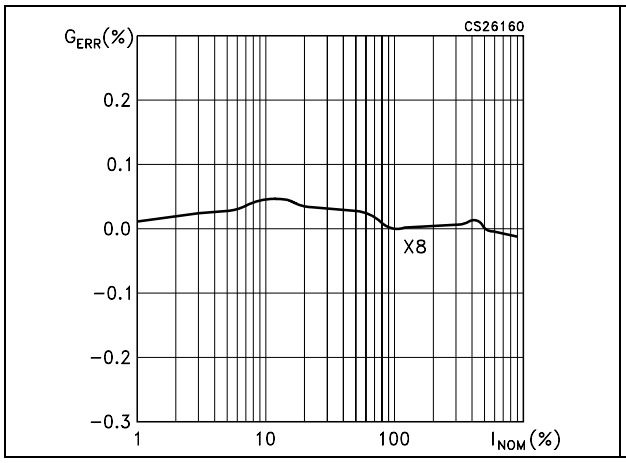


Figure 12. Primary current channel linearity at different V_{CC}

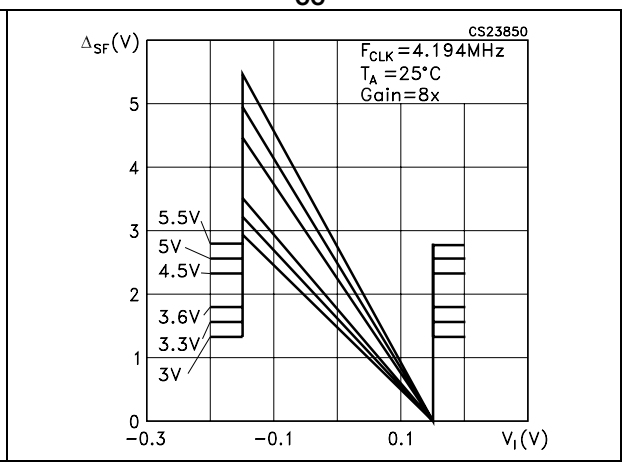
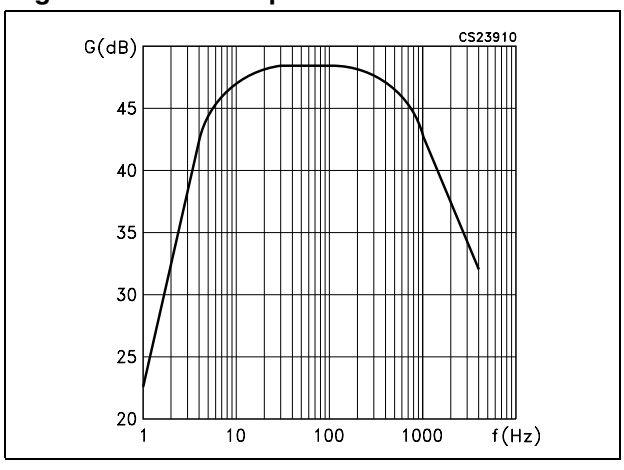


Figure 13. Gain response of ΔΣ AD converters



8 Theory of operation

8.1 General operation description

The STPM01 is able to perform active, reactive and apparent energy measurements, RMS and instantaneous values for voltage and current, line frequency information.

Most of the functions are fully programmable using internal configuration bits accessible through SPI interface. The most important configuration bits are the two application bits (APL - see *Table 16* for configuration register). Using these bits the STPM01 can be programmed as peripheral (APL = 0 or APL = 1) in microcontroller based meter systems or as standalone meter device (APL = 2 or APL = 3).

In standalone mode, the STPM01 is able to drive a stepper motor with the MOP and MON pins, while some of the SPI pins (see *Table 5*) are used to provide information on tamper, no load and negative power.

In peripheral mode, due to the fact that the stepper motor is not used, the MOP and MON pins are used to provide different information (see *Table 5*), while the SPI pins are used to communicate with the microcontroller.

The STPM01 includes internal registers that hold the useful information for the meter system. Two kinds of active energy are available: the total active energy that includes all harmonic content called type 0 and the active energy limited to the 1st harmonic called type 1. This last energy value is obtained filtering the type 0 active energy. The resolution of both the two active energies is 20-bit. Reactive and Apparent energies are also available with a 20-bit resolution.

STPM01 provides also the RMS values of voltage and current. Due to the modest dynamic variation of the voltage, the RMS value is stored with a resolution of 11 bit. While the RMS current value has a resolution of 16 bit. The momentary sampled value of voltage and current are available also with a resolution of 11 and 16 bit respectively. The line frequency value is stored with a resolution of 14 bits.

Due to the proprietary energy computation algorithm, STPM01 calibration is very easy and fast allowing calibration in only one point over the whole current range. The calibration parameters are stored permanently in the OTP (one time programmable) cells, preventing calibration tampering.

8.2 Analog inputs

Input amplifiers

The STPM01 has one fully differential voltage input channel and two fully differential current input channels.

The voltage channel consists of a differential amplifier with a gain of 4. The maximum differential input voltage for the voltage channel is ± 0.3 V.

The two current channels are multiplexed (see tamper section for details) to provide a single input to a preamplifier with a gain of 4. The output of this preamplifier is connected to the input of a programmable gain amplifier (PGA) with possible gain selections of 2, 4, 6, 8. The total gain of the current channels are then 8, 16, 24, 32. The gain selections are made by writing to the gain register and it can be different for the two current channels. In case the tamper function is not used, the secondary current can be disabled.

The maximum differential input voltage is dependent on the selected gain according to the following table.

Table 8. Gain of voltage and current channels

Voltage channels		Current channels	
Gain	**Max Input voltage (V)**	**Gain**	**Max input voltage (V)**
4	±0.30	8X	±0.15
		16X	±0.075
		24X	±0.05
		32X	±0.035

The gain register is included in the device configuration register with the address names PST and ADDG. The table below shows the gain configuration according to the register values:

Table 9. Configuration of current sensors

Primary		Secondary		Configuration Bits	
Gain	**Sensor**	**Gain**	**Sensor**	**PST (3 bits)**	**ADDG (1 bit)**
8	Rogowsky Coil	Disabled (No Tamper)		0	0
16				0	1
24				1	0
32				1	1
8	CT			2	X
32	Shunt			3	X
8	Rogowsky Coil	8	Rogowsky Coil	4	0
16		16		4	1
24		24		5	0
32		32		5	1
8	CT	8	CT	6	X
8		32	Shunt	7	X

Note: If the device is used in configuration PST = 7 (primary channel with CT, secondary channel with Shunt), the shunt Ks must always be equal to one fourth of the current transformer Ks.

Both the voltage and current channels implement an active offset correction architecture which gives the benefit to avoid any offset compensation.

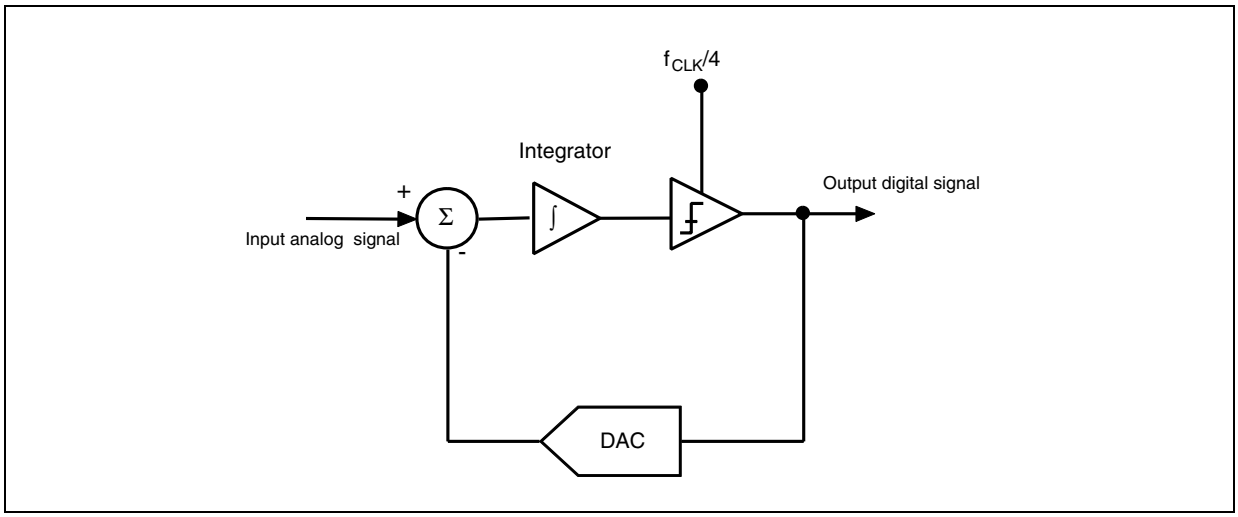
The analog voltage and current signals are processed by the $\sum \Delta$ Analog to digital converters that feed the hardwired DSP. The DSP implements an automatic digital offset cancellation that make possible avoiding any manual offset calibration on the analog inputs.

8.3 ∑Δ A/D converters

The analog to digital conversion in the STPM01 is carried out using two first order ∑ Δ converters. The device performs A/D conversions of analog signals on two independent channels in parallel. The current channel is multiplexed as primary or secondary current channel in order to be able to perform a tamper function, if it is enabled. The converted ∑ Δ signals are supplied to the internal hardwired DSP unit, which filters and integrates those signals in order to boost the resolution and to yield all the necessary signals for computations.

A ∑ Δ modulator converts the input signal into a continuous serial stream of 1 s and 0 s at a rate determined by the sampling clock. In the STPM01, the sampling clock is equal to $f_{CLK/4}$. The 1-bit DAC in the feedback loop is driven by the serial data stream. The DAC output is subtracted from the input signal. If the loop gain is high enough, the average value of the DAC output (and therefore the bit stream) can approach that of the input signal level. When a large number of samples are averaged a very precise value of the analog signal is obtained. This averaging is carried out in the DSP section which implements decimation, integration and DC offset cancellation of the supplied ∑ Δ signals. The gain of the decimation filters is 1.004 for the voltage channel and 0.502 for the current channel. The resulting signal has a resolution of 11bits for voltage channel and 16 bits for current channel.

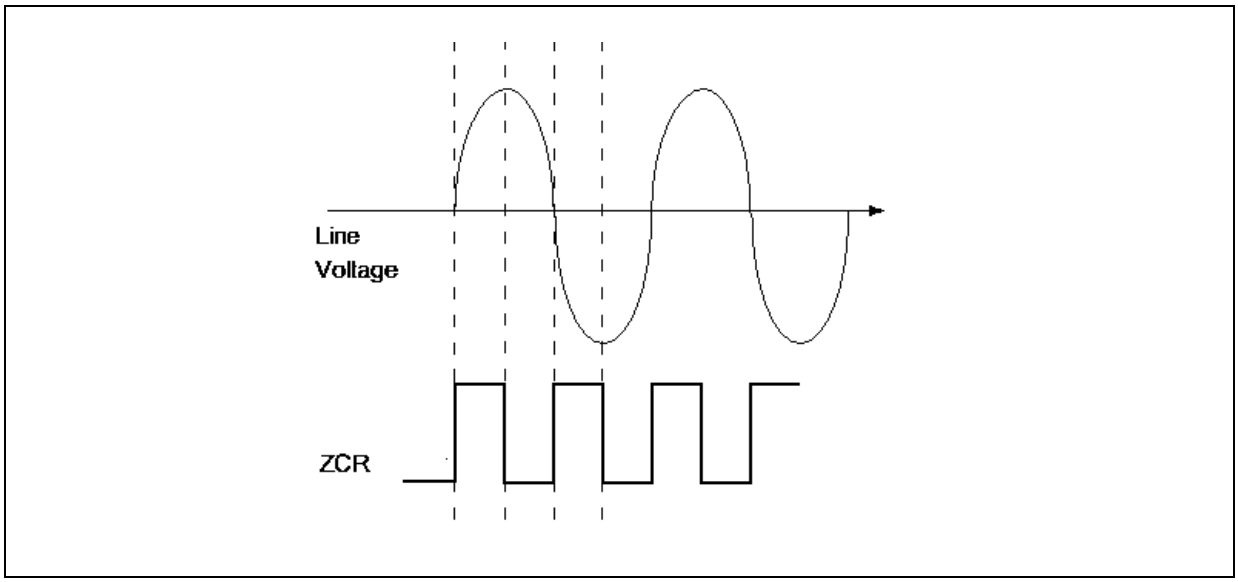
Figure 14. First order ∑ Δ A/D converter



8.4 Zero crossing detection

The STPM01 has a zero crossing detector circuit on the voltage channel which can be used by application for synchronization of some utility equipment to event of zero crossing of line voltage. This circuit produces the internal signal ZCR which has a rising edge every time the line voltage crosses zero and a negative edge every time the voltage reaches its positive or negative peak. The ZCR signal is then at twice the line voltage frequency. The ZCR signal is available on the MOP pin only when STPM01 works as peripheral with the configuration bit APL = 0.

Figure 15. ZCR signal



8.5 Period and line voltage measurement

The period module measures the period of the base frequency of the voltage channel and checks if the voltage signal frequency is within the $f_{CLK}/2^{17}$ to $f_{CLK}/2^{15}$ band. To do this, the LIN signal is produced, which is low when the line voltage is rising, and high when the line voltage is falling. This means that the LIN signal is the sign of dv/dt. With further elaboration, the ZCR signal is also produced. On the trailing edge of LIN (line frequency) the period counter starts counting up pulses of the f_{CLK} /4 reference signal. The LIN signal is available on the status bit register (see *Table 15*).

If the counted number of pulses between two trailing edges of LIN is higher than 2^{15}, or if the counting is never stopped (no LIN trailing edge) this means that the base frequency is lower than $f_{CLK}/2^{17}$ Hz and a BFR (base frequency range) error flag is set.

If the number of pulses counted between two trailing edges of LIN is lower than 2^{13}, the base frequency exceeds the limit (means it is higher than $f_{CLK}/2^{15}$. In this case, the error must be repeated three consecutive times in order to set the BFR error flag.

For example, with a 4.194304 MHz oscillator frequency and MDIV bit clear (or 8.192 MHz with MDIV set), $f_{CLK}/4$ is 1048.576 MHz. If the line frequency is 30 Hz, the counted $f_{CLK}/4$ pulses between two LIN trailing edges are 34952, more than 2^{15} (32768 pulses). The BFR low frequency limit is then:

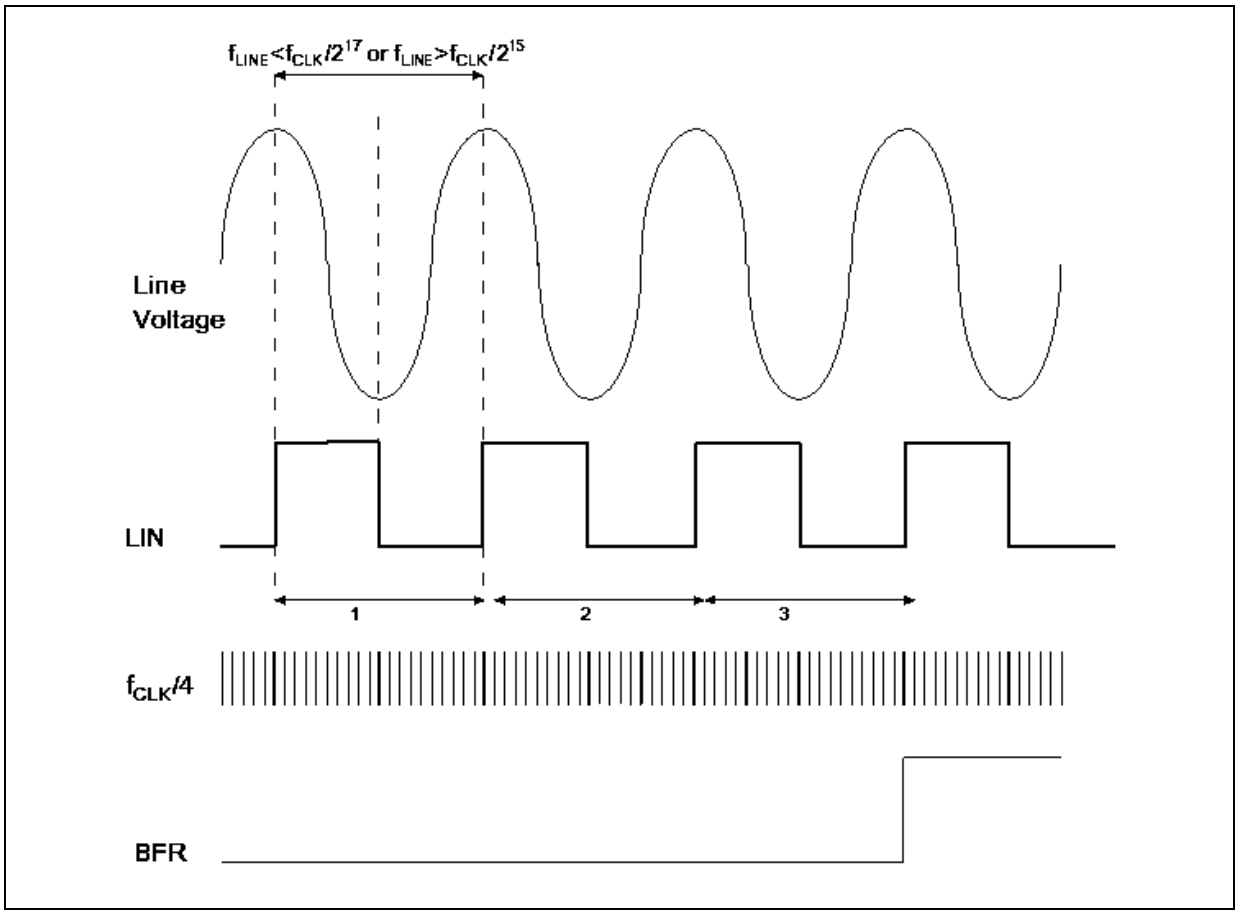
$f_{CLK}/2^{17}$ = 4194304/131072 = 32 Hz.

With the same clock frequency, if the line frequency is 130Hz, the $f_{CLK}/4$ pulses between two LIN trailing edges are 8066, more than 2^{13} (8192). The BFR high frequency limit is then:

$f_{CLK}/2^{15}$ = 4194304/32768 = 128 Hz.

When the line frequency re-enters the nominal band, the BFR flag is automatically reset. This BFR error flag is also assembled as part of the 8-bit status register (see *Table 15*).

Figure 16. LIN and BFR signal



The BFR flag is also set if the register value of the RMS voltage drops below 64. BFR is cleared when the register value goes above 128. The BFR, then, also gives information about the presence of the line voltage within the meter.

When the BFR error is set, the computation of power is zero unless the FRS bit is set or the single wire mode operation is selected (see *Section 8.6*).

In fact, the effect of the BFR bit can be overridden by setting FRS configuration bit.

It means that if FRS is set and BFR is also set, all the energy computation is carried on as BFR was cleared. In this case then p=u*i, where u could be zero or not (if BFR was set because voltage RMS register value is below 64).

In standalone mode, the MOP, MON and LED provide the energy information, their operation is not affected by FRS bit, it means that when BFR is set they stop switching regardless the FRS value.

8.6 Single wire meter mode (only Rogowsky coil sensor)

STPM01 support single wire meter (SWM) operation when working with Rogowsky coil current sensors. In SWM mode there is no available voltage information in the voltage channel. It is possible that someone has disconnected one wire (live or neutral) of the meter

for tampering purposes or in case the line voltage is very stable, it is possible to use a predefined value for computing the energy without sensing it.

In order to enable the SWM mode, the STPM01 must be configured with PST values of 4 or 5, (tamper enabled-Rogowsky coils). In this way, if the BFR error is detected, STPM01 enters in SWM. If BFR is cleared the energy calculation is performed normally, when BFR is set (no voltage information is available) the energy computation is carried out using a nominal voltage value according to the NOM configuration bits.

Since there is no more information on the phase shift between voltage and current, the apparent rather than active power is used for tamper and energy computation. The calculated apparent energy is the product between I_{RMS} (effectively measured) and an equivalent V_{RMS} that can be calculated as follows:

$V_{RMS} = V_{PK}{}^{*}K_{NOM}$,

where V_{PK} represents the maximum line voltage reading of the STPM01 and K_{NOM} is a coefficient that changes according to the following table:

Table 10. Nominal voltage values

NOM	K_{NOM}
0	0.3594
1	0.3906
2	0.4219
3	0.4531

For example, if a R_1 = 783 kΩ and R_2 = 475 Ω are used as resistor divider when the line voltage is present, the positive voltage present at the input of the voltage channel of STPM01 is:

$$VI = \frac{R_2}{R_1 + R_2} \cdot V_{RMS}\sqrt{2}$$

since the maximum voltage value applicable to the voltage channel input of STPM01 is +0.3 V, the equivalent maximum line voltage applicable is:

$V_{PK} = R_1{+}R_2/R_2 \bullet 0.3 = 494.82$

considering the case of NOM=2, the correspondent RMS values used for energy computation are:

$V_{RMS} = V_{PK} \bullet 0.4219 = 208.76$ [V]

Usually the supply voltage for the electronic meter is taken from the line voltage, in SWM, since the line voltage is not present any more, some other power source must be used in order to provide the necessary supply to STPM01 and the other electronic components of the meter.

8.7 Power supply

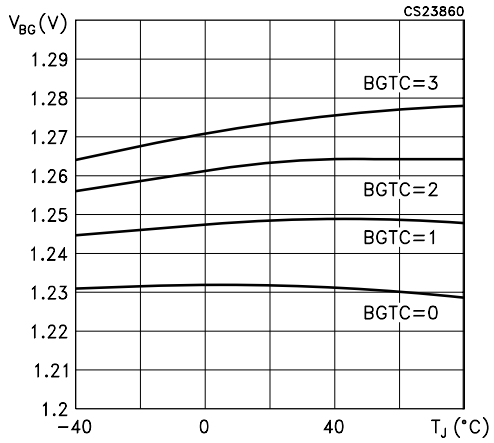
The main STPM01 supply pin is the V_{CC} pin. From the V_{CC} pin two linear regulators provide the necessary voltage for the analog part V_{DDA} (3 V) and for the digital part V_{DDD} (1.5 V). The V_{SS} pin represents the reference point for all the internal signals. 100 nF low ESR

capacitor should be connected between V_{CC} and V_{SS}, V_{DDA} and V_{SS}, V_{DDD} and V_{SS}. All these capacitors must be located very close to the device.

The STPM01 contains a power on reset (POR) detection circuit. If the V_{CC} supply is less than 2.5 V then the STPM01 goes into an inactive state, all the functions are blocked asserting a reset condition. This is useful to ensure correct device operation at power-up and during power-down. The power supply monitor has built-in hysteresis and filtering, which give a high degree of immunity to false triggering due to noisy supplies.

A bandgap voltage reference (VBG) of 1.23 V ±1 % is used as reference voltage level source for the two linear regulators and for the A/D converters. Also, this module produces several bias currents and voltages for all other analog modules and for the OTP module. The bandgap voltage can be compensated regardless to the temperature variations with the BGTC bits.

Figure 17. Bandgap temperature variation



8.8 Load monitoring

The STPM01 includes a no load condition detection circuit with adjustable threshold. This circuit monitors the voltage and the current channels and, when the measured voltage is below the set threshold, the internal signal BIL becomes high. The information about this signal is also available in the status bit BIL.

The no load condition occurs when the product between V_{RMS} and I_{RMS} register values is below a given value. This value can be set with the LTCH configuration bits.

Four different no-load threshold values can be chosen according to the two configuration bits LTCH (see *Table 11*).

Table 11. No load detection thresholds

LTCH	K_{LTCH}
0	800
1	1600
2	3200
3	6400

When a no load condition occurs (BIL=1) the integration of power is suspended and the tamper module is disabled.

In standalone mode, if a no load condition is detected, the BIL signal blocks generation of pulses for stepper and forces SCLNLC pin to be low. If APL = 2 (see *Section 8.14*) the LED pin continues providing the high frequency pulses, while if APL = 3, the pulses are stopped as happens for MOP and MON.

In peripheral mode, the BIL signal can be accessed only through the SPI interface.

8.9 Error detection

In addition to the no load condition and the line frequency band, the integration of power can be suspended also due to detected error on the source signals.

There are two kinds of error detection circuits involved. The first checks all the $\sum \Delta$ signals from the analog part if any is stacked at 1 or 0 within the 1/128 of f_{CLK} period of observation. In case of detected error the corresponding $\sum \Delta$ signal is replaced with an idle $\sum \Delta$ signal, which represents a constant value 0. All error and other resolved flags are treated as bits of a device status and can be read out by means of SPI interface.

Another error condition occurs if the MOP, MON and LED pin outputs signals are different from the internal signals that drive them. This can occur if some of this pin is forced to GND or to some other imposed voltage value. In this case the internal status bit PIN is activated providing the information that some hardware problem has been detected, for example the stepper motor has been mechanically blocked.

8.10 Tamper detection module

The STPM01 is able to measure the current in both live and neutral wire with a time domain multiplexing approach on a unique sigma delta modulator. This mechanism is adopted to implement anti-tamper function. If this function is selected (see *Table 9*), the live and neutral wire currents are monitored; when the difference between the two measurements exceeds a rated threshold the STPM01 enters the "tamper state", while in "normal state" the two measurements are below the threshold.

In particular, both channels are not observed all the time, rather a time multiplex mechanism is used. During the observation time of each channel, its active energy is calculated. A tamper condition occurs when the absolute value of the difference between the two active energy values is greater than a certain percentage of the averaged energy during the activated tamper module (see *Equation 1:*).

This percentage value can be selected between two different values (12.5 % and 6.25 %) according to the value of the configuration bit CRIT.

The tamper condition is detected when the following formula is satisfied:

Equation 1

$$EnergyCH1 - EnergyCH2 > K_{CRIT} (EnergyCH1 + EnergyCH2)/2;$$

where K_{CRIT} can be 12.5 % or 6.25 %.

The detection threshold is much higher than the accuracy difference of the current channels, which should be less than 0.2 %, but, some headroom should be left for possible transition effect, due to accidental synchronism of actual load current change with the rhythm of taking the energy samples.

The tamper circuit works if the energies associated with the two current channels are both positive or negative, if the two energies have different sign, the tamper is on all the time however, the channel with the associated higher power is selected for the final computation of energy.

In single wire mode, the apparent energy rather than the active is used for tamper detection.

When internal signals are not good enough to perform the calculations, i.e. line period is out or range or $\Delta\Sigma$ signals from analog section are stacked at high or low logic level, or no load condition is activated, the tamper module is disabled and its state is preset to normal.

8.10.1 Detailed operational description

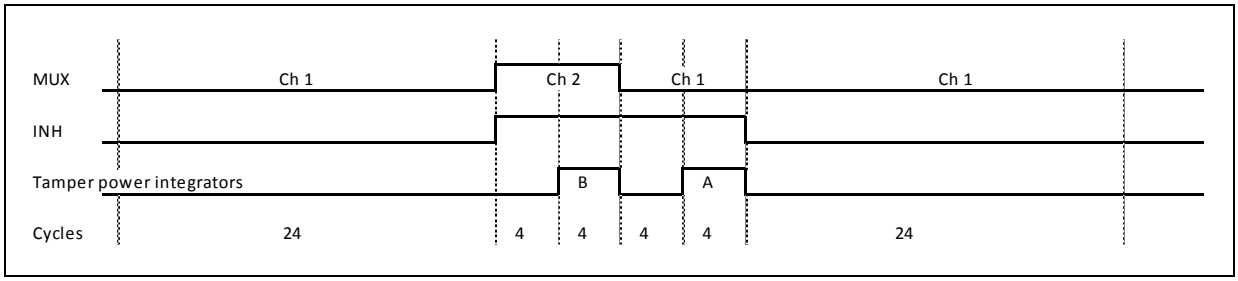
The meter is initially set to normal state, i.e. tamper not detected.In this condition the primary channel is selected for final integration of energy. In such state the values of both load currents should not differ more than the accuracy difference of the channels does. Sixty-four periods of line voltage is used as a tamper checking period.

After 24 periods of line voltage two internal signals MUX and INH are changed in order to enable secondary current channel and to freeze the last power and RMS values of primary current channel. The following 16 periods of line frequency are used for tamper detection integration. During this gap, the final energy calculation does not use the signal from selected channel but the frozen values.

Four line periods after the INH switch, the integration of power from secondary current channel is started and lasts four periods. Additional four line periods later MUX signal is switched back to primary current channel and the integration for tamper detection is started.

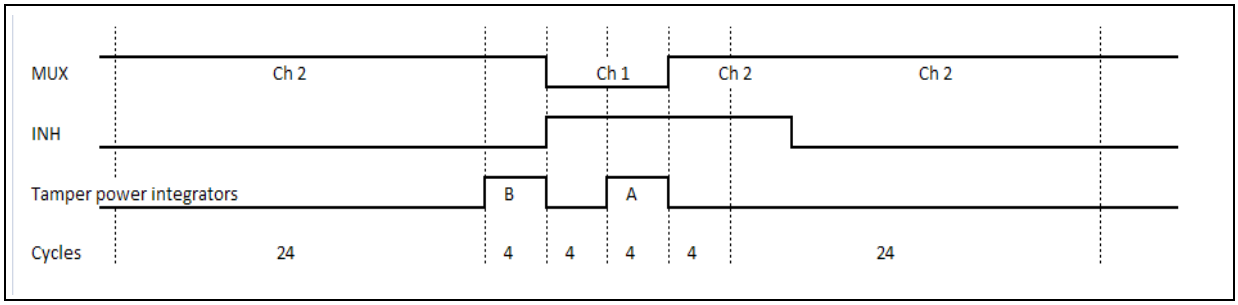
The timings of MUX and INH signals are shown in *Figure 18* below.

Figure 18. Timings of tamper module - Primary channel selected



When the secondary channel is selected to be integrated by the final energy integrator, the MUX and INH signals change according to *Figure 19* below.

Figure 19. Timings of tamper module - Secondary channel selected



This means that energy of four periods from secondary channel followed by energy of four periods from primary channel is sampled within the tamper module. From these two