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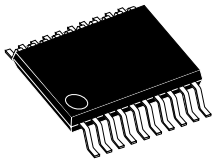
STPM10

Programmable single-phase energy metering IC with tamper detection

Datasheet - production data



TSSOP20

Features

- Measures active, reactive, and apparent energies
- Current, voltage RMS and instantaneous measurement
- Frequency measurement
- Ripple-free active energy pulsed output
- Live and neutral monitoring for tamper detection
- Fast and simple one-point digital calibration over the whole current range
- Integrated linear voltage regulators for digital and analog supply
- Selectable RC or crystal oscillator
- Supports 50 - 60 Hz - IEC62052-11, IEC62053- 2x specifications
- Less than 0.1% error in the 1000:1 range
- Precision voltage reference: 1.23 V with 30 ppm/°C max.

Description

The STPM10 is designed for effective measurement of active, reactive and apparent energy in a power line system using current transformer and shunt sensors. The device can be implemented for peripheral measurement in a microcontroller-based single-phase or poly-phase energy meter. The STPM10 consists of two main sections: analog and digital. The analog part is composed of preamplifier and first-order sigma-delta A/D converter blocks, a band-gap voltage reference and low-drop voltage regulator. The digital part is composed of system control, oscillator, hard-wired DSP and SPI interface. There is also an internal volatile memory, which is controlled through the SPI by means of a dedicated command set. The configured bits are used for configuration and calibration purposes. From a pair of sigma-delta output signals produced by the analog section, the DSP unit computes the amount of active, reactive and apparent energy consumed, as well as the RMS and instantaneous voltage and current values. The results of the computation are available as pulse frequencies and states on the digital outputs of the device, or as data bits in a data stream, which can be read from the device by means of the SPI interface. The system bus interface is also used for temporary programming of bits of internal volatile memory. The STPM10 generates an output signal with a pulse frequency proportional to the energy, and this signal is used in the calibration phase of the energy metering application.

Table 1: Device summary

Oder code	Temperature range	Package	Packing
STPM10BTR	- 40 to 85 °C	TSSOP20 (tape and reel)	2500 pieces per reel

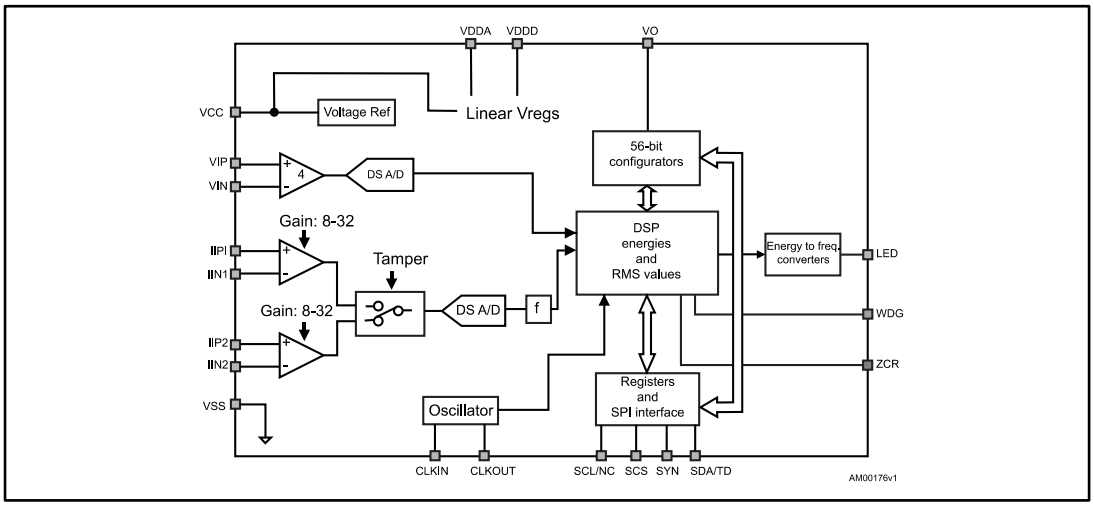
Contents

List of tables

List of figures

1 Schematic diagram

Figure 1: Block diagram



2 Pin configuration

Figure 2: Pin connections (top view)

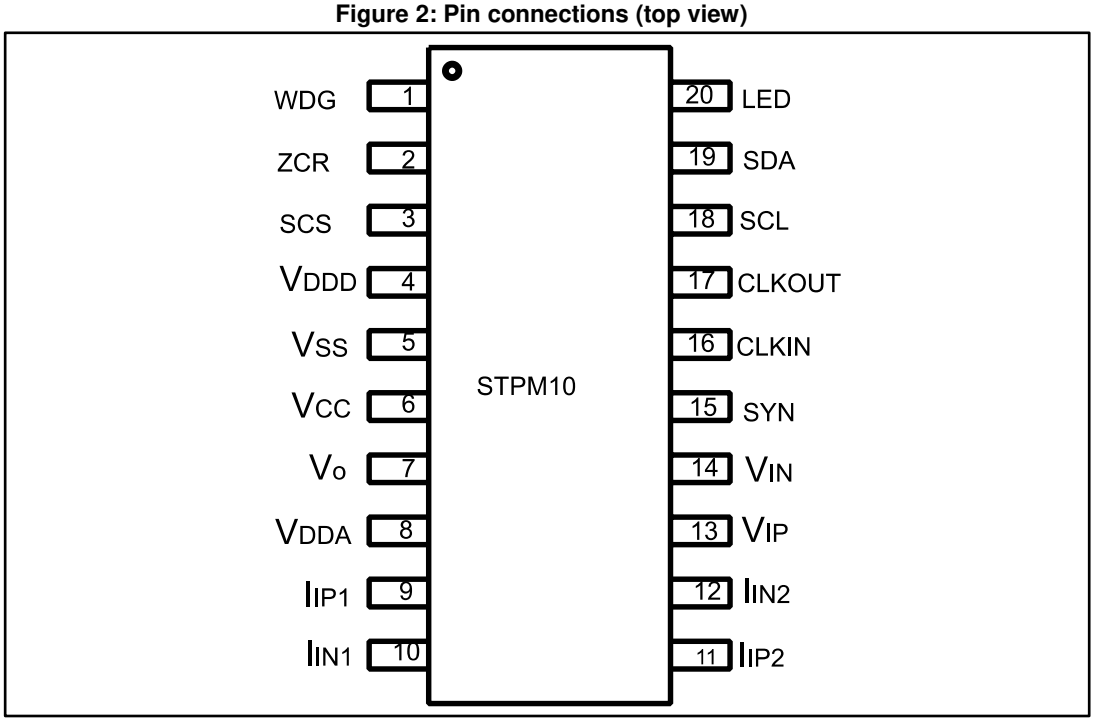


Table 2: Pin description

Pin	Symbol	Type(1)	Description
1	WDG	D O	Watchdog
2	ZCR	D O	Zero-crossing signal
3	SCS	D IN	SPI interface enable pin
4	V_{DDD}	A OUT	1.8 V output of internal low drop regulator which supplies the digital core
5	V_{SS}	GND	Ground
6	V_{CC}	P IN	Supply voltage
7	V_O	P OUT	Output of internal low drop regulator
8	V_{DDA}	A OUT	3 V output of internal low drop regulator which supplies the analog part
9	I_{IP1}	A IN	Positive input of primary current channel
10	I_{IN1}	A IN	Negative input of primary current channel
11	I_{IP2}	A IN	Positive input of secondary current channel
12	I_{IN2}	A IN	Negative input of secondary current channel
13	V_{IP}	A IN	Positive input of voltage channel
14	V_{IN}	A IN	Negative input of voltage channel
15	SYN	D I/O	SPI interface pin
16	CLKIN	A IN	Crystal oscillator input
17	CKOUT	A OUT	Crystal oscillator output

Pin	Symbol	Type(1)	Description
18	SCL	D I/O	SPI interface clock pin
19	SDA	D I/O	SPI interface data pin
20	LED	D O	Active energy pulsed output

Notes:

(1)A: analog, D: digital, P: power.

3 Electrical ratings

Table 3: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC input voltage	-0.3 to 6	V
I_{PIN}	Current on any pin (sink/source)	± 150	mA
V_{ID}	Input voltage at digital pins (SCS, ZCR, WDG, SYN, SDA, SCL, LED)	-0.3 to V_{CC} + 0.3	V
V_{IA}	Input voltage at analog pins (I_{IP1}, I_{IN1}, I_{IP2}, I_{IN2}, V_{IP}, V_{IN})	-0.7 to 0.7	V
ESD	Human body model (all pins)	±3.5	kV
T_{OP}	Operating ambient temperature	-40 to 85	C
T_J	Junction temperature	-40 to 150	°C
T_{STG}	Storage temperature range	-55 to 150	°C

Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

Table 4: Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction-to-ambient	114.5(1)	°C/W

Notes:

(1)This value is based on a single-layer PCB, JEDEC standard test board.

4 Electrical characteristics

V_{CC} = 5 V, T_A = 25 °C, 100 nF to 1 µF between V_{DDA} and V_{SS}, 100 nF to 1 µF between V_{DDD} and V_{SS}, 100 nF to 1 µF between V_{CC} and V_{SS} unless otherwise specified.

Table 5: Absolute maximum ratings

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Energy measurement accuracy						
f_{BW}	Effective bandwidth	Limited by digital filtering (-3 dB)	4		800	Hz
e_{AW}	Accuracy of active power	Over 1 to 1000 of dynamic range		0.1		%
e_{RW}	Accuracy of reactive power	Over 1 to 1000 of dynamic range		0.1		%
e_{SW}	Accuracy of apparent power	Over 1 to 500 of dynamic range		0.1		%
SNR	Signal-to-noise ratio	Over the entire bandwidth		52		db
$PSRR_{DC}$	Power supply DC rejection	Voltage signal: 200 mV_{rms}/50 Hz Current signal: 10 mVrms/50 Hz f_{CLK}= 4.194 MHz V_{CC}=3.3 V ±10%, 5 V±10%			0.2	%
$PSRR_{AC}$	Power supply AC rejection	Voltage signal: 200 mV_{rms}/50 Hz Current signal: 10 mVrms/50 Hz f_{CLK}= 4.194 MHz V_{CC} = 3.3 V+0.2 V_{rms}1@100 Hz V_{CC} = 5.0 V+0.2 V_{rms}1@100 Hz			0.1	%
General section						
V_{CC}	Operating supply voltage		3.165		5.5	V
I_{CC}	Supply current Configuration registers cleared	4 MHz, V_{CC} = 5 V		3	4	mA
		8 MHz, V_{CC} = 5 V		5	6	
POR	Power-on-reset on V_{CC}			2.5		V
V_{DDA}	Analog supply voltage		2.85	3.00	3.15	V
V_{DDD}	Digital supply voltage		1.725	1.80	1.875	V
f_{CLK}	Oscillator clock frequency	MDIV bit = 0	4.000		4.194	MHz
		MDIV bit = 1	8.000		8.192	

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
f_{LINE}	Nominal line frequency		45		65	Hz
I_{LATCH}	Current injection latch-up immunity				300	mA
Analog inputs (I_{IP1}, I_{IN1}, I_{IP2}, I_{IN2}, V_{IP}, V_{IN})						
$V_{MAX.}$	Maximum input signal levels	Voltage channel	-0.3		+0.3	V
		Current channel, gain 8X	-0.15		+0.15	V
		Current channel, gain 32X	-0.035		+0.035	V
f_{ADC}	A/D converter bandwidth			10		kHz
f_{SPL}	A/D sampling frequency			FCLK/4		Hz
V_{OFF}	Amplifier offset				±20	mV
Z_{IP}	V_{IP}, V_{IN} impedance	Over the total operating voltage range	100		400	kΩ
Z_{IN}	I_{IP1}, I_{IN1}, I_{IP2}, I_{IN2} impedance	Over the total operating voltage range		100		kΩ
G_{ERR}	Current channels gain error			±10		%
I_{VL}	Voltage channel leakage current		-1		1	µA
I_{IL}	Current channel leakage current	Channel disabled (PST=0 to 1 CH2 disabled if CSEL=0, CH1 disabled if CSEL=1) or device off	-1		1	µA
		Input enabled	-15		15	µA
Digital I/O characteristics (SDA, CLKIN, CLKOUT, SCS, SYN, LED)						
V_{IH}	Input high voltage	SDA, SCS, SYN, LED	0.75 V_{CC}			V
		CLKIN	1.5			
V_{IL}	Input low voltage	SDA, SCL, SYN, LED			0.75 V_{CC}	V
		CLKIN			0.8	
V_{OH}	Output high voltage	I_O = -2 mA	V_{CC}-0.4			V
V_{OL}	Output low voltage	I_O = +2 mA			0.4	V

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{UP}	Pull-up current			15		µA
t_{TR}	Transition time	C_{LOAD} = 50 pF		10		ns
Crystal oscillator						
I_I	Input current on CLKIN				1	µA
R_P	External resistor	1			4	MΩ
Cp	External capacitors			22		pF
f_{CLK}	Nominal output frequency		4.00	4.194		MHz
			8.00	8.192		
I_{CLKIN}	Settling current	f_{CLK} = 4 MHz	40		60	µA
R_{SET}	Settling resistor			12		kΩ
t_{JIT}	Frequency jitter			1		ns
On-chip reference voltage						
V_{REF}	Reference voltage			1.23		V
	Reference accuracy			±1		%
T_C	Temperature coefficient	After calibration		30	50	ppm/°C
SPI interface timing						
F_{SCLKr}	Data read speed	After calibration			32	MHz
F_{SCLKw}	Data write speed				100	MHz
t_{DS}	Data set-up time		20			ns
t_{DH}	Data hold time		0			ns
t_{ON}	Data driver on time				20	
t_{OFF}	Data driver off time				20	
t_{SYN}	SYN active width		$2/f_{CLK}$			s

5 Terminology

5.1 Measurement error

The error associated with the energy measurement made by the STPM10 is defined as: percentage error = [STPM10 (reading) - true energy] / true energy.

5.2 ADC offset error

This is the error due to the DC component associated with the analog inputs of the A/D converters. Due to the internal automatic DC offset cancellation, the STPM10 measurement is not affected by DC components in the voltage and current channel. The DC offset cancellation is implemented in the DSP.

5.3 Gain error

The power section is implemented with an avalanche ruggedness N-channel MOSFET, which guarantees safe operation within the specified energy rating as well as high dv/dt capability. The power section has a BV_{DSS} of 800 V min. and a typical $R_{DS(on)}$ of 20 Ω at 25 °C.

The integrated SenseFET structure allows a virtually loss-less current sensing.

The gate driver is designed to supply a controlled gate current during both turn-on and turn-off in order to minimize common mode EMI. Under UVLO conditions an internal pull-down circuit holds the gate low in order to ensure that the Power section cannot be turned on accidentally.

5.4 Power supply DC and AC rejection

This parameter quantifies the STPM10 measurement error as a percentage of the reading when the power supplies are varied. With reference to the PSRRAC measurement, a reading at two nominal supply voltages (3.3 and 5 V) is taken. A second reading is obtained with the same input signal levels when an AC (200 mV_{RMS}/100 Hz) signal is introduced on the supplies. Any error introduced by this AC signal is expressed as a percentage of the reading. Concerning the PSRRDC measurement, a reading at two nominal supply voltages (3.3 and 5 V) is taken. A second reading is obtained with the same input signal levels when the supplies are varied ± 10%. Any error introduced is again expressed as a percentage of the reading.

5.5 Conventions

The lowest analog and digital power supply voltage is called VSS, which represents system ground (GND). All voltage specifications for digital input/output pins are referred to GND. Positive currents flow into a pin. Sinking current refers to the current flowing into the pin, and thus it is positive. Sourcing current means that the current is flowing out of the pin, so it is negative. Timing specifications of signals treated by the digital control part are relative to CLKOUT. This signal is provided by the 4.194 MHz nominal-frequency crystal oscillator or from the internal RC oscillator. An external source of 4.194 MHz or 8.192 MHz can also be used. Timing specifications of signals from the SPI interface are relative to the SCL, and there is no direct relationship between the clock (SCL) of the SPI interface and the clock of the DSP block. A positive logic convention is used in all equations.

6 Typical performance characteristics

Figure 3: Supply current vs. supply voltage, TA = 25 °C (f = 4.194 MHz, 8.192 MHz)

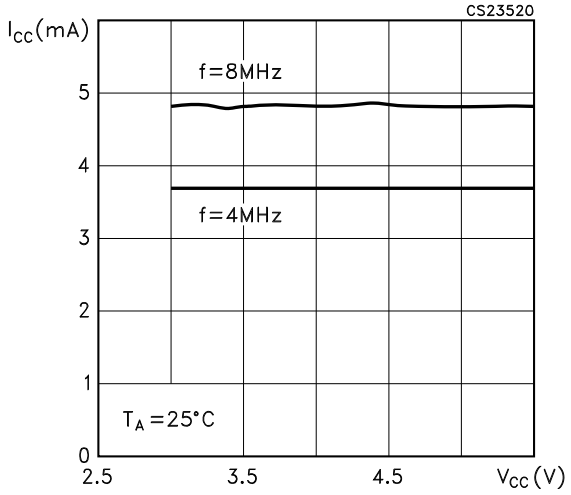


Figure 4: RC oscillator frequency vs. VCC, R = 12 kΩ, TA = 25 °C

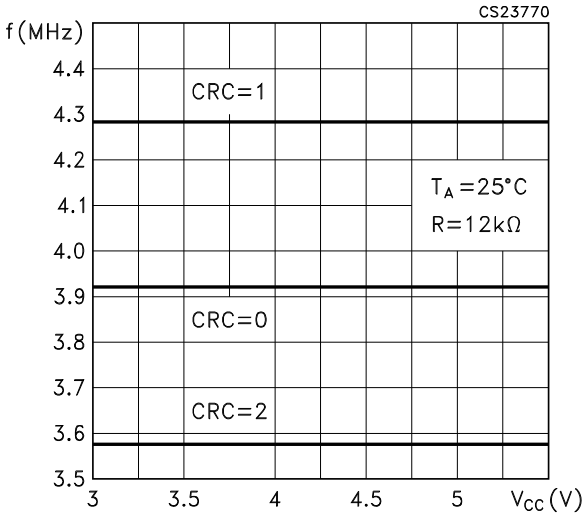


Figure 5: RC oscillator: frequency jitter vs. temperature

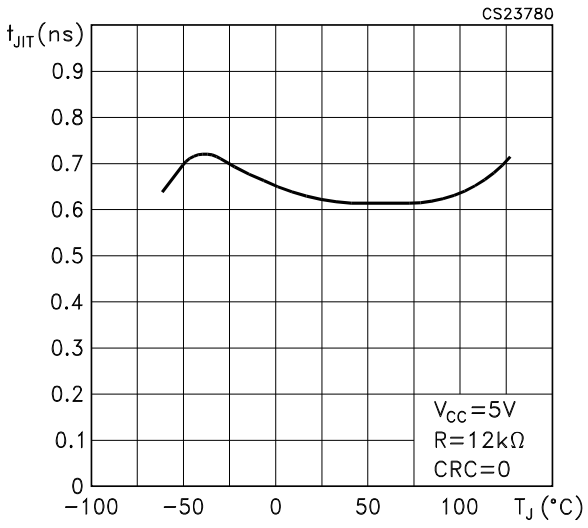


Figure 6: Analog voltage regulator: line - load regulation

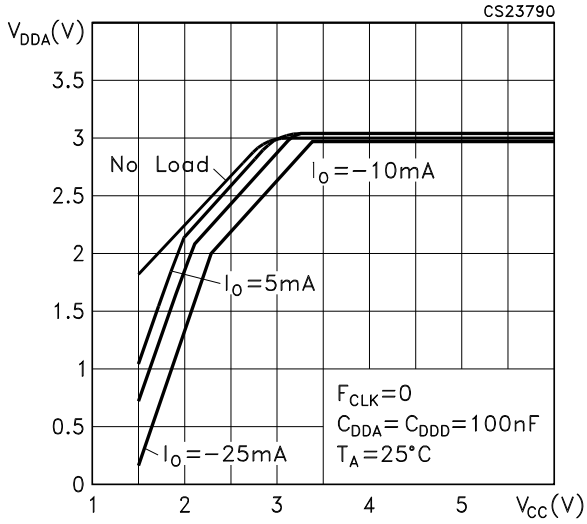


Figure 7: Digital voltage regulator: line - load regulation

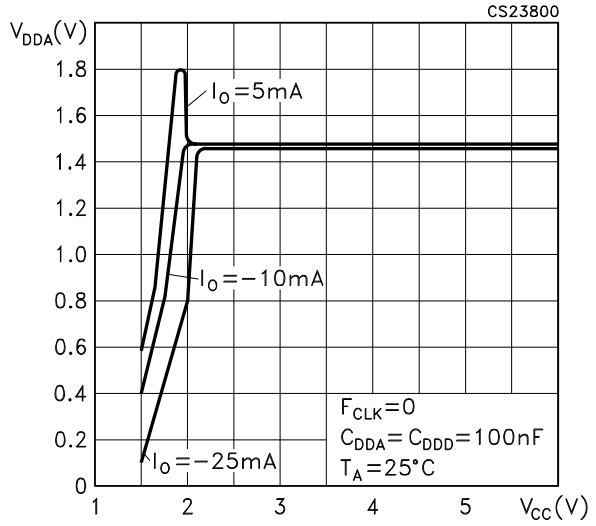


Figure 8: Voltage channel linearity at different VCC voltages

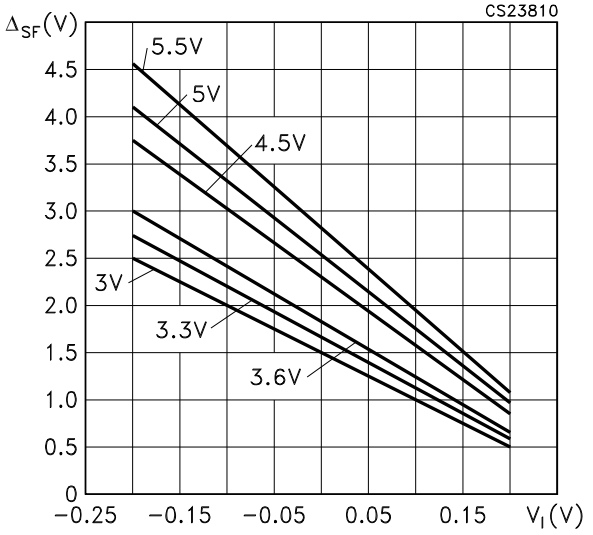


Figure 9: Power supply AC rejection vs. VCC

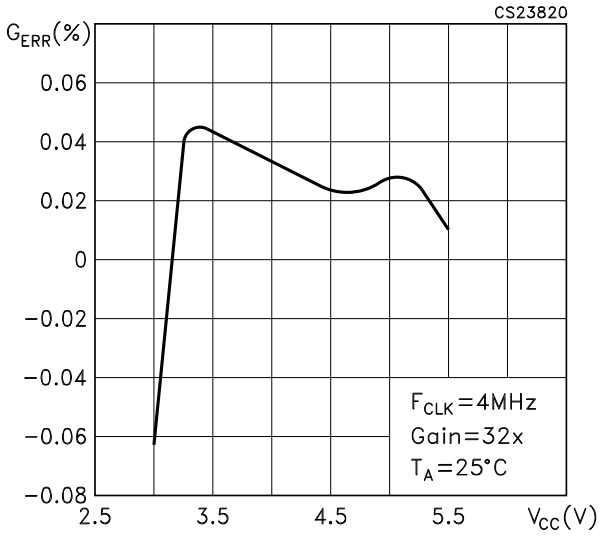


Figure 10: Power supply DC rejection vs. VCC

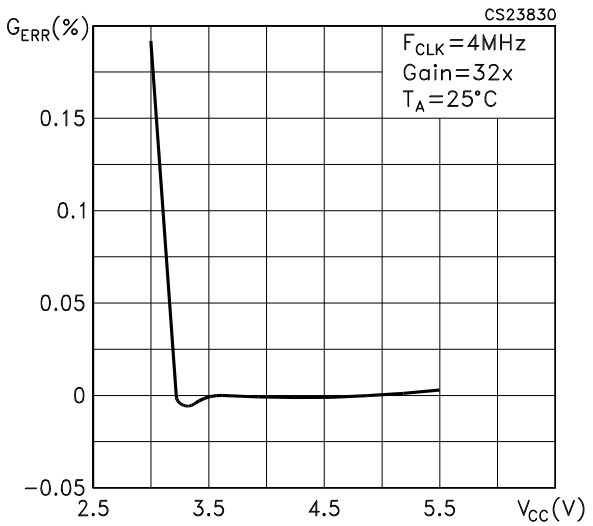


Figure 11: Error over dynamic range gain dependence

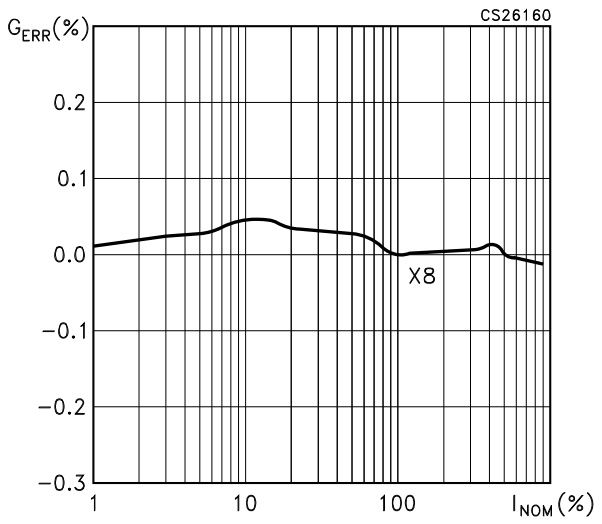


Figure 12: Primary current channel linearity at different VCC

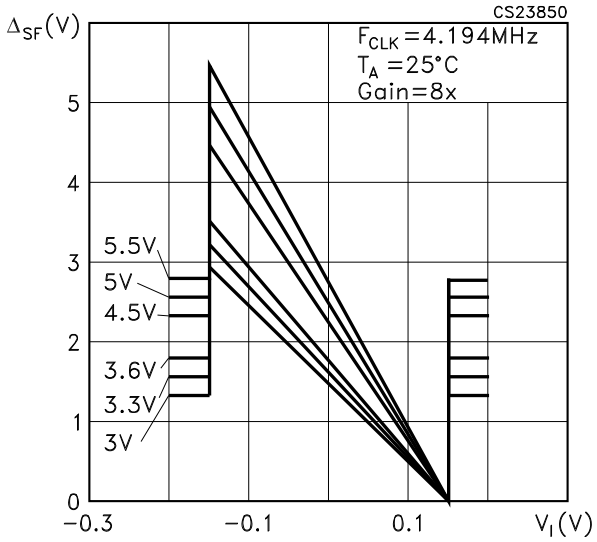
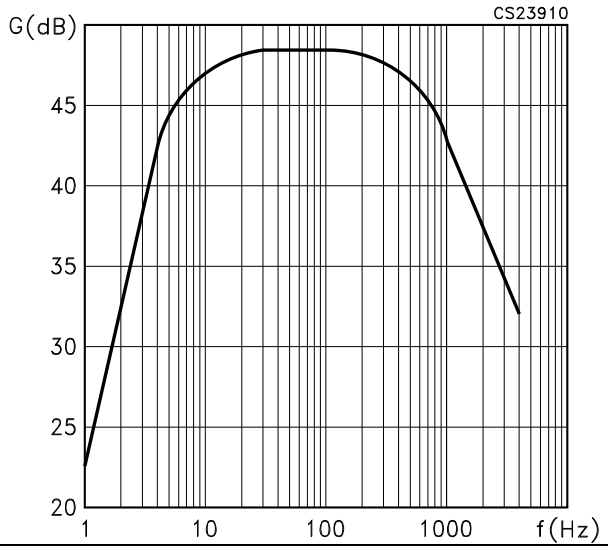


Figure 13: Gain response of ΔΣ A/D converters



7 Theory of operation

7.1 General operation description

The STPM10 is capable of performing measurements of active, reactive and apparent energy, RMS and instantaneous voltage and current values, and line frequency information. Most of the functions are fully programmable using internal configuration bits accessible through the SPI interface. The STPM10 works as a peripheral in microcontroller-based metering systems. The ZCR and WDG pins are used to provide zero-crossing and watchdog information, and the SPI pins are used to communicate with the microcontroller. The STPM10 includes volatile internal registers that hold the useful information about the metering system. Two kinds of active energy are available: wide-band active energy (AW) which includes all harmonic content (also called type 0) and fundamental active energy (AF), limited to the 1st harmonic (also called type 1). This latter energy value is obtained by filtering type 0 active energy. Both of the two active energies are stored in up-down counting accumulator registers with a 20-bit length. Reactive and apparent energies are also available with a 20-bit accumulation. The STPM10 also provides the RMS values for voltage and current. Due to the modest dynamic variation of the voltage, the RMS value is stored with a resolution of 11 bits, while the RMS current value has a resolution of 16 bits. The instantaneous (momentary) sampled value of voltage and current are also available with a resolution of 11 and 16 bits, respectively. The line frequency value is stored with a resolution of 14 bits. Due to the proprietary energy computation algorithm, the STPM10 calibration is quick and simple, allowing calibration at only one point over the entire current range. The configuration and calibration parameters must be downloaded in the internal non-volatile memory of the STPM10 at power-up.

7.2 Analog inputs

The STPM10 has one fully differential voltage input channel and two fully differential current input channels. The voltage channel consists of a differential amplifier with a gain of 4. The maximum differential input voltage for the voltage channel is ± 0.3 V. The two current channels are multiplexed (see *Section 7.9: "Tamper detection module"* for details) to provide a single input to a preamplifier with a gain of 4. The output of this preamplifier is connected to the input of a programmable gain amplifier (PGA) with possible gain selections of 2 and 8. The total gain of the current channels are then 8 and 32. The gain selections are made by writing to the gain register, and they can be different for the two current channels. If the tamper function is not used, the secondary current can be disabled. The maximum differential input voltage is dependent on the selected gain, in accordance with the table below.

Table 6: Gain of voltage and current channels

Voltage channels		Current channels	
Gain	**Max. input voltage (V)**	**Gain**	**Max. input voltage (V)**
4	±0.30	8X	±0.15
		32X	±0.35

The gain register is included in the device configuration register with the address name PST. The table below shows the gain configuration according to the register values:

Table 7: Configuration of current sensors

Primary		Secondary		Configuration bits	
Gain	**Sensor**	**Gain**	**Sensor**	**PST**	**TMP**
8	CT	Disabled	Disabled	0	0
32	Shunt	Disabled	Disabled	1	0
8	CT	8	CT	0	1
8		32	Shunt	1	1

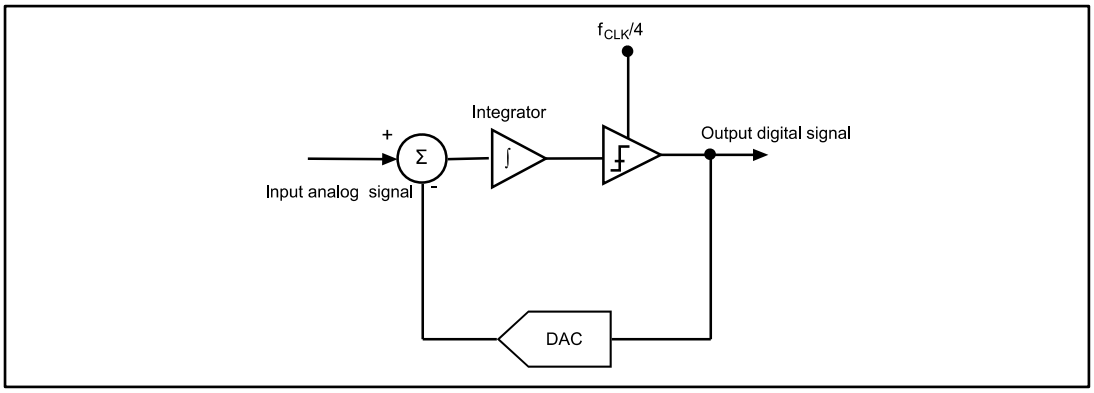
If the device is used in configuration PST = 1, TMP = 1 (primary channel with CT, secondary channel with Shunt), the shunt K_s must always be equal to one fourth of the current transformer K_s.

Both the voltage and current channels implement an active offset correction architecture which provides the benefit of avoiding any offset compensation. The analog voltage and current signals are processed by the ΣΔ analog-to-digital converters, which feed the hardwired DSP. The DSP implements an automatic digital offset cancellation that makes it possible to avoid any manual offset calibration on the analog inputs.

7.3 ΣΔ A/D converters

Analog-to-digital conversion in the STPM10 is carried out using two first-order ΣΔ converters. The device performs A/D conversions of analog signals on two independent channels in parallel. The current channel is multiplexed as a primary or secondary current channel in order to perform the tamper function, if enabled. The converted ΣΔ signals are supplied to the internal hard-wired DSP unit, which filters and integrates these signals in order to boost the resolution and to yield all the necessary signals for the computations. A ΣΔ modulator converts the input signal into a continuous serial stream of 1's and 0's at a rate determined by the sampling clock. In the STPM10, the sampling clock is equal to $f_{CLK}/4$. The 1-bit DAC in the feedback loop is driven by the serial data stream. The DAC output is subtracted from the input signal. If the loop gain is high enough, the average value of the DAC output (and therefore the bit stream) can approach that of the input signal level. When a large number of samples are averaged, a very precise value for the analog signal is obtained. This averaging is carried out in the DSP section, which implements decimation, integration and DC offset cancellation of the supplied ΣΔ signals. The gain of the decimation filters is 1.004 for the voltage channel and 0.502 for the current channel. The resulting signal has a resolution of 11 bits per voltage channel and 16 bits per current channel.

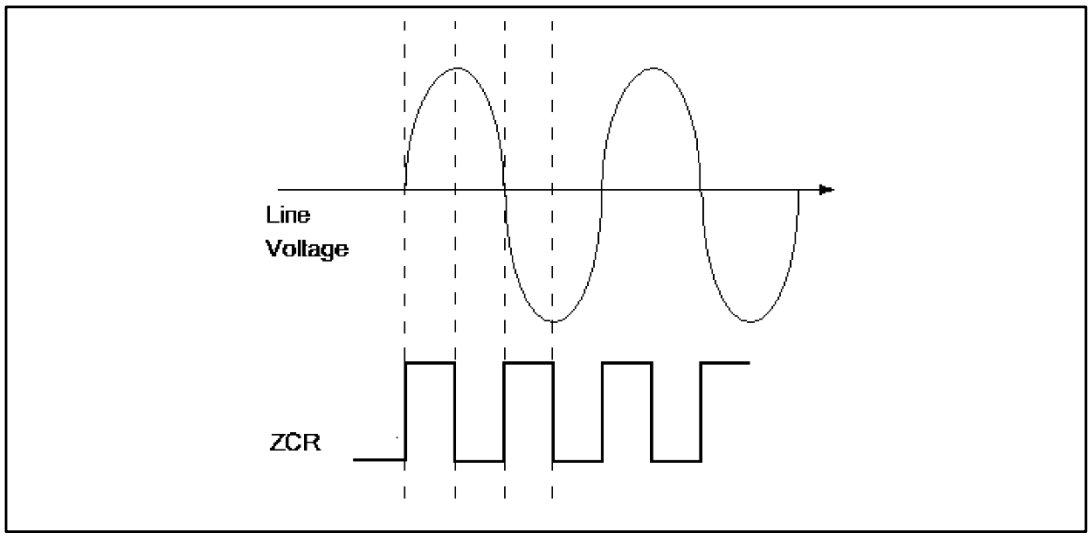
Figure 14: First-order ΣΔ A/D converter



7.4 Zero-crossing detection

The STPM10 has a zero-crossing detector circuit on the voltage channel which can be used by application for synchronization of some utility equipment in the event of zero-crossing of the line voltage. This circuit produces the internal signal ZCR which has a rising edge every time the line voltage crosses zero, and a negative edge every time the voltage reaches its positive or negative peak. The ZCR signal is then at twice the line voltage frequency. The ZCR signal is available on the ZCR pin.

Figure 15: ZCR signal

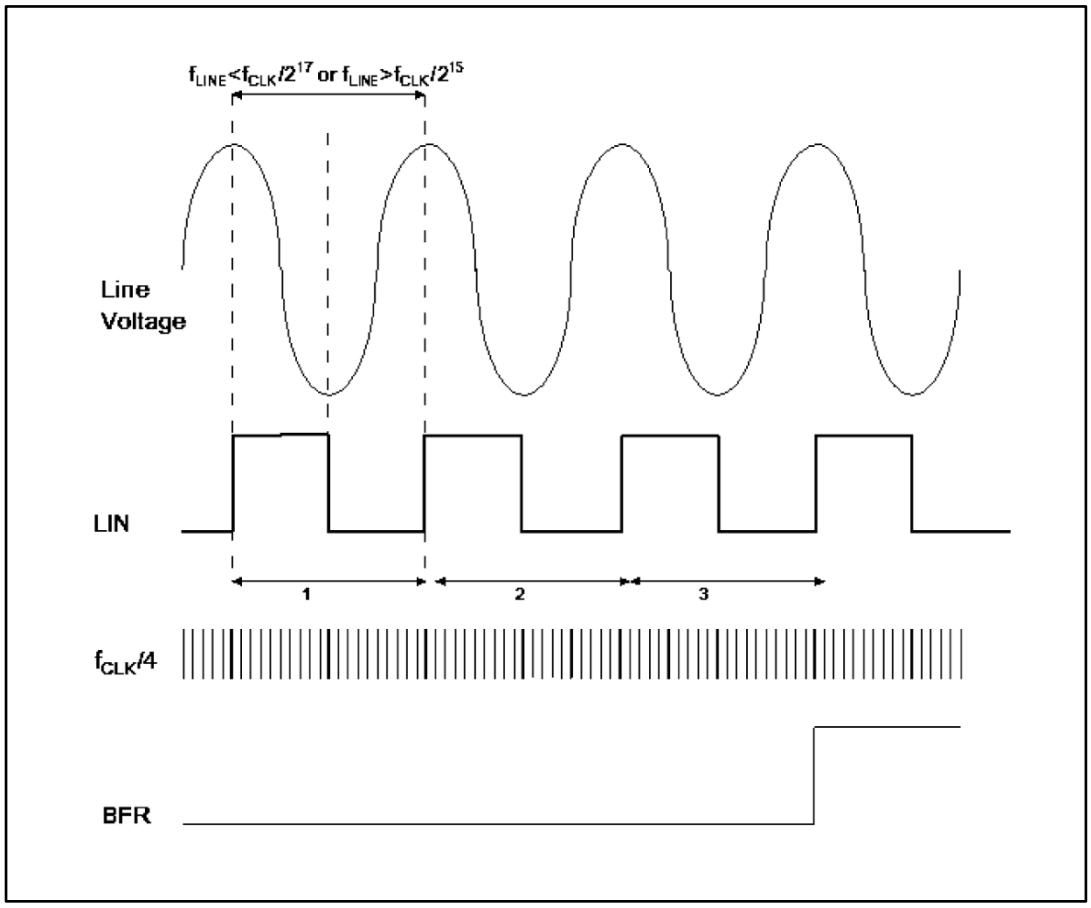


7.5 Period and line voltage measurement

The period module measures the period of the base frequency of the voltage channel and checks if the voltage signal frequency is within the $f_{CLK}/217$ to $f_{CLK}/215$ band. To do this, the LIN signal is produced, which is low when the line voltage rises, and high when the line voltage falls. This means that the LIN signal is the sign of dv/dt. With further elaboration, the ZCR signal is also produced. On the trailing edge of LIN (line frequency) the period counter starts counting up pulses of the $f_{CLK}/4$ reference signal. The LIN signal is available on the status bit register (see *Table 10: "Status bit description"*). If the counted number of pulses between two trailing edges of LIN is higher than 215, or if the counting is never

stopped (no LIN trailing edge) this means that the base frequency is lower than $f_{CLK}/217$ Hz and a BFR (base frequency range) error flag is set.

Figure 16: LIN and BFR signals



If the number of pulses counted between two trailing edges of LIN is lower than 213, the base frequency exceeds the limit (this means it is higher than $f_{CLK}/215$). In this case, the error must be repeated three consecutive times in order to set the BFR error flag. For example, with a 4.194304 MHz oscillator frequency and MDIV bit clear (or 8.192 MHz with MDIV set), $f_{CLK}/4$ is 1.048576 MHz. If the line frequency is 30 Hz, the counted $f_{CLK}/4$ pulses between two LIN trailing edges are 34952, more than 215 (32768 pulses). The BFR low frequency limit is as follows:

$f_{CLK}/217 = 4194304/131072 = 32$ Hz

With the same clock frequency, if the line frequency is 130 Hz, the $f_{CLK}/4$ pulses between two LIN trailing edges are 8066, less than 213 (8192). The BFR high frequency limit is then:

$f_{CLK}/215 = 4194304/32768 = 128$ Hz

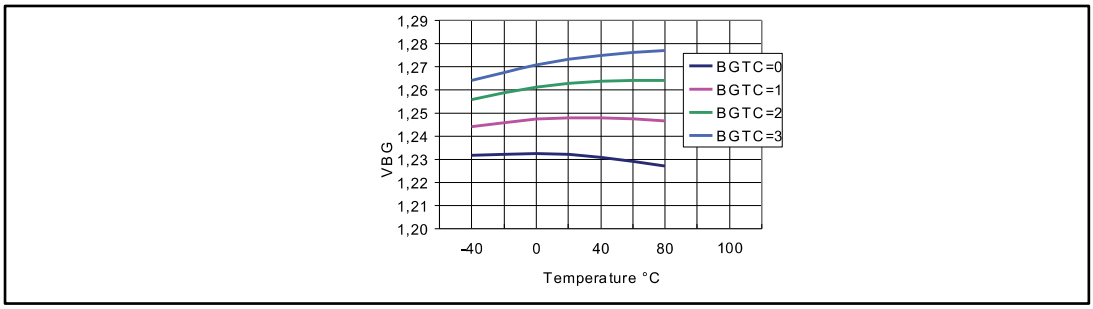
The BFR flag is also set if the register value of the RMS voltage drops below 64. BFR is cleared when the register value goes above 128. The BFR, then, also gives information about the presence of the line voltage within the meter. When the BFR error is set, the computation of power is zero unless the FRS bit is set. In fact, the effect of the BFR bit can be overridden by setting FRS configuration bit.

It means that if FRS is set and BFR is also set, all the energy computation is carried on as BFR was cleared. In this case then p=u*i, where u could be zero or not (if BFR was set because voltage RMS register value is below 64). When the line frequency re-enters the nominal band, the BFR flag is automatically reset. This BFR error flag is also assembled as part of the 8-bit status register (see *Table 10: "Status bit description"*).

7.6 Power supply

The main STPM10 supply pin is the VCC pin. From the VCC pin two linear regulators provide the necessary voltage for the analog part VDDA (3 V) and for the digital part VDDD (1.8 V). The VSS pin represents the reference point for all the internal signals. A 100 nF low ESR capacitor should be connected between VCC and VSS, VDDA and VSS, VDDD and VSS. All these capacitors must be located very close to the device. The STPM10 contains a power on reset (POR) detection circuit. If the VCC supply is less than 2.5 V, then the STPM10 goes into an inactive state, all the functions are blocked and a reset condition is asserted. This is useful to ensure correct device operation at power-up and during power-down. The power supply monitor has built-in hysteresis and filtering, which give a high degree of immunity from false triggering due to noisy supplies. A band-gap voltage reference (VBG) of 1.23 V ±1% is used as the reference voltage level source for the two linear regulators and for the A/D converters. Also, this module produces several bias currents and voltages for all other analog modules. The band-gap voltage can be compensated regardless of the temperature variations with the BGTC bits.

Figure 17: Band-gap temperature variation



7.7 Load monitoring

The STPM10 includes a no-load condition detection circuit with adjustable threshold. This circuit monitors the voltage and the current channels and, when the measured voltage is below the set threshold, the internal signal BIL becomes high. Information about this signal is also available in the status bit BIL.

The no-load condition occurs when the product of the VRMS and IRMS register values is below a given value. This value can be set with the LTCH configuration bits. Four different no-load threshold values can be chosen according to the two configuration bits LTCH (see table below). When a no-load condition occurs (BIL=1) the integration of power is suspended and the tamper module is disabled. The BIL signal can be accessed only through the SPI interface.

Table 8: No-load detection thresholds

LTCH	K_{LTCH}
0	800
1	1600
2	3200
3	6400

7.8 Error detection

In addition to the no-load condition and the line frequency band, the integration of power can also be suspended due to an error detected on the source signals. There are two kinds of error-detection circuits involved. The first checks all the ΣΔ signals from the analog part if any is stacked at 1 or 0 within the 1/128 of f_{CLK} period of observation. In case of a detected error, the corresponding ΣΔ signal is replaced with an idle ΣΔ signal, which represents a constant value of 0. All error and other resolved flags are treated as bits of a device status and can be read out by means of the SPI interface. Another error condition occurs if LED pin output signals are different from the internal signals that drive them. This can occur if some of these pins are forced to GND or to some other imposed voltage value. In this case, the internal status bit PIN is activated, providing the information that some hardware problem has been detected.

7.9 Tamper detection module

The STPM10 measures the current in both live and neutral wire with a time domain multiplexing approach on a unique sigma delta modulator. This mechanism is adopted to implement anti-tamper function. If this function is selected (see *Table 7: "Configuration of current sensors"*), the live and neutral wire currents are monitored; when the difference between the two measurements exceeds a rated threshold, the STPM10 enters the "tamper state", while in "normal state" the two measurements are below the threshold. In particular, both channels are not observed all the time, rather a time multiplex mechanism is used. During the observation time of each channel, its active energy is calculated. A tamper condition occurs when the absolute value of the difference between the two active energy values is greater than a certain percentage of the averaged energy during the activated tamper module (see equation below). This percentage value can be selected between two different values (12.5% and 6.25%) according to the value of the configuration bit CRIT. The tamper condition is detected when the following formula is satisfied:

Equation 1:

EnergyCH1 - EnergyCH2 > KCRIT (EnergyCH1 + EnergyCH2)/2

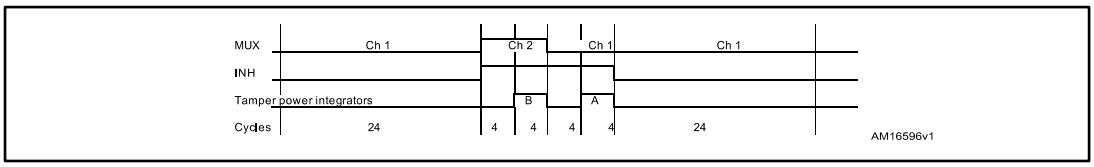
where K_{CRIT} can be 12.5% or 6.25%.

The detection threshold is much higher than the accuracy difference of the current channels, which should be less than 0.2 %, but, some headrooms should be left for possible transition effect, due to accidental synchronism of actual load current change with the rhythm of taking the energy samples. The tamper circuit works if the energies associated with the two current channels are both positive or negative, if the two energies have different sign, the tamper is on all the time however, the channel with the associated higher power is selected for the final computation of energy. When internal signals are not good enough to perform the calculations, i.e. line period is out or range or ΔΣ signals from analog section are stacked at high or low logic level, or no-load condition is activated, the tamper module is disabled and its state is preset to normal.

7.9.1 Detail operational description

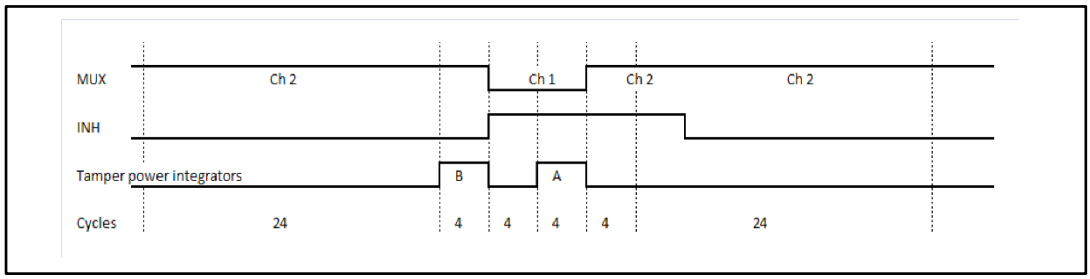
The meter is initially set to normal state, i.e. tamper not detected. In this condition the primary channel is selected for final integration of energy. In such state the values of both load currents should not differ more than the accuracy difference of the channels does. Sixty-four periods of line voltage is used as a tamper checking period. After 24 periods of line voltage two internal signals MUX and INH are changed in order to enable secondary current channel and to freeze the last power and RMS values of primary current channel. The following 16 periods of line frequency are used for tamper detection integration. During this gap, the final energy calculation does not use the signal from selected channel but the frozen values. Four line periods after the INH switch, the integration of power from secondary current channel is started and lasts four periods. Additional four line periods later MUX signal is switched back to primary current channel and the integration for tamper detection is started. The timings of MUX and INH signals are shown in the figure below.

Figure 18: Timings of tamper module - primary channel selected



When the secondary channel is selected to be integrated by the final energy integrator, the MUX and INH signals change according to the figure below.

Figure 19: Timings of tamper module - secondary channel selected



This means that energy of four periods from secondary channel followed by energy of four periods from primary channel is sampled within the tamper module. From these two samples, called B and A respectively, the criteria of tamper is calculated and the channel with higher current is selected, resulting in a new tamper state. If four consecutive new results of criteria happen, i.e. after elapsed 5.12 s at 50 Hz, the meter enters into tamper state. Thus, the channel with the higher current is selected for the energy calculation. If samples of power A and B had different signs, the tamper would be on all the time but, the channel with bigger power would be still selected for the final integration of energy. If a tamper status has been detected, the multiplex ratio is 56:8 if the primary channel energy is greater than the secondary one, otherwise it is 8:56. The detected tamper condition is stored in the BIT status bit. If BIT = 0 tamper is not detected, if BIT = 1 a tamper condition has been detected. In standalone mode the BIT flag is also available in the SDATD pin.

7.10 Phase compensation

The STPM10 does not introduce any phase shift between the voltage and current channel. However, the voltage and current signals come from transducers, which could have inherent phase errors. For example, a phase error of 0.1 ° to 0.3 ° is not uncommon for a

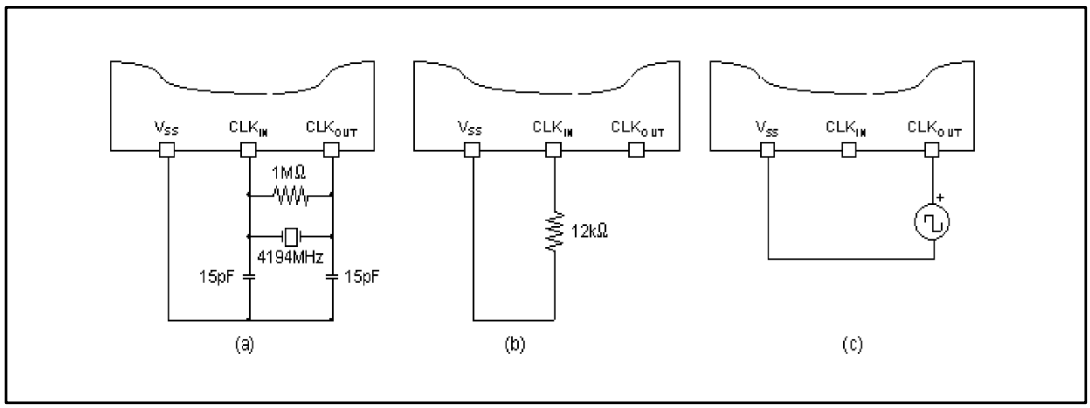
current transformer (CT). These phase errors can vary from part to part, and they must be corrected in order to perform accurate power calculations. The errors associated with phase mismatch are particularly noticeable at low power factors. The STPM10 can calibrate these small phase errors by introducing delays on the voltage or current signal. The amount of phase compensation can be set using the 4 bits of the phase calibration register (CPH). The default value of this register is at a value of 0, which gives 0 ° phase compensation. When the 4 bits give a CPH of 15 (1111) the compensation introduced is +0.576 °. This compensates the phase shift usually introduced by the current sensor, while the voltage sensor, normally a resistor divider, does not introduce any delay. The resolution step of the phase compensation is 0.038 °.

7.11 Clock generator

All the internal timing of the STPM10 is based on the CLKOUT signal. This signal can be generated in three different ways:

1. RC: this oscillator mode can be selected using the RC configuration bit. If RC = 1, the STPM10 runs using the RC oscillator. A resistor connected between CLKIN and ground sets the RC current. For 4 MHz operation, the recommended settling resistor is 12 kΩ. The oscillator frequency can be compensated using the CRC configuration bit.
2. Quartz: If RC = 0, the oscillator works with an external crystal. The recommended circuit is depicted in the figure below (b).
3. External clock: by keeping RC=0, it is also possible to feed the CLKOUT pin with an external oscillator signal.

Figure 20: Different oscillator circuits with (a) quartz, (b) internal oscillator, (c) external source



The clock generator is powered from an analog supply and is responsible for two tasks. The first is to retard the turn-on of some function blocks after POR in order to help smooth the start of the external power supply circuitry by keeping off all major loads. The second task of the clock generator is to provide all necessary clocks for the analog and digital parts. During this task, the MDIV configuration bit is used to inform the device about the nominal frequency value of CLKOUT. Two nominal frequency ranges are expected to be from 4.000 MHz to 4.194 MHz (MDIV = 0) or from 8.000 MHz to 8.192 MHz (MDIV = 1).

7.11.1 RC start-up procedure

To use the device with RC oscillator the configuration bit RC (see *Table 11: "Configuration bit map"*) must be set. Since the default configuration is for a crystal oscillator, when an RC oscillator is used instead and the device is supplied for the very first time it is not internally clocked and consequently the DSP is inactive. In this condition it is not possible to set RC

or any other configuration bit. The following SPI procedure can be run in order to set the RC bit and provide the clock to the device:

- Set the mode signal BANK
- Perform a software reset
- Read the registers: BANK mode signal should be checked and the records should show something (not 000000F0)
- Clear the mode signal BANK
- Do not perform a reading, and write configuration bit RC

In this way the RC oscillator is started. If the registers are read again, it can be seen that RC bit is set and BANK is cleared. Once the RC start-up procedure is complete, the device is clocked and active. For details on mode signals refer to *Section 7.18: "Mode signals"*, for SPI operations refer to *Section 7.19: "SPI interface"*.

7.12 Resetting the STPM10

The STPM10 has no reset pin. The device is automatically reset by the POR circuit when the VCC crosses the 2.5 V value, but it can also be reset through the SPI interface by providing a dedicated command (see *Section 7.19: "SPI interface"* for remote reset command details). In case of reset caused by the POR circuit, all clocks and both of DC buffers in the analog part are kept off for about 30 ms, as well as all blocks of the digital part, except for the SPI interface, which is held in a reset state for about 125 ms after a reset condition. When a reset is performed through SPI, no delayed turn-on is generated. Resetting the STPM10 causes all the functional modules of the STPM10 to be cleared, including the volatile memory. The reset through SPI (remote reset request) normally takes place during production testing.

7.13 Using the STPM10 in microcontroller-based meters

The STPM10 can be used in microcontroller-based energy meters. The SPI pins (SCS, SCL, SDA, SYN) are used for communication purposes, allowing the microcontroller to write and read the internal STPM10 registers. The zero-crossing signal is available at the ZCR pin (see *Section 7.4: "Zero-crossing detection"* for details about the ZCR signal). The WDG pin provides the watchdog signal (DOG). The DOG signal generates a 16 ms long positive pulse every 1.6 seconds. Generation of these pulses can be suspended if data are read in intervals shorter than 1.6 s. The DOG signal is actually a watchdog reset signal which can be used to control operation of an on-board microcontroller. It is set to high whenever the VDDA voltage is below 2.5 V, but after VDDA goes above 2.5 V this signal starts running. It is expected that an application microcontroller should access the data in the metering device on a regular basis at least 1/s (recommended is 32/s). Every latching of results in the metering device requested from the microcontroller also resets the watchdog. If latching requests are not 1.6 seconds from one another, an active high pulse on WDG is produced, because the device assumes that the microcontroller is not operating properly. An application can use this signal either to control the reset pin of its microcontroller, or it can be tied to an interrupt pin. The latter option is recommended for a battery-backup application which can enter a sleep mode due to power-down conditions, and should not be reset by a metering device as it would exit from sleep mode.

7.14 Energy-to-frequency conversion

The STPM10 provides energy-to-frequency conversion both for calibration and energy readout purposes. In fact, one convenient way to verify the meter calibration is to provide a pulse train signal with 50% duty cycle whose frequency signal is proportional to the active energy under steady load conditions. In this case, the user chooses a certain number of pulses on the LED pin that correspond to 1 kWh. This value is called P. Let us consider the