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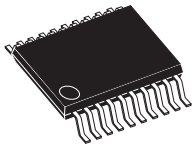
STPM11, STPM12
STPM13, STPM14

Single phase energy metering IC with pulsed output and digital calibration

Features

- Ripple free active energy pulsed output
- Direct stepper counter drivers
- Shunt, current transformer, Rogowsky coil sensors
- Live and neutral monitoring (STPM13/14)
- Easy and fast digital calibration at only one load point
- No-load, negative power and tamper indicators
- Integrated linear VREGs
- RC (STPM11/13) or crystal oscillator (STPM12/14)
- Support 50 ÷ 60 Hz - IEC62052-11, IEC62053-2X specification
- Less than 0.1% error



TSSOP20

Description

The STPM1x family is designed for effective measurement of active energy in a power line system using a Rogowski Coil, current transformer and shunt sensors. This device is specifically designed to provide all the necessary features to implement a single phase energy meter without any other active component. The STPM1x device family consists, essentially, of two parts: the analog part and the digital part. The former, is composed of a preamplifier and first order $\sum \Delta$ A/D converter blocks, band gap voltage reference, low drop voltage regulator. The digital part is composed of a system control, oscillator, hard wired DSP and interface for calibration and configuration. The calibration and configuration are done by OTP cells, that can be programmed through a serial interface. The configured bits are used for testing, configuration and calibration purposes. From two $\sum \Delta$ output signals coming from the analog section, a DSP unit computes the amount of consumed active energy. The active energy is available as a pulse frequency output and directly driven by a stepper counter. In the STPM1x an output signal with pulse frequency proportional to energy is generated. This signal is used in the calibration phase of the energy meter application allowing a very easy approach. When the device is fully configured and calibrated, a dedicated bit of OTP block can be written permanently in order to prevent accidental entry into test mode or changing any configuration bit.

Table 1. Device summary

Order codes	Package	Packaging
STPM11ATR	TSSOP20 (tape and reel)	2500 parts per reel
STPM12ATR	TSSOP20 (tape and reel)	2500 parts per reel
STPM13ATR	TSSOP20 (tape and reel)	2500 parts per reel
STPM14ATR	TSSOP20 (tape and reel)	2500 parts per reel

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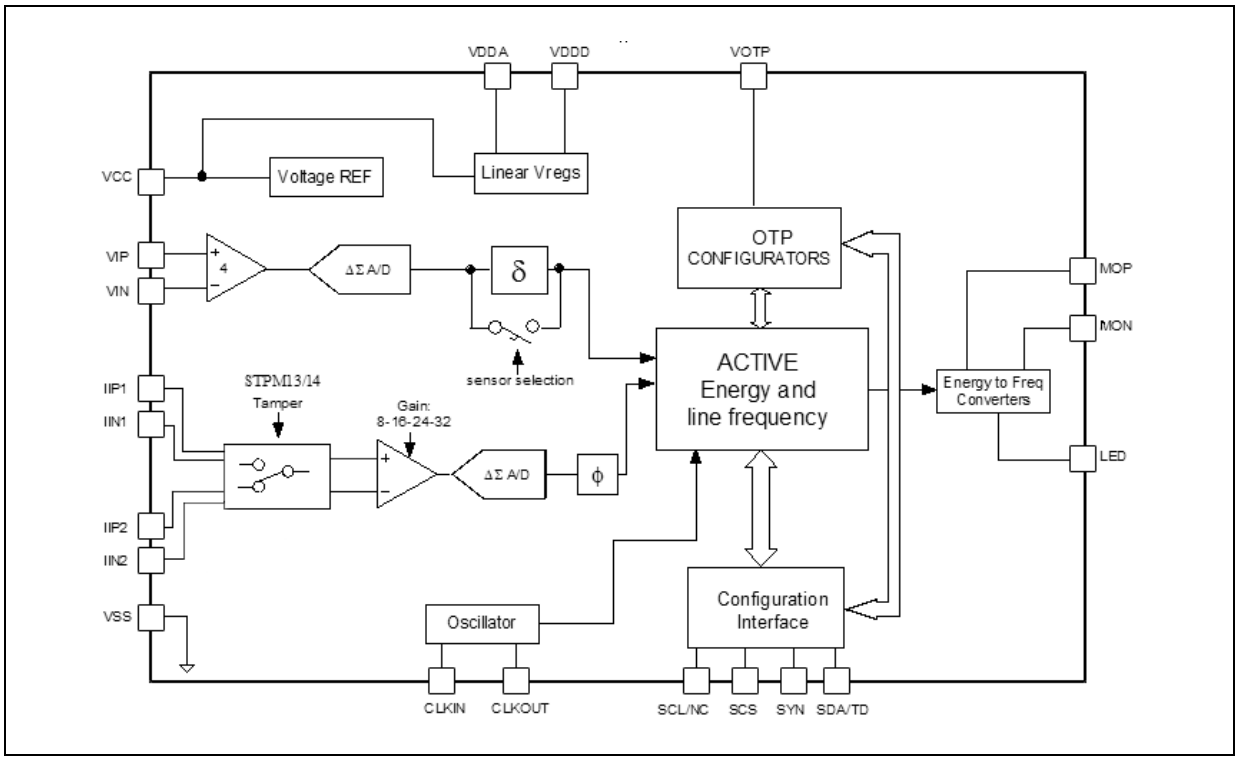
1 Schematic diagram

Figure 1. Block diagram



2 Pin configuration

Figure 2. Pin connections (top view)

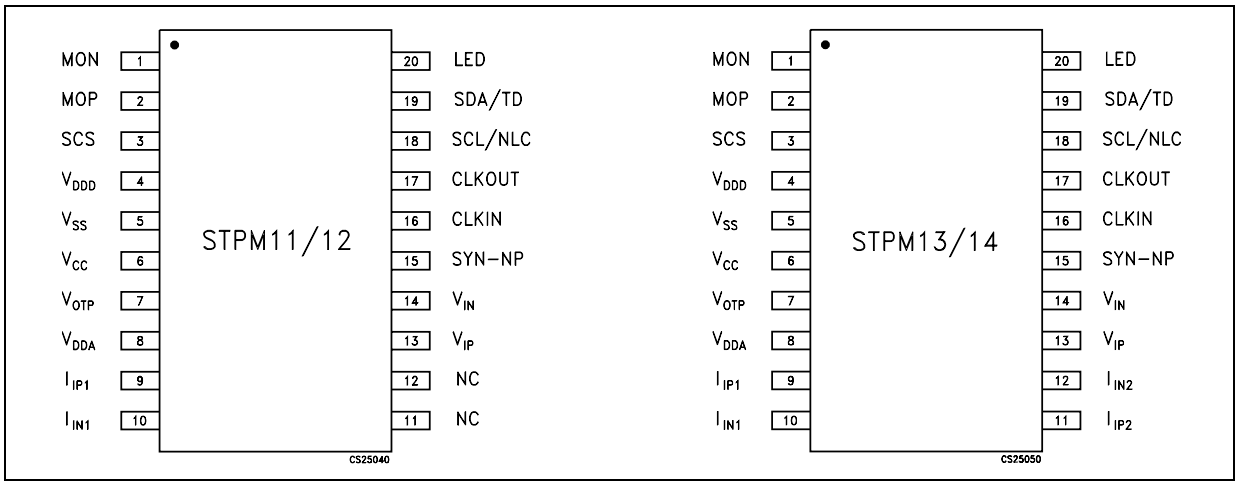


Table 2. Pin description

Pin n°	Symbol	Type (1)	Name and function
1	MON	P O	Output for Stepper's node
2	MOP	P O	Output for Stepper's node
3	SCS	D IN	Enable or disable configuration interface for device configuration.
4	V_{DDD}	A OUT	1.5 V Output of internal low drop regulator which supplies the digital core.
5	V_{SS}	GND	Ground.
6	V_{CC}	P IN	Supply voltage.
7	V_{OTP}	P INr	Supply voltage for OTP cells.
8	V_{DDA}	A OUT	3 V output of internal low drop regulator which supplies the analog part.
9	I_{IP1}	A IN	Positive input of primary current channel
10	I_{IN1}	A IN	Negative input of primary current channel
11	I_{IP2}	A IN	Positive input of secondary current channel (STPM13/14 only)
12	I_{IN2}	A IN	Negative input of secondary current channel (STPM13/14 only)
13	V_{IP}	A IN	Positive input of voltage channel
14	V_{IN}	A IN	Negative input of voltage channel
15	SYN-NP	D I/O	Negative power indicator. (Configuration interface)
16	CLKIN	A IN	Crystal oscillator input or resistor connection if RC oscillator is selected
17	CLKOUT	A OUT	Oscillator output (RC or crystal)
18	SCL/NLC	D I/O	No-load condition indicator. (Configuration interface)
19	SDATD	D I/O	Tamper detection indicator. (Configuration interface)
20	LED	D O	Pulsed output proportional to active energy

1. A: Analog, D: Digital, P: Power

3 Maximum ratings

Table 3. Absolute maximum ratings (see *Note:*)

Symbol	Parameter	Value	Unit
V_{CC}	DC input voltage	-0.3 to 6	V
I_{PIN}	Current on any pin (sink/source)	± 150	mA
V_{ID}	Input voltage at digital pins (SCS, MOP, MON, SYN, SDATD, SCLNLC, LED)	-0.3 to V_{CC}+0.3	V
V_{IA}	Input voltage at analog pins (I_{IP1}, I_{IN1}, I_{IP2}, I_{IN2}, V_{IP}, V_{IN})	-0.7 to 0.7	V
V_{OTP}	Input voltage at OTP pin	-0.3 to 25	V
ESD	Human body model (all pins)	± 3.5	kV
T_{OP}	Operating ambient temperature	-40 to 85	°C
T_J	Junction temperature	-40 to 150	°C
T_{STG}	Storage temperature range	-55 to 150	°C

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

Table 4. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction-ambient	114.5 (1)	°C/W

1. This value is referred to single-layer PCB, JEDEC standard test board.

4 Electrical characteristics

V_{CC} = 5 V, T_A= 25°C, 2.2 µF between V_{DDA} and V_{SS}, 2.2 µF between V_{DDD} and V_{SS}, 2.2 µF between V_{CC} and V_{SS} unless otherwise specified.

Table 5. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Energy measurement accuracy						
f_{BW}	Effective bandwidth	Limited by digital filtering	5		400	Hz
e_{AW}	Accuracy of active power	Over 1 to 1000 of dynamic range		0.1		%
SNR	Signal to noise ratio	Over the entire bandwidth		52		db
$PSRR_{DC}$	Power supply DC rejection	Voltage signal: 200mV_{rms}/50Hz Current signal: 10mV_{rms}/50 Hz f_{CLK}= 4.194 MHz V_{CC}=3.3V±10%, 5 V±10%			0.2	%
$PSRR_{AC}$	Power supply AC rejection	Voltage signal: 200 mV_{rms}/50 Hz Current signal: 10 mV_{rms}/50 Hz f_{CLK} = 4.194 MHz, V_{CC}=3.3 V+0.2 V_{rms}1@100 Hz V_{CC}=5.0 V+0.2 V_{rms}1@100 Hz			0.1	%
General section						
V_{CC}	Operating supply voltage		3.0		5.5	V
I_{CC}	Supply current configuration registers cleared or device locked (TSTD=1)	4 MHz, V_{CC} = 5 V		3.5	4	mA
		8 MHz, V_{CC} = 5 V		4.7	6	
ΔI_{CC}	Increase of supply current per configuration bit, during programming	4 MHz, V_{CC} = 5 V		120		µA/bit
	Increase of supply current per configuration bit with device locked	4 MHz, V_{CC} = 5 V		2		
POR	Power on reset on V_{CC}			2.5		V
V_{DDA}	Analog supply voltage		2.85	3.0	3.15	V
V_{DDD}	Digital supply voltage		1.425	1.50	1.575	V
f_{CLK}	Oscillator clock frequency	MDIV bit = 0	4.000		4.194	MHz
		MDIV bit = 1	8.000		8.192	MHz
f_{LINE}	Nominal line frequency		45		65	Hz
V_{OTP}	OTP programming voltage		14		20	V
I_{OTP}	OTP programming current per bit			2.5		mA
t_{OTP}	OTP programming time per bit		100		300	µs

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
I_{LATCH}	Current injection latch-up immunity					300	mA
Analog Inputs (I_{IP1}, I_{IN1}, I_{IP2}, I_{IN2}, V_{IP}, V_{IN})							
V_{MAX}	Maximum input signal levels	Voltage channel		-0.3		0.3	V
		Current channels	Gain 8X	-0.15		0.15	V
			Gain 16X	-0.075		0.075	
			Gain 24X	-0.05		0.05	
			Gain 32X	-0.035		0.035	
f_{ADC}	A/D Converter bandwidth				10		kHz
f_{SPL}	A/D Sampling frequency				$F_{CLK}/4$		Hz
V_{OFF}	Amplifier offset					±20	mV
Z_{IP}	V_{IP}, V_{IN} Impedance	Over the total operating voltage range		100		400	kΩ
Z_{IN}	V_{IP1}, V_{IN1}, V_{IP2}, V_{IN2} Impedance	Over the total operating voltage range			100		kΩ
G_{ERR}	Current channels gain error				±10		%
I_{ILV}	Voltage channel leakage current			-1		1	µA
I_{LEAK}	Current channel leakage current	Input disabled		-1		1	µA
		Input enabled		-10		10	
Digital I/O Characteristics (SDA-TD, CLKIN, CLKOUT, SCS, SYN-NP, LED)							
V_{IH}	Input high voltage	SDA-TD, SCS, SYN-NP, LED		$0.75V_{CC}$			V
		CLKIN		1.5			
V_{IL}	Input low voltage	SDA-TD, SCS, SYN-NP, LED				$0.25V_{CC}$	V
		CLKIN				0.8	
V_{OH}	Output high voltage	I_O = -2 mA		V_{CC}-0.4			V
V_{OL}	Output low voltage	I_O = +2 mA				0.4	V
I_{UP}	Pull up current				15		µA
t_{TR}	Transition time	C_{LOAD} = 50 pF			10		ns
Power I/O Characteristics (MOP, MON)							
V_{OH}	Output high voltage	I_O = -14 mA		V_{CC}-0.5			V
V_{OL}	Output low voltage	I_O = +14 mA				0.5	V
t_{TR}	Transition time	C_{LOAD} = 50 pF		5	10		ns
Crystal oscillator (STPM12/14)							
I_I	Input current on CLKIN					±1	µA

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
R_P	External resistor		1		4	MΩ
C_P	External capacitors			22		pF
f_{CLK}	Nominal output frequency		4	4.194		MHz
			8	8.192		
RC Oscillator (STPM11/13)						
I_{CLKIN}	Settling current	f_{CLK} = 4 MHz	40		60	µA
R_{SET}	Settling resistor			12		kΩ
t_{JIT}	Frequency jitter			1		ns
On chip reference voltage						
V_{REF}	Reference voltage			1.23		V
	Reference accuracy			±1		%
T_C	Temperature coefficient	After calibration		30	50	ppm/°C
Configuration interface timing						
F_{SCLKw}	Data write speed				100	kHz
t_{DS}	Data setup time		20			ns
t_{DH}	Data hold time		0			ns
t_{SYN}	SYN-NP active width		$2/f_{CLK}$			s

Table 6. Typical external components

Function	Component	Parameter	Value	Tolerance	Unit
Line voltage interface	Resistor divider	R to R ratio V_{RMS} = 230 V	1650	±1%	V/V
		R to R ratio V_{RMS} = 110 V	830	±1%	
Line current interface	Current shunt	Current to voltage conversion ratio	0.2	±5%	mV/A
	Current transformer		30	±12%	
	Rogowsky coil		3	±12%	

5 Terminology

5.1 Measurement error

The error associated with the energy measured by STPM1X is defined as:

Percentage Error = [STPM1X (reading) - True Energy] / True Energy

5.2 ADC offset error

This is the error due to the DC component associated with the analog inputs of the A/D converters. Due to the internal automatic DC offset cancellation, the STPM1X measurement is not affected by DC components in voltage and current channel. The DC offset cancellation is implemented in the DSP.

5.3 Gain error

The gain error is gain due to the signal channel gain amplifiers. This is the difference between the measured ADC code and the ideal output code. The difference is expressed as a percentage of the ideal code.

5.4 Power supply DC and AC rejection

This parameter quantifies the STPM1X measurement error as a percentage of the reading when the power supplies are varied. For the $PSRR_{AC}$ measurement, a reading at two nominal supply voltages (3.3 and 5 V) is taken. A second reading is obtained with the same input signal levels when an ac (200 mV_{RMS}/100 Hz) signal is introduced onto the supply voltages. Any error introduced by this ac signal is expressed as a percentage of reading.

For the $PSRR_{DC}$ measurement, a reading at two nominal supply voltages (3.3 and 5 V) is taken. A second reading is obtained with the same input signal levels when the supplies are varied ±10%. Any error introduced is again expressed as a percentage of the reading.

5.5 Conventions

The lowest analog and digital power supply voltage is named V_{SS} which represents the system Ground (GND). All voltage specifications for digital input/output pins are referred to GND.

Positive currents flow into a pin. Sinking current means that the current is flowing into the pin and is positive. Sourcing current means that the current is flowing out of the pin and is negative.

The timing specifications of the signal treated by digital control are relative to CLKOUT. This signal is provided by from the crystal oscillator of 4.194 MHz nominal frequency or by the internal RC oscillator. An external source of 4.194 MHz or 8.192 MHz can be used.

The timing specifications of signals of the CFGI interface are relative to the SCL-NLC, there is no direct relationship between the clock (SCL-NLC) of the CFGI interface and the clock of the DSP block.

A positive logic convention is used in all equations.

6 Typical performance characteristics

Figure 3. Supply current vs. supply voltage, T_A = 25 °C

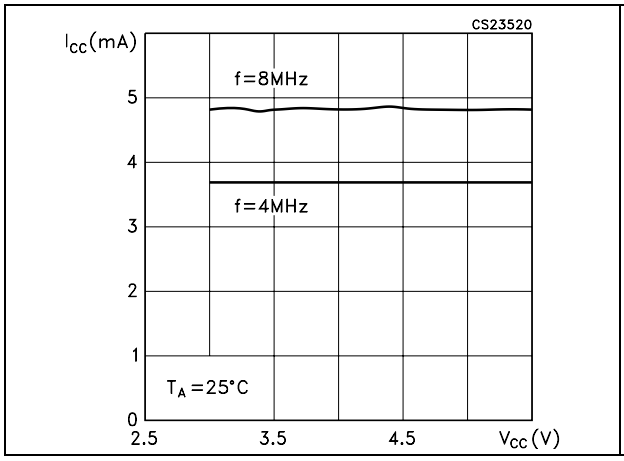


Figure 4. RC oscillator frequency vs. V_{CC}, R = 12 kΩ, T_A = 25 °C

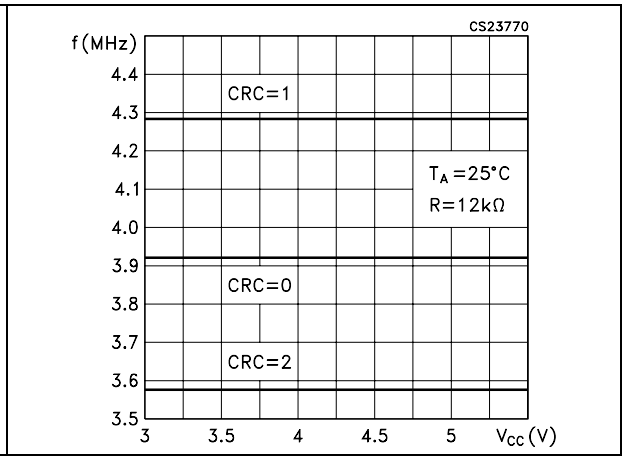


Figure 5. RC oscillator: frequency jitter vs. temperature

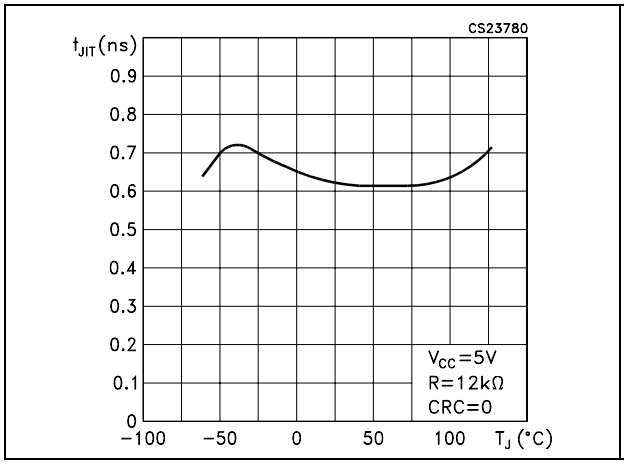


Figure 6. Analog voltage regulator: line - load regulation

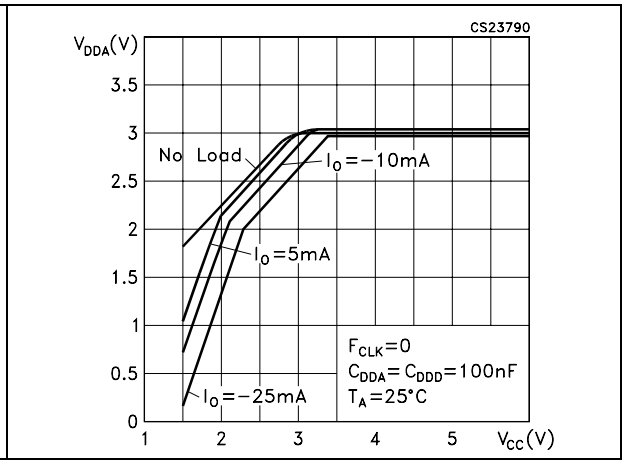


Figure 7. Digital voltage regulator: line - load regulation

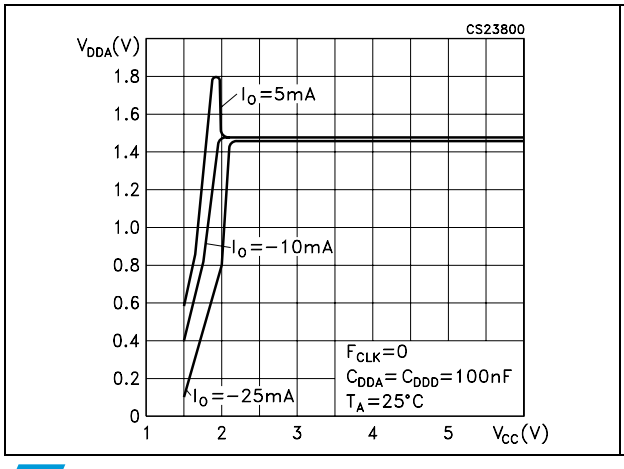


Figure 8. Voltage channel linearity at different V_{CC} voltages

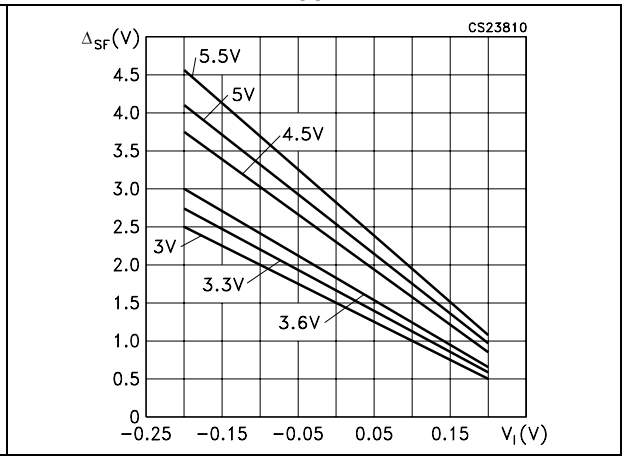


Figure 9. Power supply AC rejection vs. V_{CC}

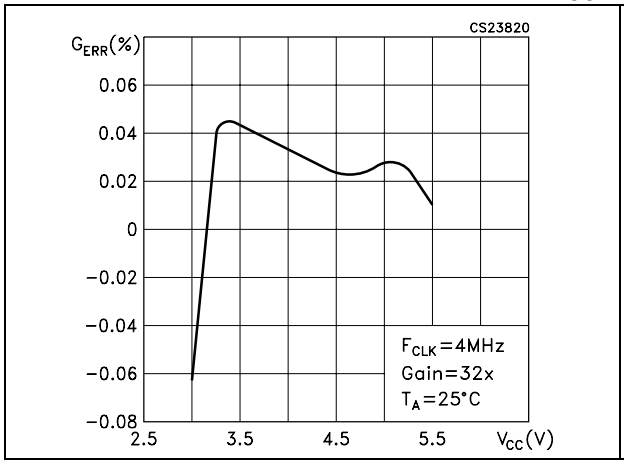


Figure 10. Power supply DC rejection vs. V_{CC}

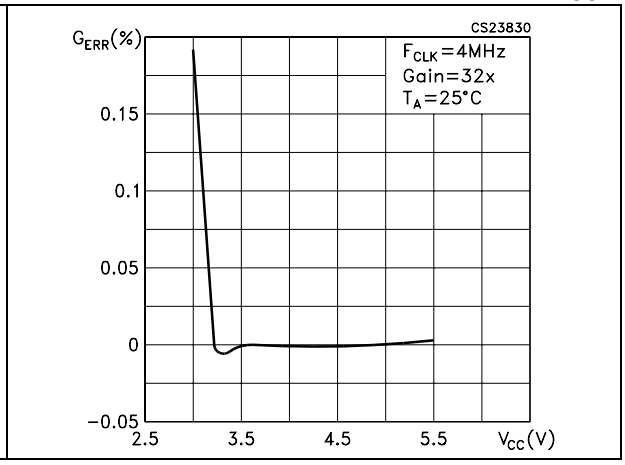


Figure 11. Error over dynamic range gain dependence

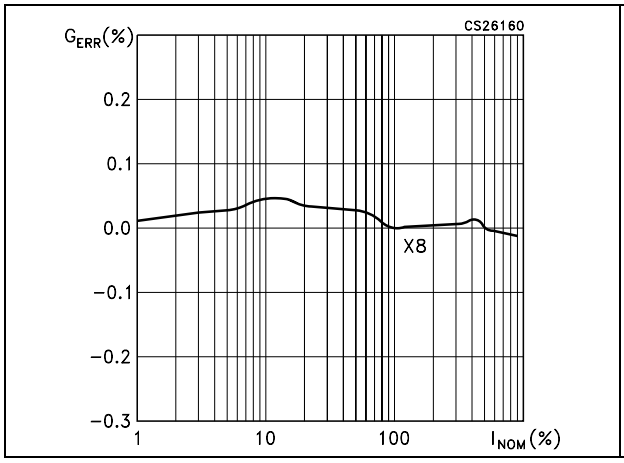


Figure 12. Primary current channel linearity at different V_{CC}

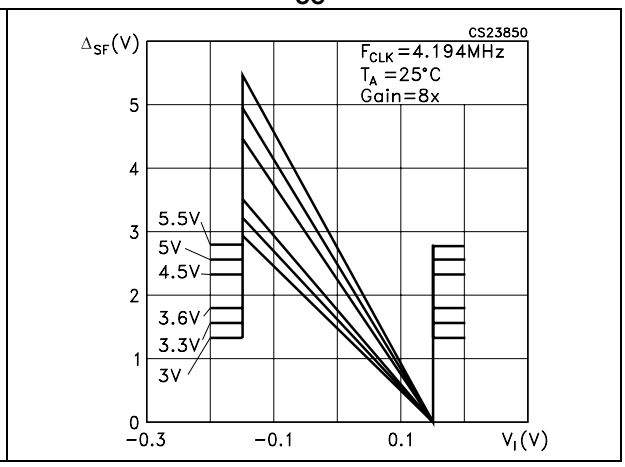


Figure 13. Gain response of ΔΣ AD Converters

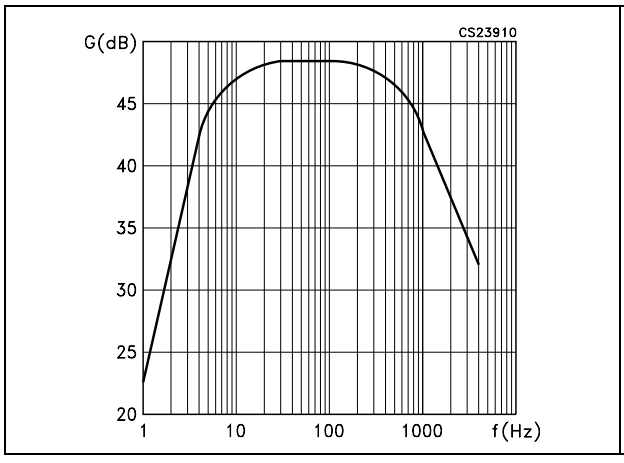
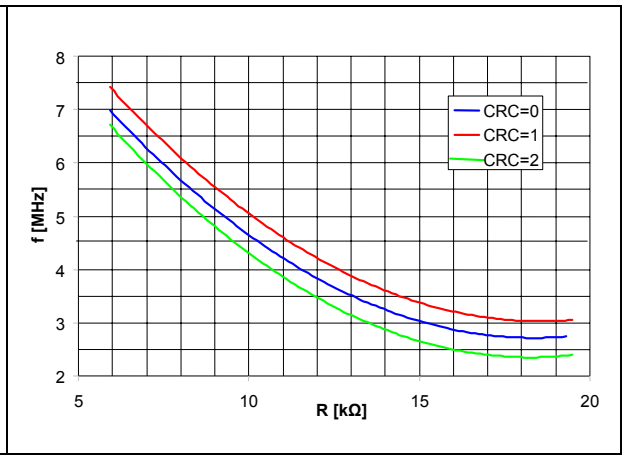


Figure 14. Clock frequency vs. external resistor



7 Theory of operation

7.1 General operation

The STPM1X is able to perform active energy measurement (wide band or fundamental) in single-phase energy meter systems.

Due to the proprietary energy computation algorithm, STPM1X active energy is not affected by any ripple at twice the line frequency. The calibration is very easy and fast allowing calibration in only one point over the whole current range which allows saving time during the calibration phase of the meter. The calibration parameters are permanently stored in the OTP (one time programmable) cells, preventing calibration tampering.

Several functions are programmable using internal configuration bits accessible through the configuration interface. The most important configuration bits are two configuration bits called PST that allow the selection of the sensor and the gain of the input amplifiers.

The STPM1X is able to directly drive a stepper motor with the MOP and MON pins, and provides information on tamper, no-load and negative power.

Two kinds of active energy can be selected to be brought to the LED pin: the total active energy that includes all harmonic content in bandwidth or the active energy limited to the 1st harmonic only. This last energy value is obtained by filtering the wide band active energy.

7.2 Analog inputs

Input amplifiers

The STPM1X has one fully differential voltage input channel and one (STPM11/12) or two (STPM13/14) fully differential current input channels.

The voltage channel consists of a differential amplifier with a gain of 4. The maximum differential input voltage for the voltage channel is ± 0.3 V.

In STPM13/14, the two current channels are multiplexed (see tamper section for details) to provide a single input to a preamplifier with a gain of 4. The output of this preamplifier is connected to the input of a programmable gain amplifier (PGA) with possible gain selections of 2, 4, 6, 8. The total gain of the current channels will be then 8, 16, 24, 32. The gain selections are made by writing to the gain configuration bits PST and it can be different for the two current channels. The maximum differential input voltage is dependent on the selected gain according to the *Table 7*:

Table 7. Voltage channel

Voltage channels		Current channels	
Gain	**Max input voltage (V)**	**Gain**	**Max input voltage (V)**
4	±0.30	8X	±0.15
		16X	±0.075
		24X	±0.05
		32X	±0.035

The *Table 8* and *Table 9* below show the gain values according to the configuration bits:

Table 8. Configuration of current sensors

STPM11/12			
Current channel		Configuration Bits	
Gain	Sensor	PST (2bits)	ADDG (1 bit)
8	Rogowsky Coil	0	0
16		0	1
24		1	0
32		1	1
8	CT	2	x
32	Shunt	3	x

Table 9. Configuration of current sensors

STPM13/14					
Primary		Secondary		Configuration Bits	
Gain	Sensor	Gain	Sensor	PST (2bits)	ADDG (1 bit)
8	Rogowsky Coil	8	Rogowsky Coil	0	0
16		16		0	1
24		24		1	0
32		32		1	1
8	CT	8	CT	2	x
8		32	Shunt	3	x

Both the voltage and current channels implement an active offset correction architecture which has the benefit of avoiding any offset compensation.

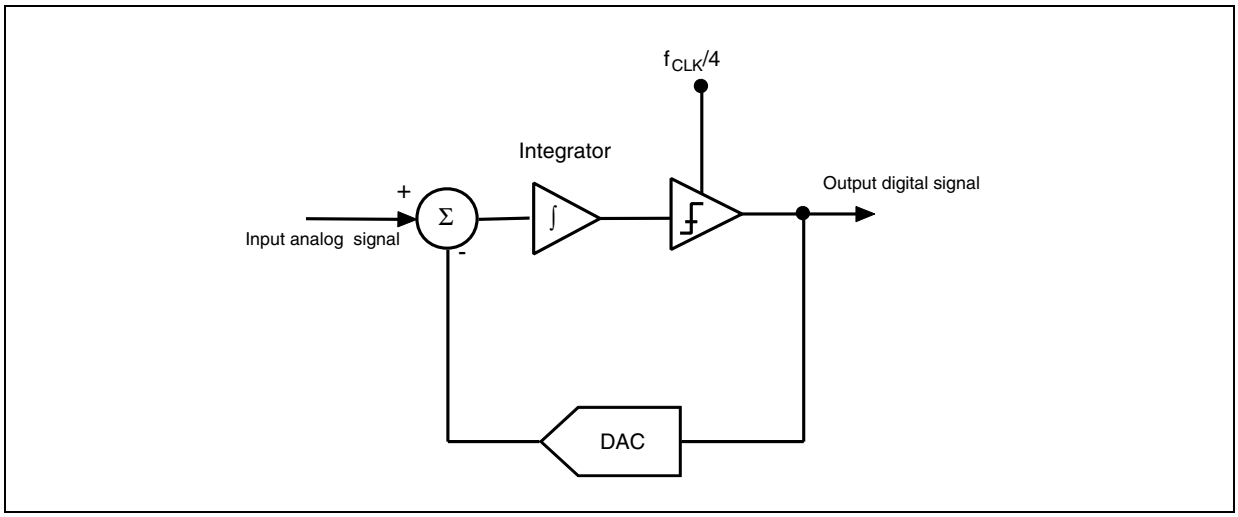
The analog voltage and current signals are processed by the $\sum \Delta$ Analog to digital converters that feed the hardwired DSP. The DSP implements an automatic digital offset cancellation that makes possible avoiding any manual offset calibration on the analog inputs.

7.3 $\sum\Delta$ A/D Converters

The analog to digital conversion in the STPM1X is carried out using two first order $\sum \Delta$ converters. The device performs A/D conversions of analog signals on two independent channels in parallel. In STPM13/14, the current channel is multiplexed as primary or secondary current channel in order to be able to perform a tamper function. The converted $\sum \Delta$ signals are supplied to the internal hardwired DSP unit, which filters and integrates those signals in order to boost the resolution and to yield all the necessary signals for computations.

A ∑ Δ modulator converts the input signal into a continuous serial stream of 1s and 0s at a rate determined by the sampling clock. In the STPM1X, the sampling clock is equal to $f_{CLK}/4$. The 1-bit DAC in the feedback loop is driven by the serial data stream. The DAC output is subtracted from the input signal. If the loop gain is high enough, the average value of the DAC output (and therefore the bit stream) can approach that of the input signal level. When a large number of samples are averaged, a very precise value of the analog signal is obtained. This averaging is carried out in the DSP section which implements decimation, integration and DC offset cancellation of the supplied ∑ Δ signals. The gain of the decimation filters is 1.004 for the voltage channel and 0.502 for the current channel. The resulting signal has a resolution of 11bits for voltage channel and 16 bits for current channel.

Figure 15. First order ∑ Δ A/D converter



7.4 Period and line voltage measurement

The period module measures the period of base frequency of voltage channel and checks if the voltage signal frequency is in the band from $f_{CLK}/2^{17}$ to $f_{CLK}/2^{15}$. An internal signal is produced at every positive peak of the line voltage. If the counted number of pulses between two trailing edges of this signal is higher than the $f_{CLK}/2^{17}$ Hz equivalent pulses or if the counting is stopped (internal signal is not available), it means that the base frequency is lower than $f_{CLK}/2^{17}$ Hz and an internal error flag BFR (base frequency range) is set.

If the counted number of pulses within one line period is higher than the $f_{CLK}/2^{15}$ equivalent pulses, the base frequency exceeds the limit. In this case, such error must be repeated three times in a row, in order to set the error flag BFR.

The BFR flag is also set if the value of the RMS voltage drops below a certain value (BFR-on) and it is cleared when the RMS voltage goes above BFR-off threshold. The table below shows the equivalent RMS voltage on the V_{IP}/V_{IN} pins according to the value of the voltage channel calibrator.

The BFR flag is also set if the RMS voltage across V_{IP}-V_{IN} drops below a threshold value calculated with the following formula:

Equation 1

$$V_{IRMS-BFR} = \frac{64}{6703 \cdot K_V}$$

(CT/Shunt)

Equation 2

$$V_{IRMS-BFR} = \frac{64}{6687 \cdot K_V}$$

(Rogowsky)

Where K_V is the voltage calibrator value ranging from 0.875 to 1.000.

The BFR flag is cleared when the V_{IRMS} value goes above twice $V_{IRMS-BFR}$. When the BFR error is set, the computation of power is suspended and MOP, MON and LED will be held low.

Table 10. RMS voltage check

	BFR-on	BFR-off
Rogowsky	0.009571/Kv	0.019142/Kv
CT-Shunt	0.0078/Kv	0.0156/Kv

7.5 Single wire meter mode (STPM13/14 with Rogowsky coil sensor)

STPM1X supports the single wire meter (SWM) operation when working with Rogowsky Coil current sensors. In SWM mode there is no available voltage information in the voltage channel. It is possible that someone has disconnected one wire (live or neutral) of the meter for tampering purposes or in case the line voltage is very stable, it is possible to use a predefined value for computing the energy without sensing it.

In order to enable the SWM mode, the STPM1X must be configured with PST values of 0 or 1. In this way, if the BFR error is detected, STPM1X enters in SWM. If BFR is cleared, the energy calculation is performed normally. When BFR is set (no voltage information is available), the energy computation is carried out using a nominal voltage value according to the NOM configuration bits.

Since there is no information on the phase shift between voltage and current, the apparent rather than active power is used for tamper and energy computation. The calculated apparent energy will be the product between I_{RMS} (effectively measured) and an equivalent V_{RMS} that can be calculated as follows:

V_{RMS}=VPK*K_{NOM}, where VPK represents the maximum line voltage reading of the STPM1X and K_{NOM} is a coefficient that changes according to *Table 11*:

Table 11. Nominal voltage values

NOM	K_{NOM}
0	0.3594
1	0.3906
2	0.4219
3	0.4531

For example, if R1 = 783kΩ and R2 = 475Ω are used as resistor divider when the line voltage is present, the positive voltage present at the input of the voltage channel of STPM1x is:

Equation 3

$$VI = \frac{R_2}{R_1 + R_2} \cdot V_{RMS}\sqrt{2}$$

since the maximum voltage value applicable to the voltage channel input of STPM1x is +0.3V, the equivalent maximum line voltage applicable is:

Equation 4

$V_{PK} = R_1+R_2/R_2 \bullet 0.3 = 494.82$

considering the case of NOM=2, the correspondent RMS values used for energy computation is:

Equation 5

$V_{RMS} = V_{PK} \bullet 0.4219 = 208.76$ [V]

Usually the supply voltage for the electronic meter is taken from the line voltage. In SWM, since the line voltage is no longer present, another power source must be used in order to provide the necessary supply to STPM1x and the other electronic components of the meter.

7.6 Power supply

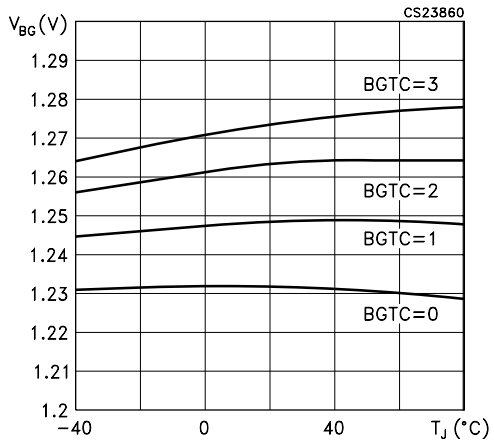
The main STPM1X supply pin is the V_{CC} pin. From the V_{CC} pin two linear regulators provide the necessary voltage for the analog part V_{DDA} (3 V) and for the digital part V_{DDD} (1.5 V). The V_{SS} pin represents the reference point for all the internal signals. The 100nF capacitor should be connected between V_{CC} and V_{SS}, V_{DDA} and V_{SS}, V_{DDD} and V_{SS}. All these capacitors must be located very close to the device.

The STPM1X contains a power-on-reset (POR) detection circuit. If the V_{CC} supply is less than 2.5 V, then the STPM1X goes into an inactive state, all the functions are blocked asserting and a reset condition is set. This is useful to ensure that the correct device operation at power-up and during power-down. The power supply monitor has built-in hysteresis and filtering, which give a high degree of immunity to false triggering due to noisy supply voltages.

A bandgap voltage reference (VBG) of 1.23 V ±1% is used as reference voltage level source for the two linear regulators and for the A/D converters. Also, this module produces several

bias currents and voltages for all other analog modules and for the OTP module. The bandgap voltage temperature behavior can be changed in order to better compensate the variation of sensor sensitivity with temperature. This task is performed with the BGTC configuration bits.

Figure 16. Bandgap temperature variation



7.7 Load monitoring

The STPM1X include a no-load condition detection circuit with adjustable threshold. This circuit monitors the voltage and the current channels and, when the measured power is below the set threshold, the internal signal BIL becomes high. The information about this signal is also available in the status bit BIL.

The no load condition occurs when the product between V_{RMS} and I_{RMS} input values is below a given value. This value can be set with the LTCH configuration bits, and it is also dependent on the selected current gain (Ai) and the calibration registers constant Kp=Kv*Ki.

Four different no-load threshold values can be chosen according to the two configurations bits LTCH (see *Table 12*).

Table 12. No load detection thresholds

LTCH	V_{RMS} * I_{RMS} (input channel voltages)	V_{RMS} * I_{RMS} (input channel voltages)
	Rogowski coil (PST<2)	Ct or Shunt (PST>1)
0	0.004488 / (Ai*Kp)	0.003648 / (Ai*Kp)
1	0.008976 / (Ai*Kp)	0.007296 / (Ai*Kp)
2	0.017952 / (Ai*Kp)	0.014592 / (Ai*Kp)
3	0.035904 / (Ai*Kp)	0.029184 / (Ai*Kp)

When a no-load condition occurs (BIL=1), the integration of power is suspended and the tamper module is disabled.

If a no-load condition is detected, the BIL signal blocks generation of pulses for stepper and forces the SCLNLC pin to be low.

7.8 Error detection

In addition to the no-load condition and the line frequency band, the integration of power can be suspended also due to detected error on the source signals.

There are two kinds of error detection circuits involved. The first checks all the $\sum \Delta$ signals from the analog part if any are stacked at 1 or 0 within the 1/128 of f_{CLK} period of observation. In case of detected error the corresponding $\sum \Delta$ signal is replaced with an idle $\sum \Delta$ signal, which represents a constant value 0.

Another error, condition occurs if the MOP, MON and LED pin outputs signals are different from the internal signals that drive them. This can occur if some of this pin is forced to GND or to some other imposed voltage value.

7.9 Tamper detection module (STPM13/14 only)

The STPM13/14 is able to measure the current in both live and neutral wires to implement an anti-tamper function. When a difference between the two measurements is detected, the STPM13/14 enters the tamper state. When there is a very small difference between the two channels, the STPM13/14 is in normal state.

In particular, both channels are not constantly observed. A time multiplex mechanism is used. During the observation time of the selected channel, its active energy is calculated. The detection of a tamper condition occurs when the absolute value of the difference between the two active energy values is greater than a certain percentage of the averaged energy during the activated tamper module. This percentage value can be selected between two different values (12.5% and 6.25%) according to the value of the configuration bit CRIT.

The tamper condition will be detected when the following formula is satisfied:

Equation 6

EnergyCH1 - EnergyCH2 > K_{CRIT} (EnergyCH1 + EnergyCH2)/2; where K_{CRIT} can be 12.5% or 6.25%.

The detection threshold is much higher than the accuracy difference of the current channels, which should be less than 0.1%. Some margin should be left for a possible transition effect, due to accidental synchronism between the actual load current change and the rhythm of taking the energy samples.

The tamper circuit works if the energies associated with the two current channels will be both positive or both negative. If the two energies have different signs, the tamper remains on constantly. However, the channel with the associated higher power is selected for the final computation of energy.

In single wire mode, the apparent energy rather than active is used for tamper detection.

Detailed operational description

Normal state

The meter is initially set to normal state, i.e. tamper not detected. In such state, we expect that the values of both load currents should not differ more than the accuracy difference of the channels. For this reason, we can use an average value of currents of both channels for the active energy calculation. The average is implemented with the multiplex ratio of 32:32 periods of line per channel. This means that for 32 periods of line voltage, i.e. 640 ms at 50 Hz, the current of the primary channel is used for the calculation followed by another 32

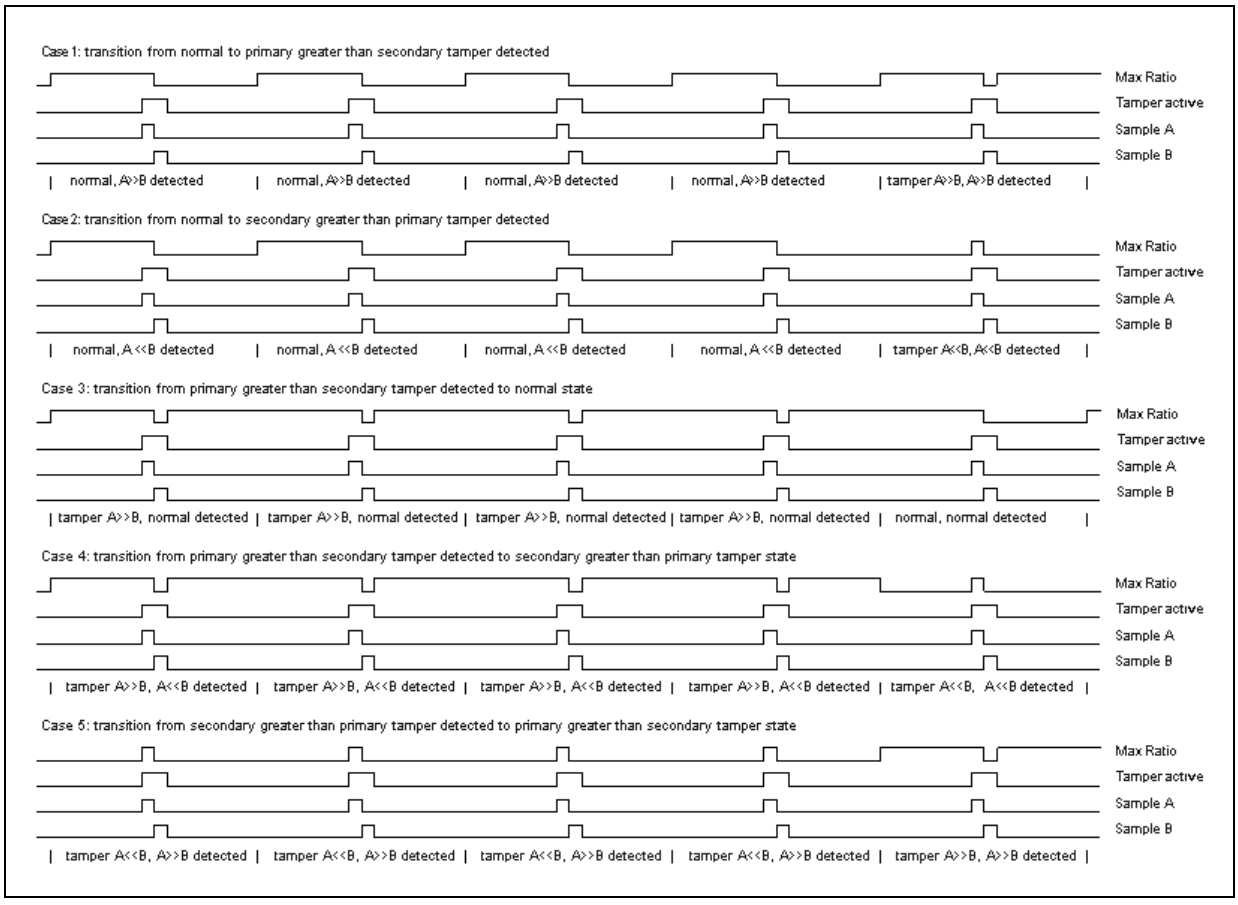
periods of line voltage when the current of secondary channel is used instead. Four periods before the primary to secondary switching point, a tamper detection module is activated. It is deactivated after eight periods of line have elapsed. This means that energy of four periods of primary channel immediately followed by energy of four periods of secondary channel is sampled within the tamper module. We shall call those samples A and B respectively. From these two samples the criteria of tamper detection is calculated. If four consecutive new results of criteria happen, i.e. after elapsed 5.12s at 50 Hz, the meter will enter into tamper state.

Tamper state

Within this state the multiplex ratio will change either to 60:4, when primary current is higher than secondary, or to 4:60 otherwise. Thus, the channel with the higher current is used in the energy calculation. The energy is not averaged by the mentioned ratio, rather the last measured higher current is used also during 4 line period gap. The gap is still needed in order to monitor the samples of the non-selected channel, which should check when the tamper detected state is changed to either normal or another tamper detected state.

Several cases of transition of the state are shown in the *Figure 17* - below

Figure 17. Tamper conditions



The detected tamper condition is stored in the BIT signal. This signal is connected to the SDA-TD pin. When this pin is low, a tamper condition has been detected.

When internal signals are not good enough to perform the computation, i.e. line period is out or range or $\sum\Delta$ signals from the analog part are stacked at high or low logic level, or no load condition is activated, the tamper module is disabled and its state is preset to normal.

7.10 Phase compensation

The STPM1X is does not introduce any phase shift between voltage and current channels.

However, the voltage and current signals come from transducers, which could have inherent phase errors. For example, a phase error of 0.1° to 0.3° is not uncommon for a current transformer (CT). These phase errors can vary from part to part, and they must be corrected in order to perform accurate power calculations. The errors associated with phase mismatch are particularly noticeable at low power factors. The STPM1x provide a means of digitally calibrating these small phase errors through a introducing delays on the voltage or current signal. The amount of phase compensation can be set using the 4 bits of the phase calibration register (CPH).

The default value of this register is at a value of 0 which gives 0° phase compensation. A CPH value of 15 (1111) introduces a phase compensation of +0.576°. This compensates the phase shift usually introduced by the current sensor, while the voltage sensor, normally a resistor divider, does not introduce any delay. The resolution step of the phase compensation is 0.038°.

7.11 Clock generator

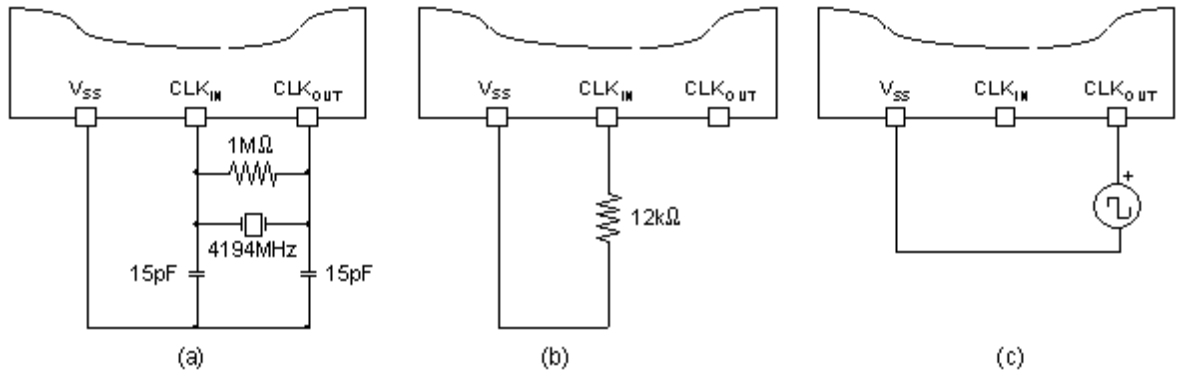
All the internal timing of the STPM1X is based on the CLKOUT signal. This signal is generated by different circuits according to the STPM1x version.

- STPM11/13: Internal RC Oscillator. A resistor connected between CLKIN and Ground will set the RC current. For 4 MHz operation the suggested settling resistor is 12 kΩ; The oscillator frequency can be compensated using the CRC configuration bit (see *Table 15* and *Figure 14*)
- STPM12/14: Quartz Oscillator. The oscillator circuit is designed to support an external crystal. The suggested circuit is depicted in *Figure 18*. These versions support also an external oscillator signal source that must be connected to the CLKOUT pin.

The clock generator is powered from analog supply and is responsible for two tasks. The first one is to retard the turn-on of some function blocks after POR in order to help smooth start of external power supply circuitry by keeping all major loads off.

The second task of the clock generator is to provide all necessary clocks for analog and digital parts. Within this task, the MDIV configuration bit is used to inform the device about the nominal frequency value of CLKOUT. The suggested operation frequency range is from 4.000 MHz to 4.194 MHz.

Figure 18. Different oscillator circuits (a); (b); (c)



STPM12/14 with quartz **STPM11/13** **STPM12/14 with external source**

7.12 Resetting the STPM1x

The STPM1x has no reset pin. The device is automatically reset by the POR circuit when the V_{CC} crosses the 2.5 V value. When the reset occurs, all clocks and both DC buffers in the analog part are kept off for about 30 ms and all blocks of the digital part are held in a reset state for about 125 ms after a reset condition.

Resetting the STPM1x causes all the functional modules of STPM1x to be cleared including the OTP shadow latches (see 7.15 for OTP shadow latches description)

7.13 Energy to frequency conversion

The STPM1x provides energy to frequency conversion both for calibration and energy readout purposes. In fact, one convenient way to verify the meter calibration is to provide a pulse train signal with 50% duty cycle whose frequency signal is proportional to the active energy under steady load conditions. It is convenient to have high frequency pulses during calibration phase and low frequency for readout purposes; STPM1x supports both cases. Let's suppose to choose a certain number of pulses on the LED pin (high frequency) that will corresponds to 1 kWh. We will name this value as P.

The Active Energy frequency-based signal is available in the LED pin. The LED is driven from internal signal AW (Active Energy) whose frequency is proportional to the active energy. The desired P is achieved acting on the digital calibrators during the calibration procedure.

The APL configuration bit changes the internal divider that provides the signal on the LED pin according to *Table 13*, setting APL=1 the number of pulses are reduced in order to provide low frequency pulses for readout purposes. The division factor is set according to KMOT configuration bits. In this case the pulses will have a fixed width of 31.25 ms.

Table 13. Different settings for led signal

KMOT (2 Bits)	APL=0	APL=1
	Pulses	Pulses
0	P	P/64
1		P/128
2		P/32
3		P/256

Due to the innovative and proprietary power calculation algorithm, the frequency signal is not affected by any ripple at twice the line frequency. This feature strongly reduces the calibration time of the meter.

7.14 Driving a stepper motor

The STPM1x is able to directly drive a stepper motor. An internal divider (mono-flop and decoder) generates stepper driving signals MA and MB from signal AW. The MA and MB signals are brought to the MOP and MON pins that are able to drive the stepper motor. Several kinds of selections are possible for the driving signals according to the configuration bits LVS and KMOT.

The numbers of pulses per kWh (PM) in the MOP and MON outputs are linked with the number of pulses of the LED P (see previous paragraph - *7.13*) pin with the following relationship.

Table 14. Configuration of MOP and MON pins

LVS (1 Bit)	KMOT (2 Bits)	Pulses length	PM
0	0	31.25 ms	P/64
0	1	31.25 ms	P/128
0	2	31.25 ms	P/32
0	3	31.25 ms	P/256
1	0	156.25 ms	P/640
1	1	156.25 ms	P/1280
1	2	156.25 ms	P/320
1	3	156.25 ms	P/2560

The mono-flop limits the length of the pulses according to the LVS bit value.

The decoder distributes the pulses to MA and MB alternatively, which means that each of them has only one half of selected frequency.

Negative power is computed with its own sign, and the MOP and MON signals invert their logic state in order to make the backward rotation direction of the motor. See the diagram below.