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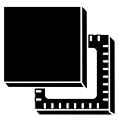
STPM32, STPM33, STPM34

ASSP for metering applications with up to four independent 24-bit 2nd order sigma-delta ADCs, 4 MHz OSF and 2 embedded PGLNA

Datasheet - production data

QFN24L 4x4x1



QFN32L 5x5x1

Features

- Active power accuracy:
  - <0.1% error over 5000: 1 dynamic range
  - <0.5% error over 10000: 1 dynamic range
- Exceeds 50-60 Hz EN 50470-x, IEC 62053-2x, ANSI12.2x standard requirements for AC watt meters
- Reactive power accuracy:
  - <0.1% error over 2000:1 dynamic range
- Dual mode apparent energy calculation
- Instantaneous and averaged power
- RMS and instantaneous voltage and current
- Under and overvoltage detection (sag and swell) and monitoring
- Overcurrent detection and monitoring
- UART and SPI serial interface with programmable CRC polynomial verification
- Programmable LED and interrupt outputs
- Four independent 24-bit 2nd order sigma-delta ADCs
- Two programmable gain chopper stabilized low-noise and low-offset amplifiers
- Bandwidth 3.6 kHz @ -3 dB
- V_{cc} supply range 3.3 V±10%
- Supply current I_{cc} 4.3 mA (STPM32)
- Input clock frequency 16 MHz, Xtal or external source
- Twin precision voltage reference: 1.18 V with independent programmable TC, 30 ppm/°C typ.
- Internal low drop regulator @ 3 V (typ.)
- QFN packages
- Operating temperature from 40 °C to +85 °C

Description

The STPM3x is an ASSP family designed for high accuracy measurement of power and energies in power line systems using the Rogowski coil, current transformer or shunt current sensors. The STPM3x provides instantaneous voltage and current waveforms and calculates RMS values of voltage and currents, active, reactive and apparent power and energies. The STPM3x is a mixed signal IC family consisting of an analog and a digital section. The analog section consists of up to two programmable gain low-noise low-offset amplifiers and up to four 2nd order 24-bit sigma-delta ADCs, two bandgap voltage references with independent temperature compensation, a low drop voltage regulator and DC buffers. The digital section consists of digital filtering stage, a hardwired DSP, DFE to the input and a serial communication interface (UART or SPI). The STPM3x is fully configurable and allows a fast digital system calibration in a single point over the entire current dynamic range.

Table 1. Device summary

Order code	Package	Packing
STPM34TR	QFN32L 5x5x1	Tape and reel
STPM33TR	QFN32L 5x5x1	Tape and reel
STPM32TR	QFN24L 4x4x1	Tape and reel

This is information on a product in full production. www.st.com

Contents

List of tables

List of figures

1 Schematic diagram

Figure 1. STPM34 block diagram

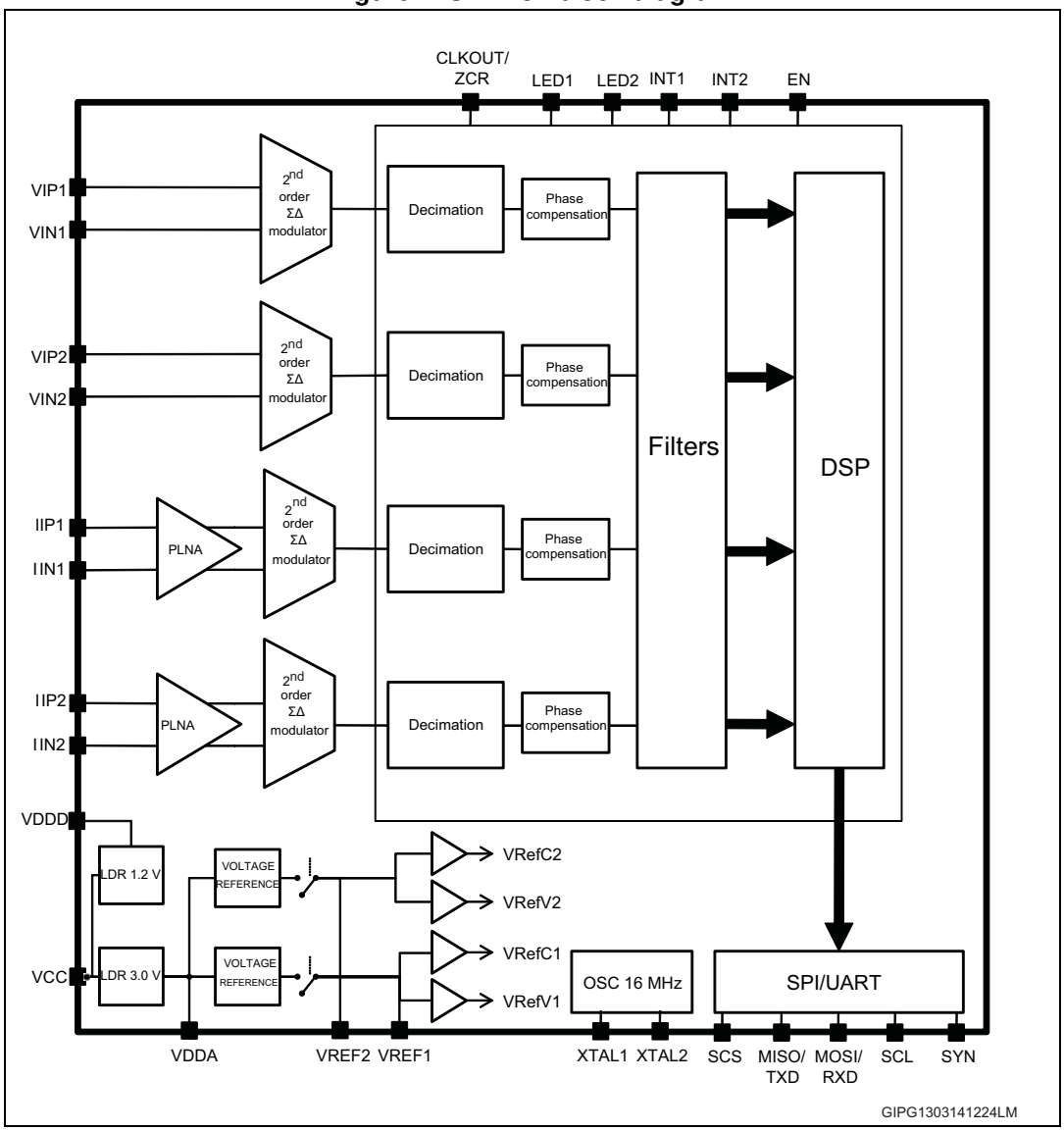


Figure 2. STPM33 block diagram

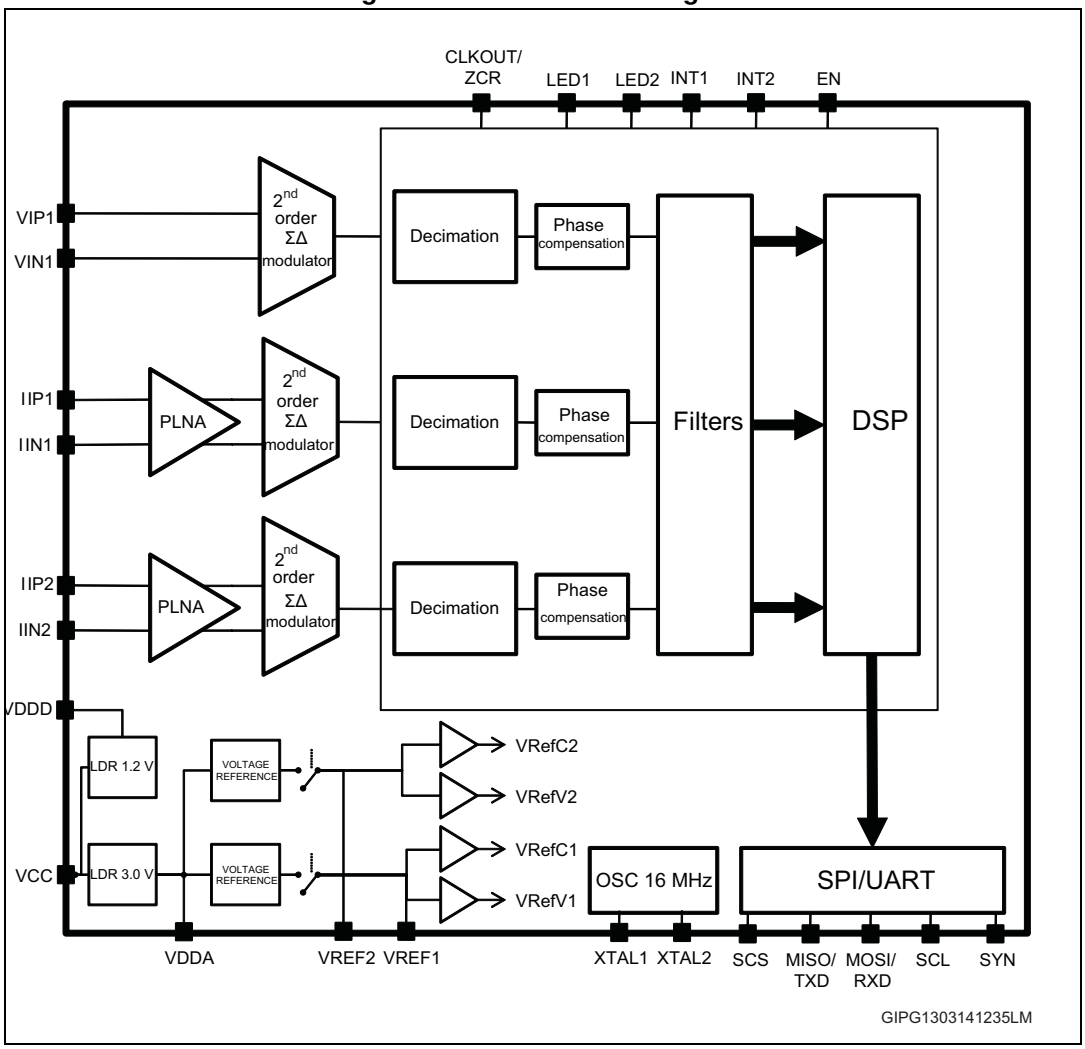
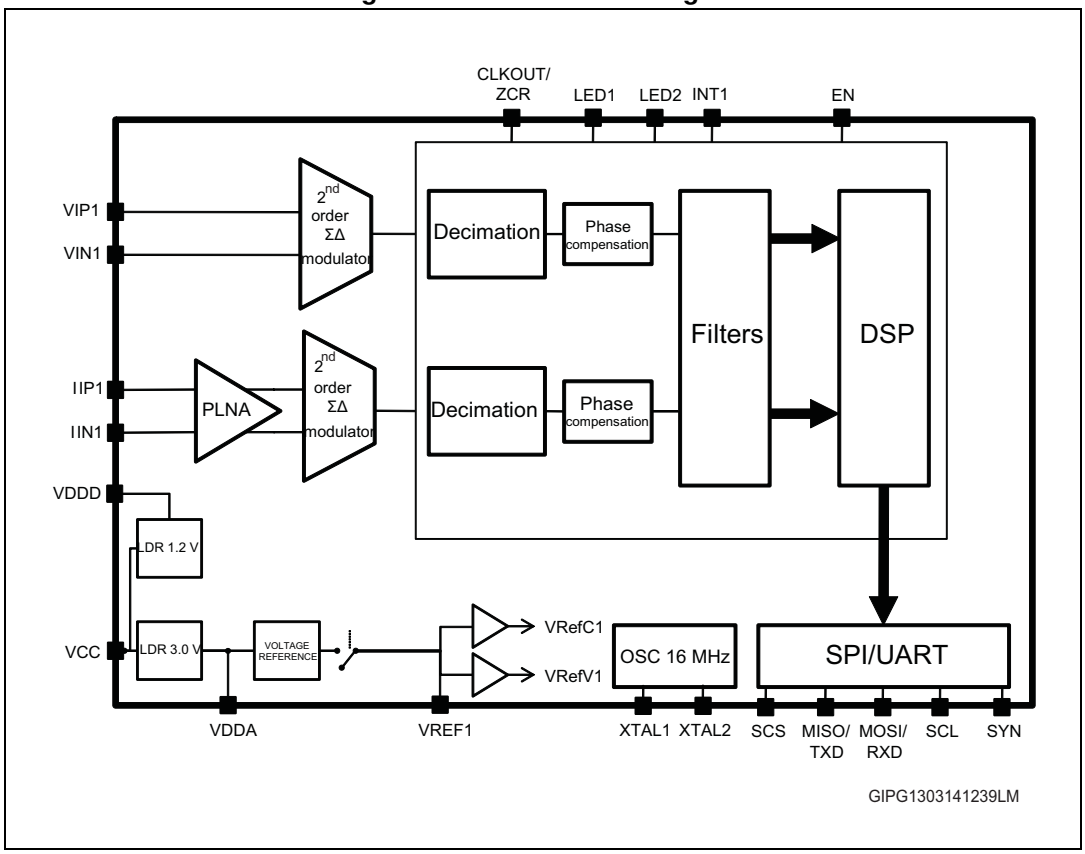


Figure 3. STPM32 block diagram



2 Pin configuration

Figure 4. STPM34 pinout (top view), QFN32L 5x5x1

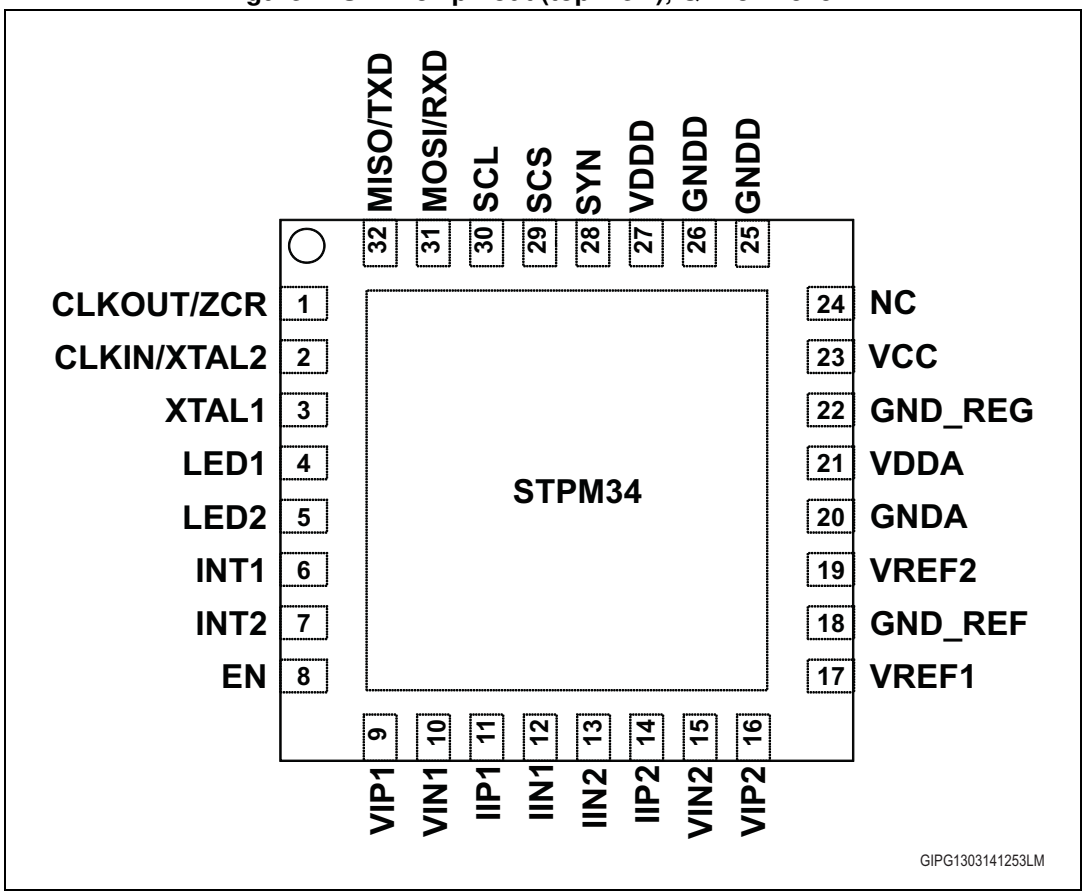


Figure 5. STPM33 pinout (top view), QFN32L 5x5x1

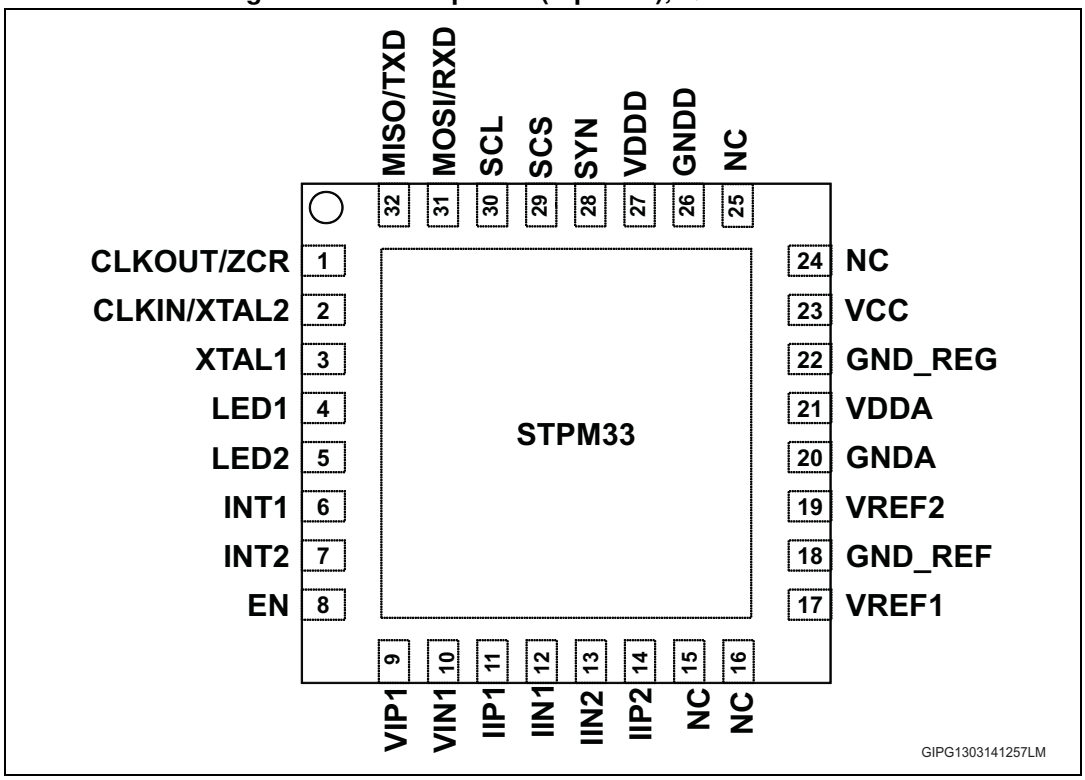


Figure 6. STPM32 pinout (top view), QFN24L 4x4x1

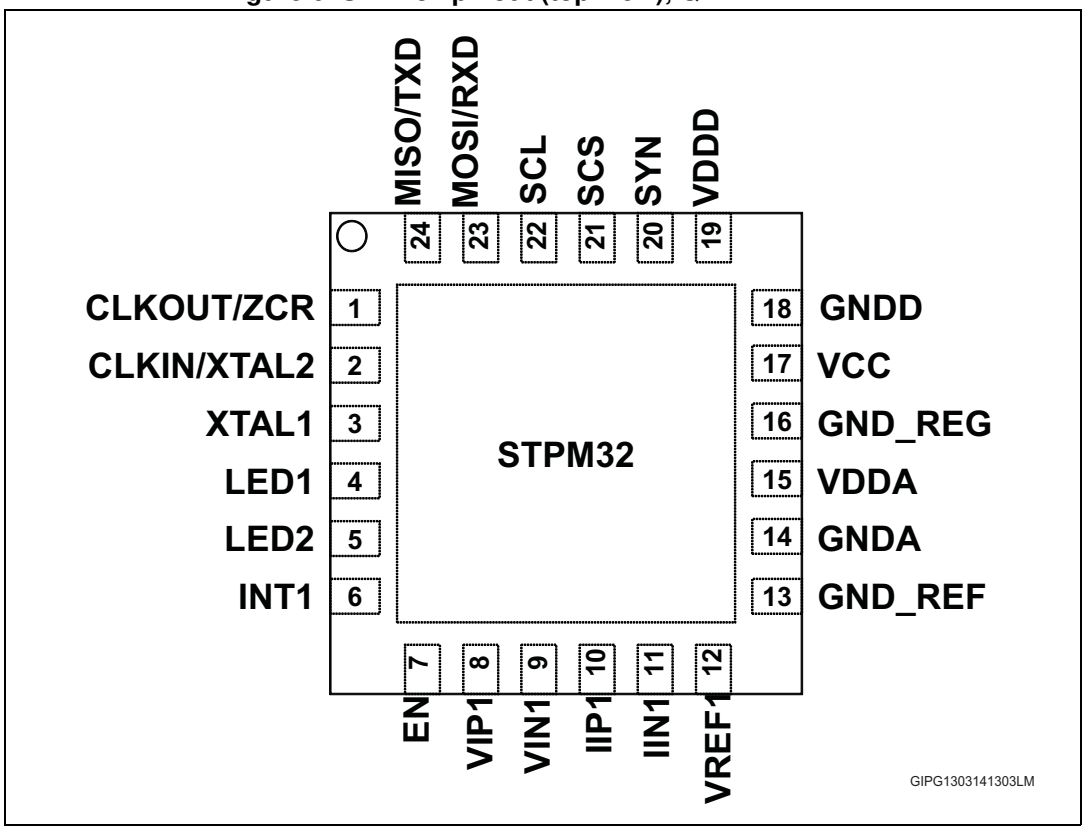


Table 2. STPM34, STPM33, STPM32 pin description

STPM34	STPM33	STPM32	Name	Description and multiplexed function	Voltage range	Functional section
1	1	1	CLKOUT/ZCR	-Zero-crossing output -System clock output	From 0 to V_{CC}	Multifunctional
2	2	2	CLKIN/XTAL2	-Input of external clock -External crystal input 2	From 0 to V_{CC}	Oscillator
3	3	3	XTAL1	-External crystal input 1	From 0 to V_{CC}	Oscillator
4	4	4	LED1	-Pulse output 1 -Primary current SD bitstream	From 0 to V_{CC}	Multifunctional
5	5	5	LED2	-Pulse output 2 -Secondary current SD bitstream	From 0 to V_{CC}	Multifunctional
6	6	6	INT1	-Interrupt 1 -Primary voltage SD bitstream	From 0 to V_{CC}	Multifunctional
7	7		INT2	-Interrupt 2 -Secondary voltage SD bitstream	From 0 to V_{CC}	Multifunctional
8	8	7	EN	Enable pin	From 0 to V_{CC}	Signal
9	9	8	VIP1	Positive voltage primary input	From -0.3 V to 0.3 V	Signal
10	10	9	VIN1	Negative voltage primary input	From -0.3 V to 0.3 V	Signal
11	11	10	IIP1	Positive current primary input	From -0.3 V to 0.3 V	Signal
12	12	11	IIN1	Negative current primary input	From -0.3 V to 0.3 V	Signal
13	13		IIN2	Negative current secondary input	From -0.3 V to 0.3 V	Signal
14	14		IIP2	Positive current secondary input	From -0.3 V to 0.3 V	Signal
15	-		VIN2	Negative voltage secondary input	From -0.3 V to 0.3 V	Signal
16	-		VIP2	Positive voltage secondary input	From -0.3 V to 0.3 V	Signal
17	17	12	VREF1	Output of voltage reference 1	From 1.16 V to 1.18 V	Power
18	18	13	GND_REF	Analog ground of VREF		Power
19	19		VREF2	Output of voltage reference 2	From 1.16 V to 1.18 V	Power
20	20	14	GNDA	Analog ground (shield)		Power

Table 2. STPM34, STPM33, STPM32 pin description (continued)

STPM34	STPM33	STPM32	Name	Description and multiplexed function	Voltage range	Functional section
21	21	15	VDDA	Output of voltage regulator	3.0 V	Power
22	22	16	GND_REG	Ground		Power
23	23	17	VCC	Voltage supply	From 3.0 V to 3.6 V	Power
24	15, 16, 24, 25	-	NC	Not connected		
25, 26	26	18	GNDD	Digital ground		Power
27	27	19	VDDD	Output of voltage regulator	1.2 V	Power
28	28	20	SYN	Synchronization pin	From 0 to V_{CC}	SPI
29	29	21	SCS	Chip-select SPI/UART select	From 0 to V_{CC}	SPI/UART
30	30	22	SCL	SPI clock	From 0 to V_{CC}	SPI
31	31	23	MOSI/RXD	SPI master OUT slave IN UART RX	From 0 to V_{CC}	SPI/UART
32	32	24	MISO/TXD	SPI master IN slave OUT UART TX	From 0 to V_{CC}	SPI/UART

3 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC input voltage	-0.3 to 4.2	V
V_{ID}	Any pin input voltage	-0.3 to V_{CC} + 0.3	V
V_{IA}	Analog pin input voltage (VIP, VIN, IIP, IIN)	-0.7 to 0.7	V
ESD	Human body model (all pins)	±2	kV
I_{LATCH}	Current injection latch-up immunity	100	mA
T_{OP}	Operating junction temperature range	-40 to 85	°C
T_j	Junction temperature	-40 to 150	°C
T_{STG}	Storage temperature range	-55 to 150	°C

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. All values are referred to GND.

Table 4. Thermal data

Symbol	Parameter	Package	Value	Unit
R_{thJA}	Thermal resistance junction-ambient	QFN32L 5x5x1	30	°C/W
		QFN24L 4x4x1	20	

Note: This value is referred to single-layer PCB, JEDEC standard test board.

4 Electrical characteristics

V_{CC} = 3.3 V, C_L=1 µF between V_{DDA} and GNDA, C_L = 4.7 µF between V_{DDD} and GNDD, C_L= 1 µF between V_{CC} and GND, C_L = 100 nF between VREF1, 2 and GNDREF, F_{CLK} = 16 MHz, T_{AMB} = 25 °C, EN = V_{CC}, SPI/UART not used, unless otherwise specified.

Table 5. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
General section						
V_{CC}	Operating supply voltage		2.95	3.3	3.65	V
I_{CC}	Operating current	STPM32		4.3		mA
		STPM33		5.0		
		STPM34		5.9		
		STPM34 Primary channel ON: ENVREF1 = 1, enV1 = enC1 = 1 Secondary channel OFF: ENVREF2 = 0, enV2 = enC2 = 0		4.5		
		STPM34 Primary current channel ON only: ENVREF1 = 1, enV1 = 0, enC1 = 1 Secondary channel OFF: ENVREF2 = 0, enV2 = enC2 = 0		4.0		
F_{CLK}	Nominal frequency			16		MHz
Power management (VDDA, VDDD, GNDA, GNDD, GND_REG, EN)						
V_{POR}	Power-on-reset on V_{CC}			2.5		V
I_{STBY}	Standby current consumption	EN=GND		<1		uA
V_{DDA}	Analog regulated voltage			2.85		V
V_{DDD}	Digital regulated voltage			1.2		V
$PSRR_{REGS}$	Power supply rejection ratio (1)	50 Hz		50		dB
On-chip reference voltage (VREF1, VREF2)						
V_{REF}	Reference voltage	No load on V_{REF}, T_C = 010 (default)		1.18		V
T_C	Temperature coefficient(2)	Default		30		ppm/°C
T_{Cstep}	TC programmable step(2)			±30		ppm/°C

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Analog inputs (VIP1, VIN1, VIP2, VIN2, IIP1, IIN1, IIP2, IIN2)						
V_{MAX}	Maximum input signal levels	Voltage channels (VIP1-VIN1, VIP2-VIN2)	-300		+300	V
		Current channels (IIP1-IIN1, IIP2-IIN2) Gain 2X Gain 4X Gain 8X Gain 16X	 -300 -150 -75 -37.5		 +300 +150 +75 +37.5	mV
V_{off}	Amplifier offset(2)	Shorted and grounded input		1		mV
Z_{Vin}	Voltage channel input impedance(1)			8		MΩ
Z_{Iin}	Current channel input differential impedance(1)	Gain 2X Gain 4X Gain 8X Gain 16X		90 170 300 510		kΩ
G_{ERR}	Channel gain error	Input $V_{MAX}/2$		±5		%
	Crosstalk(1)	Voltage to current channels		-120		dB
		Current to voltage channels		-120		
Digital I/O (CLKOUT/ZCR, XTAL1, *CLKIN*/XTAL2, LED1, LED2, INT1, INT2)						
V_{IH}	Input high-voltage		0.75 V_{CC}		3.3	V
V_{IL}	Input low-voltage	V_{CC} = 3.2 V	-0.3		0.6	V
V_{OH}	Output high-voltage	I_O = -1 mA, C_L= 50 pF, V_{CC} = 3.2 V	V_{CC}-0.4			V
V_{OL}	Output low-voltage	I_O = +1 mA, C_L= 50 pF, V_{CC} = 3.2 V			0.4	V
Energy measurement accuracy						
AP	Active power	Over dynamic range 5000:1 PGA = 2 to 16		0.1		%
		Over dynamic range 10000:1 PGA = 2 to 16		0.5		
RP	Reactive power	Over dynamic range 2000:1 PGA = 2 to 16		0.1		
RMS	Voltage RMS	Over dynamic range 1:200		0.5		%
	Current RMS	Over dynamic range 1:500		0.5		
f_{BW}	Effective bandwidth	-3 dB, HPF = 1	4		3600	Hz
Sigma-delta ADC performance						
OSF	Oversampling frequency			4		MHz
DR	Decimation ratio			1/512		

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
F_s	Sampling frequency			7.8125		kHz
FBW	Flat band	<0.05 dB allowed ripple	2			kHz
BW	Effective bandwidth	-3 dB, HPF=0	0		3600	Hz
DC measurement accuracy						
$PSRR_{AC}$	Power supply AC rejection(2)	Voltage input shorted Current input shorted V_{CC} = 3.3 V±150 mVp @ 1 kHz		65		dB
SPI timings(3)						
t_en	Time between selection and clock		50			ns
t_clk	Clock period		50			ns
t_cpw	Clock pulse width		25			ns
t_setup	Set-up time before slave sampling		10			ns
t_hold	Hold time after slave sampling		40			ns
tpZL	Enable to low level time	V_{CC} = 3.3 V± 10%, V_{IN} = 0 to 3 V, 1 MHz, Rise time = fall time = 6 ns RL = 1 kΩ, CL = 50 pF see *Figure 10*		25		ns
tpLZ	Disable from low level time			15		ns
UART timings(3)						
t_1		CS enable to RX start	5			ns
t_2		Stop bit to CS disable	1			µs
t_3		CS disable to TX idle hold time			250	ns
tpZH	Enable to high level time	V_{CC} = 3.3 V± 10%, V_{IN} = 0 to 3 V, 1 MHz, Rise time = fall time = 6 ns RL = 1 kΩ, CL = 50 pF see *Figure 10*		21		ns
tpHZ	Disable from high level time			11		ns
SYN timings(3)						
t_ltch	Time between de-selection and latch		20			ns
t_lpw	Latch pulse width		4			µs
t_w	Time between two consecutive latch pulses		4			µs

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_rpw	Reset pulse width		4			µs
t_rel	Time between pulse and selection		40			ns

1. Guaranteed by design.
2. Guaranteed by characterization.
3. Guaranteed by application.

Figure 7. SPI timings

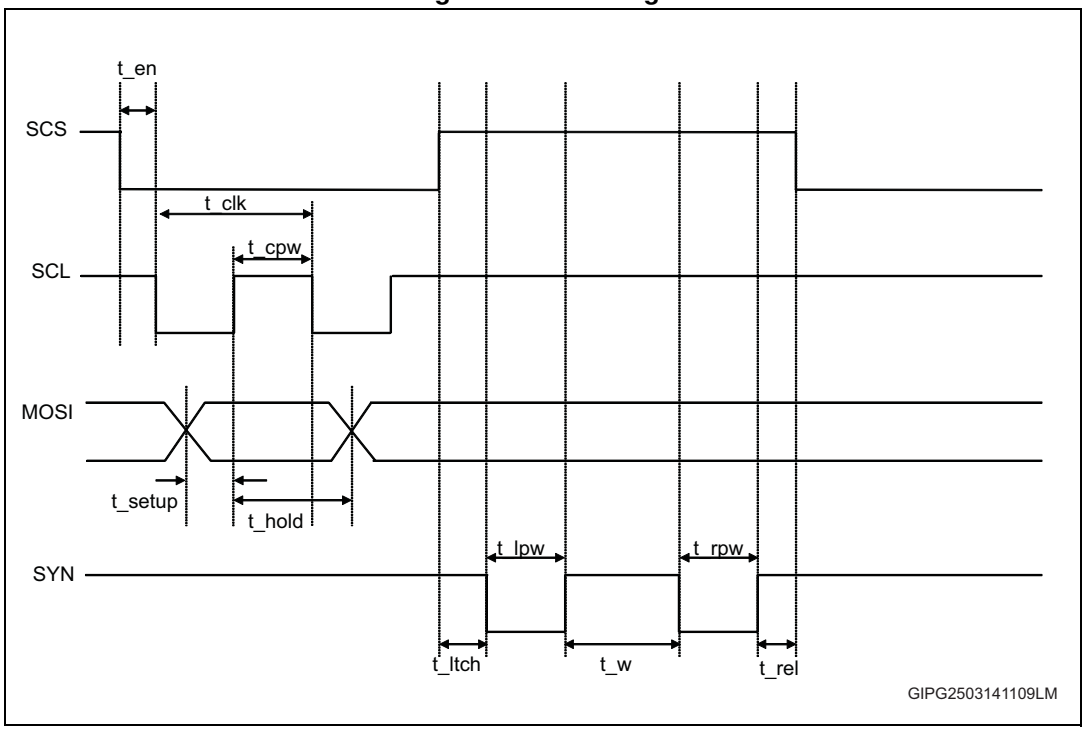


Figure 8. SPI enable and disable timing diagrams

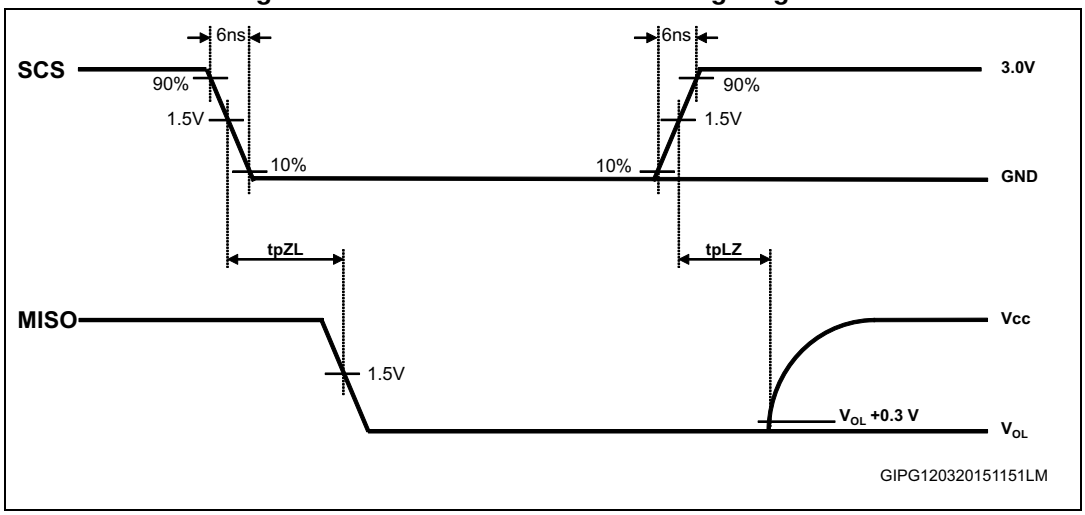


Figure 9. UART enable and disable timing diagrams

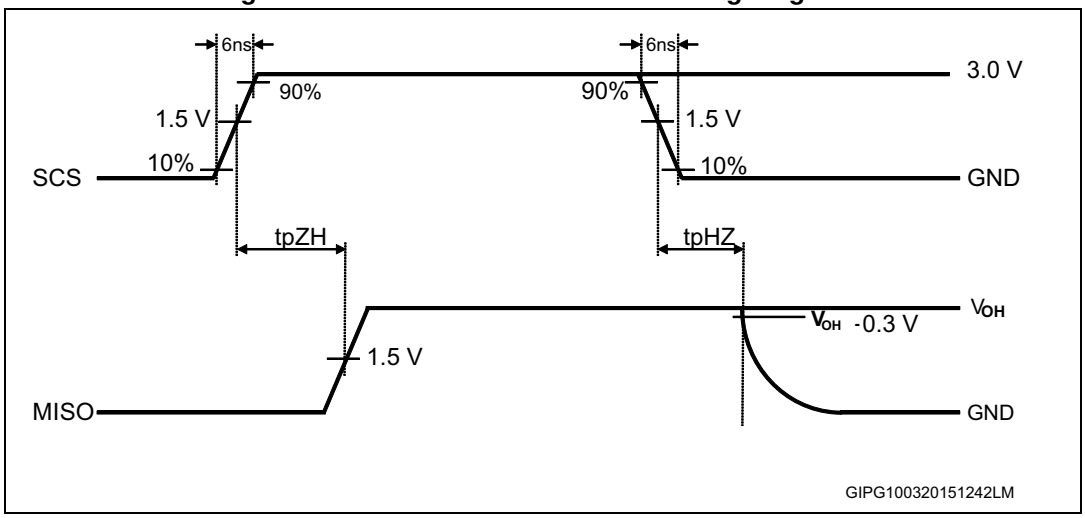
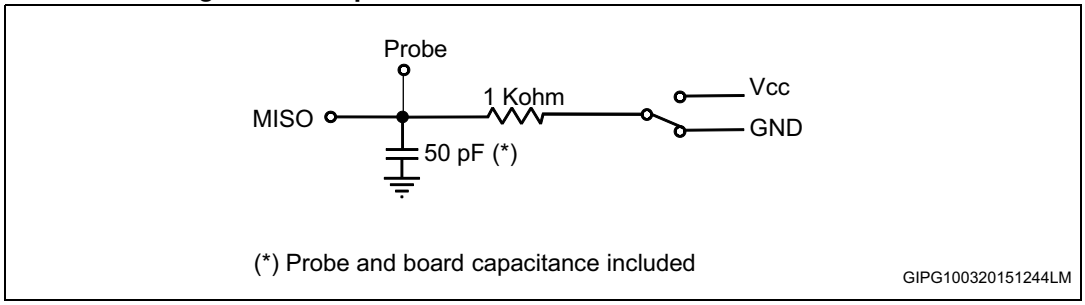


Figure 10. Output load circuit for enable and disable times



4.1 Pin programmability

Table 6. Programmable pin functions

Name	Multiplexed function	Functional description	I/O
CLKOUT/ZCR	System clock signal	Clock signals (*DCLK, SCLK, MCLK, CLKIN*)	Output
	Zero-crossing	Line voltage/current zero-crossing	
LED1	Programmable pulse 1	Primary channel energies (A, AF, R, S)(1)	Output
		Secondary channel energies (A, AF, R, S)	
		Primary ± secondary channel energies (A, AF, R, S)	
	SD out current (DATI1)	Sigma-delta bitstream of primary current channel	
LED2	Programmable pulse 2	Primary channel energies (A, AF, R, S)	Output
		Secondary channel energies (A, AF, R, S)	
		Primary ± secondary channel energies (A, AF, R, S)	
	SD current (DATI2)	Sigma-delta bitstream of secondary current channel	
INT1	Interrupt	Programmable interrupt 1	Output
	SD voltage (DATV1)	Sigma-delta bitstream of primary voltage	
INT2	Interrupt	Programmable interrupt 2	Output
	SD out voltage (DATV2)	Sigma-delta bitstream of secondary voltage	
SCS	SPI/UART select	Serial port selection at power-up	Output
	Chip-select	SPI/UART chip-select	
MOSI/RXD	SPI master OUT slave IN	SPI	Input
	UART RX	UART	
MISO/TXD	SPI master IN slave OUT	SPI	Output
	UART TX	UART	

1. A: active wideband; AF: active fundamental; R: reactive; S: apparent.

5 Typical application example

Figure 11 below shows the reference schematic of an application with the following properties:

- Constant pulses C_P = 41600 imp/kWh
- I_{NOM} = 5 A
- I_{MAX} = 90 A

Typical values for current sensor sensitivity are indicated in *Table 7*.

For more information about the application dimensioning and calibration please refer to *Section 9*.

Figure 11. STPM34 application schematic

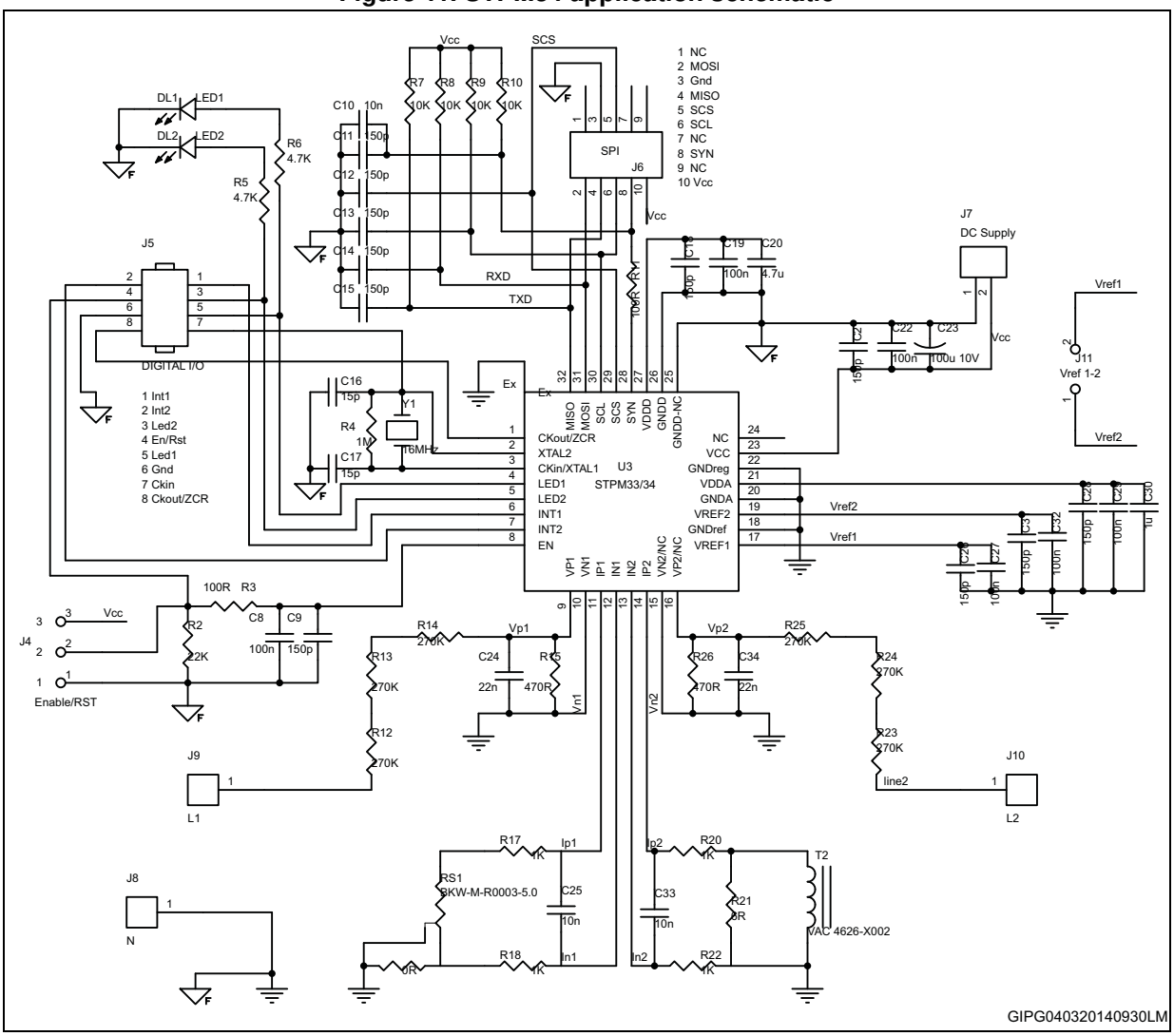


Table 7. Suggested external components in metering applications

Function	Component	Description	Value	Tolerance		Unit
Line voltage interface	Resistor divider	R to R ratio V_{RMS}=230 V	1:1650	±± 1%	50 ppm/°C	V/V
		R to R ratio V_{RMS}=110 V	1:830			
Line current interface	Rogowski coil	Current-to-voltage ratio k_S	0.15	±± 5%	50 ppm/°C	mV/A
	CT		2.4	±± 5%		
	Shunt		0.3	±± 5%		

Note: Above listed components refer to typical metering applications. The STPM3x operation is not limited to the choice of these external components.