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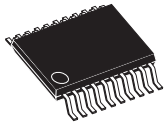
STPMC1

Programmable poly-phase energy calculator IC

Datasheet – production data

Features

- Supports 1-, 2- or 3-phase WYE and Delta services, from 2 to 4 wires
- Computes cumulative active and reactive wide-band and fundamental harmonic energies
- Computes active and reactive energies, RMS and momentary voltage and current values for each phase
- Supports Rogowski coil, current transformer, Shunt or Hall current sensors
- Exclusive ripple-free energy calculation algorithm
- Programmable pulsed output
- Stepper motor outputs
- Neutral current, temperature, and magnetic field monitoring
- OTP memory for configuration and calibration
- SPI interface
- Supports IEC 62052-11 / 62053-21 / 62053-23 standards
- Less than 0.1 % error over 1:1000 dynamic range



TSSOP20

Applications

- Power metering

Description

The STPMC1 device functions as an energy calculator and is an ASSP designed for effective energy measurement in power line systems utilizing Rogowski, current transformer, Shunt or Hall current sensors. Used in combination with one or more STPMSx ICs, it implements all the functions needed in a 1-, 2- or 3-phase energy meter. It can be coupled with a microprocessor for multi-function energy meters, or it can directly drive a stepper motor for a simple active energy meter. The calculator has five input data pins. The first three receive the voltage and current information of the phases. In fact, each data input processes two ΔΣ signals, multiplexed in time and generated by the STPMSx device. The fourth input receives multiplexed ΔΣ signals also, and can be used to sense the neutral current or another signal - temperature, for example. The fifth input data pin accepts non-multiplexed ΔΣ signals and it can be used for sensing the magnetic field information from a Hall sensor. Four internal hard-wired DSP (digital signal processing) units perform all the computations on the ΔΣ streams in real time by means of ΔΣ arithmetic blocks. This allows the achievement of very high computation precision with fast and efficient digital architecture. All the data recorded by the STPMC1 are accessible through an SPI port, which is also used to configure and calibrate the device. The configuration and calibration data can be saved in a 112-bit OTP block, or dynamically set in microprocessor-based meters.

Table 1. Device summary

Order code	Temperature range	Package	Packaging
STPMC1BTR	- 40 to 85 °C	TSSOP20 (tape and reel)	2500 parts per reel

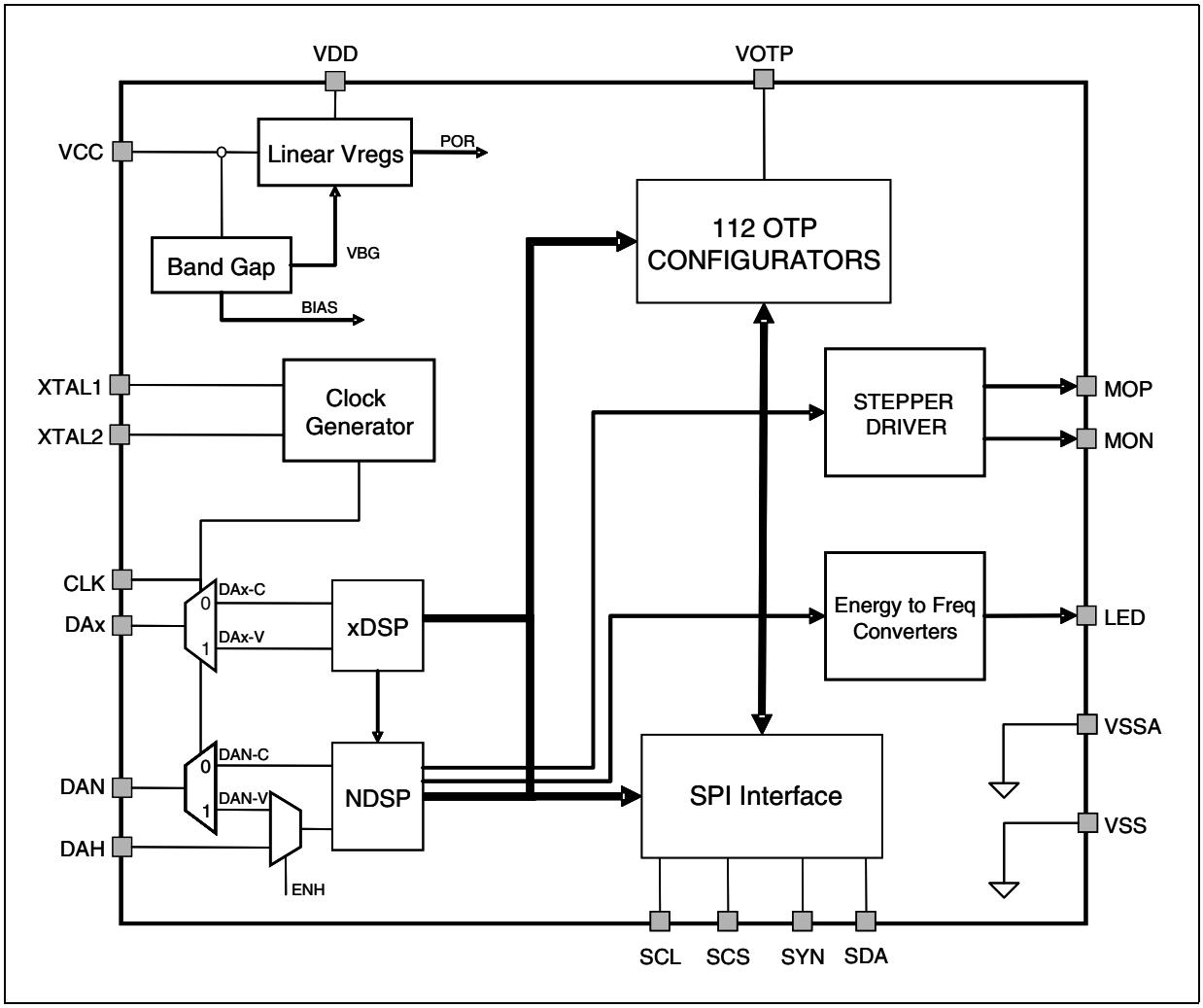
Contents

List of tables

List of figures

1 Functional block diagram

Figure 1. STPMC1 device block diagram



Note: DAx stands for DAR, DAS, DAT, and xDSP stands for RDSP, SDSP, TDSP.

2 Pin configuration

Figure 2. Pin connections (top view)

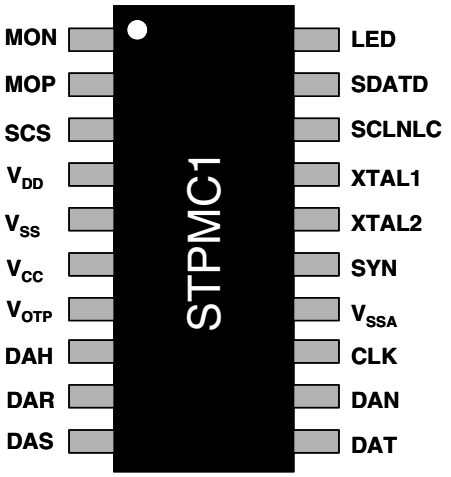


Table 2. Pin description

Pin n°	Symbol	Type (1)	Name and function
1	MON	D / P O	Programmable output pin, see *Table 5*
2	MOP	D / P O	Programmable output pin, see *Table 5*
3	SCS	D I	Digital input pin, see *Table 5*
4	V_{DD}	A O	1.8 V output of internal low drop regulator which supplies the digital core
5	V_{SS}	A GND	Ground level for pad-ring and power supply return
6	V_{CC}	P I	Supply voltage
7	V_{OTP}	P I	Supply voltage for OTP cells
8	DAH	D I	Input for non-multiplexed ΔΣ signals
9	DAR	D I	Input for multiplexed ΔΣ R-phase signals
10	DAS	D I	Input for multiplexed ΔΣ S-phase signals
11	DAT	D I	Input for multiplexed ΔΣ T-phase signals
12	DAN	D I	Input for multiplexed ΔΣ PTAT and neutral signal
13	CLK	D O	2 mA clock output for STPMSx devices
14	V_{SSA}	A GND	Ground level of core
15	SYN	D I/O	Programmable input/output pin, see *Table 5*
16	XTAL2	A	Crystal oscillator pin
17	XTAL1	A	Crystal oscillator pin
18	SCLNLC	D I/O	Programmable input/output pin, see *Table 5*
19	SDATD	D I/O	Programmable input/output pin, see *Table 5*
20	LED	D O	Programmable output pin, see *Table 5*

1. A: Analog, D: Digital, P: Power, I: Input, O: Output, GND: Ground

3 Maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC input voltage	- 0.3 to 6	V
I_{PIN}	Current on any pin (sink/source)	± 150	mA
V_{ID}	Input voltage at all pins	-0.3 to V_{CC} + 0.3	V
V_{OTP}	Input voltage at OTP pin	- 0.3 to 25	V
ESD	Human body model (all pins)	± 3.5	kV
T_{OP}	Operating ambient temperature	- 40 to 85	°C
T_J	Junction temperature	- 40 to 150	°C
T_{STG}	Storage temperature range	- 55 to 150	°C

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

Table 4. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction-ambient	114.5 (1)	°C/W

1. This value refers to single-layer PCB, JEDEC standard test board.

4 Functions

Table 5. Programmable pin functions

Programmable pin	Standalone mode (APL = 2 or 3)	Peripheral mode (APL = 0 or 1)
MON	Output for stepper node (MB) - charge pump	Watchdog reset
MOP	Output for stepper node (MA) - charge pump	*ZCR* signal
LED	3-phase energy pulsed output	Programmable energy pulsed output
SCLNLC	No load indicator	SPI interface
SDATD	Tamper indicator	
SYN-NP	Negative power indicator	
SCS	SPI data transmission enable	

5 Application

Figure 3. Application schematic in standalone operating mode

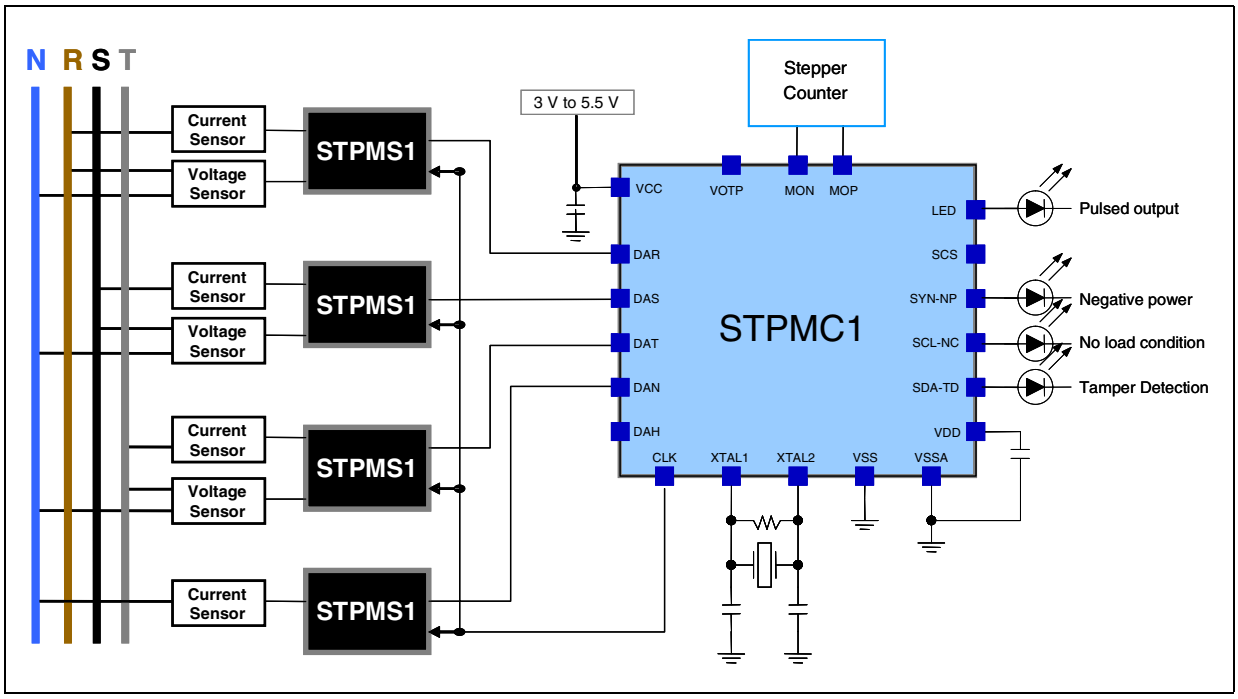


Figure 4. Application schematic using an MCU

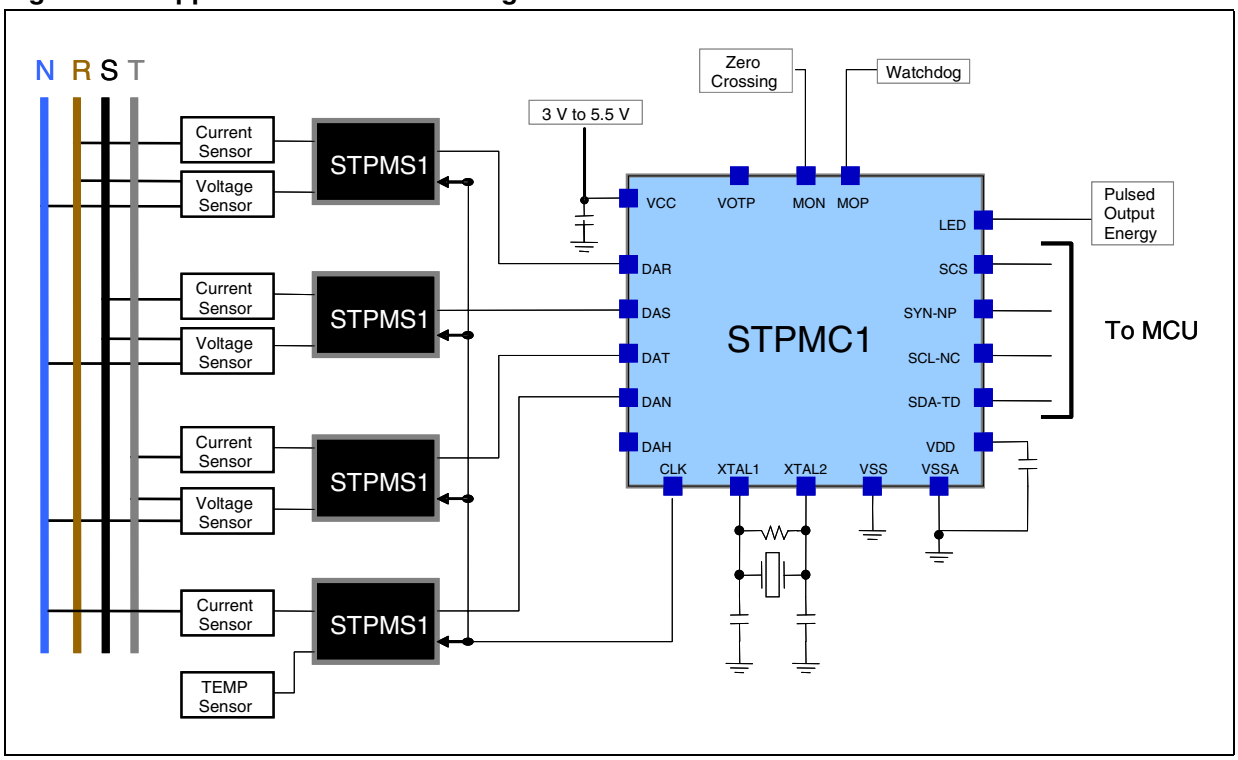


Table 6. Typical external components

Function	Component	Value	Tolerance	Unit
Reads or writes to a calculator device via SPI and performs computation	Microprocessor	---	---	---
Measurement reference clock	Crystal oscillator	4.194 8.192 4.915 9.830	± 30 ppm	MHz
Interface R-phase voltage, current	STPMSx	---	---	---
Interface S-phase voltage, current	STPMSx	---	---	---
Interface T-phase voltage, current	STPMSx	---	---	---
Interface PTAT, neutral current	STPMSx	---	---	---
Interface PTAT or hall	STPMSx	---	---	---
Low-end user interface	Stepper counter			

Note: The components listed above refer to a typical metering application. In any case, STPMC1 operation is not limited to the choice of these external components.

6 Electrical characteristics

(V_{CC} = 5 V, T_A= - 40 to + 85 °C, 100 nF across V_{CC} and V_{SS}; 1 µF across V_{DD} and V_{SSA}, unless otherwise specified).

Table 7. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Energy measurement accuracy						
f_{BW}	Effective bandwidth	Limited by digital filtering	5		400	Hz
General Section						
V_{CC}	Operating supply voltage		3.17		5.5	V
I_{CC}	Supply current. Configuration registers cleared or device locked	f_{XTAL1} =4.194MHz; V_{CC}=3.2V; C_L=100nF; no loads	5	6	7	mA
ΔI_{CC}	Increase of supply current per configuration bit, during programming	f_{XTAL1} =4.194MHz; V_{CC}=3.2V		100		µA/bit
POR	Power on reset on V_{CC}	f_{XTAL1} =4.194MHz		2.5		V
V_{DD}	Digital supply voltage		1.70	1.80	1.90	V
V_{OTP}	OTP programming voltage		14		20	V
I_{OTP}	OTP programming current per bit	Single bit programming		5		mA
t_{OTP}	OTP programming time per bit	Single bit programming		500		µs
I_{LATCH}	Current injection latch-up immunity				300	mA
Digital I/O (DAH, DAR, DAS, DAT, DAN, CLK, SDA, SCS, SYN, LED)						
V_{IH}	Input high voltage	Other pins	0.75V_{CC}			V
V_{IL}	Input low voltage	Other pins			0.25V_{CC}	V
V_{OH}	Output high voltage	I_O=-2mA	V_{CC}-0.4			V
V_{OL}	Output low voltage	I_O=+2mA			0.4	V
I_{UP}	Pull up current			15		µA
t_{TR}	Transition time	C_{LOAD}=50pF, V_{CC} =5V		10		ns
Power I/O (MOP, MON)						
V_{OH}	Output high voltage	I_O=-16mA	0.9V_{CC}			V
V_{OL}	Output low voltage	I_O=+16mA			0.1V_{CC}	V
t_{TR}	Transition time	C_{LOAD}=50pF, V_{CC} =5V		10		ns

Table 7. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Crystal oscillator						
V_{IH}	Input high voltage		1.2			V
V_{IL}	Input low voltage				0.6	V
I_{in}	Input current on XTAL2	V_{CC} =5.3V	-1		+1	µA
R_p	External resistor		1		4	MΩ
C_p	External capacitors			22		pF
f_{XTAL1}	Nominal output frequency		4.000	4.194	4.915	MHz
			8.000	8.192	9.830	
f_{MCLK}	Internal clock frequency	see *Table 10*	8.000	8.192	9.830	MHz
f_{CLK}	Output CLK pin frequency	HSA = 0		$f_{XTAL1}/4$		MHz
		HSA = 1		$f_{XTAL1}/2$		
SPI interface timing						
F_{SCLKr}	Data read speed	T_A= 25°C			32	MHz
F_{SCLKw}	Data write speed	T_A= 25°C			100	kHz
t_{DS}	Data setup time			20		ns
t_{DH}	Data hold time			0		ns
t_{ON}	Data driver on time			20		ns
t_{OFF}	Data driver off time			20		ns
t_{SYN}	SYN active width			$2/f_{XTAL1}$		s

Note: Typical value, not production tested.

7 Terminology

7.1 Measurement error

The error associated with the energy measured by the STPMC1 is defined as:

$$\text{Percentage Error} = \frac{\text{SPMC1(reading)} - \text{True Energy}}{\text{True Energy}}$$

7.2 Conventions

The lowest analog and digital power supply voltage is called V_{SS} which represents the system ground (GND). All voltage specifications for digital input/output pins are referred to GND.

Positive currents flow into a pin. “Sinking current” is the current flowing into the pin, and so it is positive. “Sourcing current” is the current flowing out of the pin, and so it is negative.

Signal timing specifications treated by a digital control part are relative to XTAL1. This signal is provided from the crystal oscillator or from an external source as specified in paragraph *9.4*.

Signal timing specifications of the SPI interface are relative to the SCLNLC. There is no direct relationship between the clock (SCLNLC) of the SPI interface and the clock of the DSP block (XTAL1).

A positive logic convention is used in all equations.

7.3 Notation

Table 8. Notation

Label	Description
u	Voltage
i	Current
u_X	Phase X voltage (X = R, S, T)
i_X	Phase X current (X = R, S, T)
i_N	Neutral current
U_X	Phase X RMS voltage (X = R, S, T)
I_X	Phase X RMS current (X = R, S, T)
P	Active energy full bandwidth
F	Active energy fundamental
Q	Reactive energy full bandwidth
R	Reactive energy fundamental
X_Y	X energy type per Y phase X = P, F, Q, R Y = R, S, T or Σ for 3-phase
PIN	Pin names are UPPERCASE
CFG	Configuration bit names are UNDERLINED
SIG	Internal signals and status bits are in *ITALICS*

8 Typical performance characteristics

Figure 5. Supply current vs. supply voltage, T_A = 25°C (f_{XTAL1} = 4.194 MHz, f_{XTAL1} = 8.192 MHz)

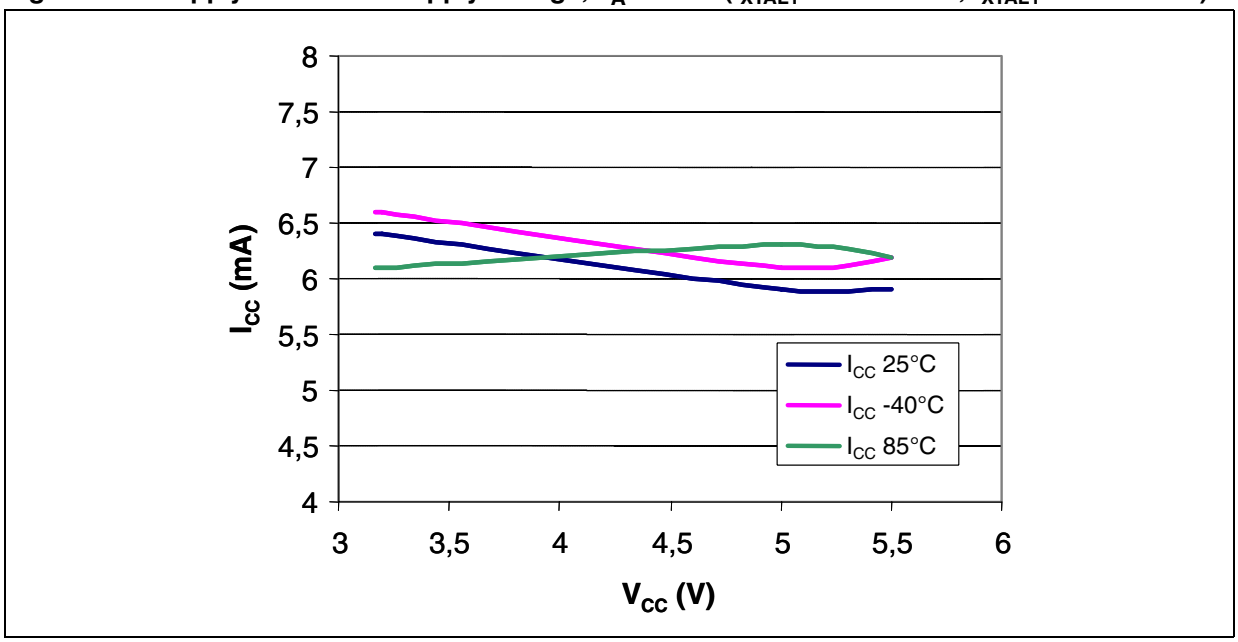


Figure 6. Digital voltage regulator: line - load regulation. (f_{XTAL1} = 0; 100 nF across V_{CC} and V_{SS}; 1 µF across V_{DD} and V_{SSA}; T_A = 25 °C)

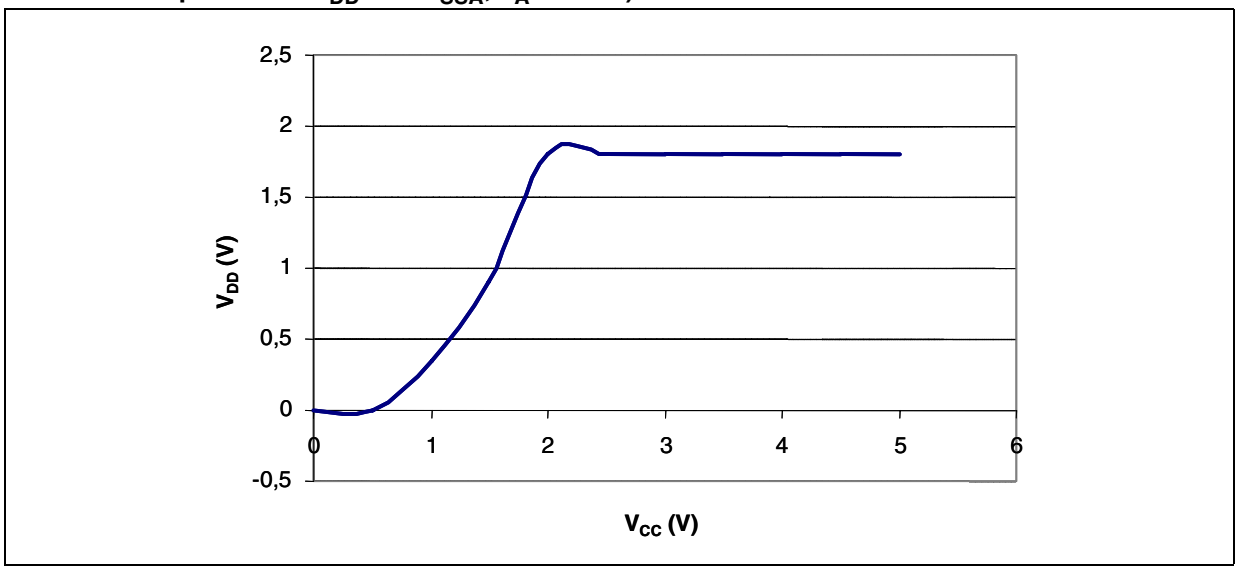
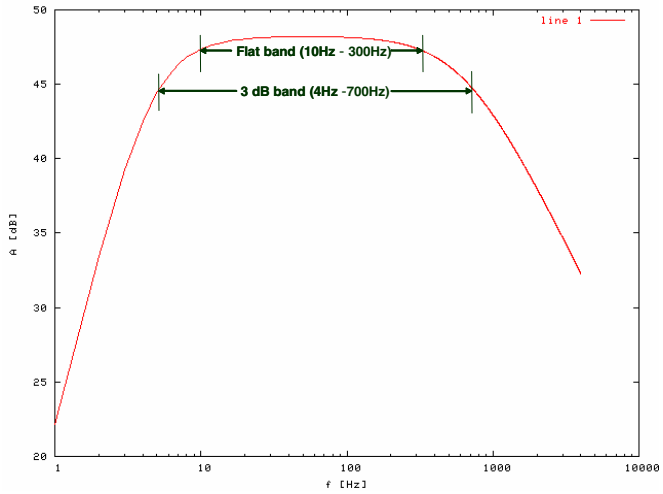


Figure 7. Gain response of decimator



9 Theory of operation

9.1 General operation

The STPMC1 (also called a calculator) is an ASSP designed for effective measurement in power line systems utilizing the Rogowski coil, current transformer, Shunt or Hall current sensors. This device, used with the STMicroelectronics STPMSx companion chip (an analog front-end device), can be implemented as standalone or as a peripheral in a microprocessor based 1-, 2- or 3-phase energy meter.

The calculator consists of three sections: analog, digital and OTP (see *Figure 1*):

- The analog section is composed of a band-gap voltage reference and a low-drop voltage regulator.
- The digital section consists of a system control, clock generator, three PDSP and a NDSP, a SPI interface.
- The 112-bit OTP block and the 16 system signals, used for testing, configuration and calibration purposes, are controlled through SPI by means of a dedicated command set.

The calculator has five input data pins, of which four are fed by signals generated by the STPMSx, see *Table 9*.

Three of them (DAR/DAS/DAT) are used to receive multiplexed signals of voltage and current, implementing energy measurement in 1-, 2- and 3-phase (3 and 4 wires) systems.

After being de-multiplexed, each phase input is sent to the correspondent DSP unit that processes voltage and current information and performs energy calculation, according to the settings of the configuration bits (see *Table 33*).

The DAN input, which also receives a multiplexed signal output from STPMSx device, is typically used to monitor neutral current for anti tampering functions in 1-, 2- and 3-phase (4 wires) systems. Normally the STPMSx monitors current and voltage but in case of neutral monitoring the voltage channel can be connected to a different type of sensor, for example a temperature sensor.

The fifth input data pin (DAH) accepts non-multiplexed $\Delta\Sigma$ signals. It can be used for EMI sensing through Hall sensors or for temperature sensing.

Table 9. Input channels from the STPMSx

Channel name	Property	Signal 1	Signal 2
DAR	Multiplexed	Voltage	Current
DAS	Multiplexed	Voltage	Current
DAT	Multiplexed	Voltage	Current
DAN	Multiplexed	Temperature	Current
DAH	Not multiplexed	EMI or temperature	

The companion chip (STPMSx) embeds 2 $\Delta\Sigma$ ADC converters and the necessary logic capable of providing the multiplexed $\Delta\Sigma$ streams.

See the STPMSx documentation for more details.

These four multiplexed signals are separated, by a digital de-multiplexer, back into eight ΔΣ signals, called streams. The signal coming from the voltage channel of the STPMSx is named with the suffix V, while the stream coming from the current channel is named with the suffix C. For example, the voltage stream of the S-phase is named DAS-V.

Then, each pair of phase the voltage and current stream coming from DAR, DAS and DAT is connected to a dual-channel RDSP, SDSP, TDSP unit (i.e. DAR-V and DAR-C are connected to RDSP).

Each phase voltage input stream is proportional to phase voltage u. Each phase current input stream is proportional to derivation of phase current di/dt, when it originates from Rogowski coil, or to phase current i, when it originates from Shunt or CT or Hall sensor. In this case a derivative is inserted into the voltage channel to get a stream proportional to du/dt. The sensors differ from each other for sensitivity, phase error and susceptibility to external EM fields.

Each of these DSP units performs the following:

- checks the integrity of the streams
- calibrates streams
- filters both streams with a dedicated decimation filter
- computes active and reactive energies, momentary and RMS values for voltage and current, period of power line voltage signal.

In each DSP there are calibrators capable of adjusting the readings ±12.5%.

The power computer does the final calculations of the value and direction of the power and checks for no-load condition.

Another dual DSP unit, called NDSP, processes the streams coming from DAN and DAH. In fact, using the ENH bit (see *Table 33*), the user can select either the voltage stream of the DAN pin (DAN-V) or the DAH stream as the input of the NDSP unit, while the current stream DAN-C is always processed as neutral current.

In its voltage channel, the NDSP unit uses a 2 s time multiplex to process two streams. During the first half of the interval the voltage input stream is processed (which can be DAN-V or DAH, according to the ENH bit), while during the second half a stream constituted by the sum of all four calibrated currents (i.e. DAR-C + DAS-C + DAT-C + DAN-C).

In its current channel the NDSP unit process the current stream of the neutral conductor as follows:

- checks the integrity of stream
- calibrates the stream
- filters the stream with a dedicated decimation filter
- computes momentary and RMS values of the stream
- if no errors have been detected in the phase timing, computes phase frequency, integrates the phase powers by means of 3-input integrators of energies and generates all pulse output signals.

When the DAH input stream is selected, it is checked to detect an external magnetic influence (EMI) to the meter.

The calculator, thanks to its flexibility, can work in all worldwide distribution network standards. By programming the SYS OTP bits, it is possible to implement the following systems:

- 3-phase, 4-wire RSTN, 4-system RSTN (tamper);
- 3-phase, 4-wire RSTN, 3-system RST;
- 3-phase, 3-wire RST_, 3-system RST_ (tamper);
- 3-phase, 3-wire RST_, 2-system R_T_ (Aron);
- 2-phase, 3-wire _STN, 2-system _ST_ (America);
- 1-phase, 2-wire __TN, 2-system _ST_ (tamper coil:coil);
- 1-phase, 2-wire __TN, 2-system _ST_ (tamper coil:shunt);
- 1-phase, 2-wire __TN, 1-system __T_.

The results of all DSP units are available as pulse frequency on pin LED, MOP and MON, which can also drive a stepper counter, and as states on the digital outputs of device or as data bits in data records, which can be read from the device by means of SPI interface from pins SDA, SNC, SCL and SYN. This system bus interface is also used during temporary or permanent programming OTP bits and system signals or to execute a remote reset request.

A logic block common to all DSP units performs other operations like:

- selecting the valid phase period result from which line frequency is computed in NDSP unit
- checking the equality of phase angles between all three phase voltages
- preparing current values for compensation of external intermediate phase magnetic influences
- checking the sum of currents
- computing intermediate phase voltages
- combining the 3-phase status bits
- performing a watchdog user function

After the device is fully tested, configured and calibrated, a dedicated bit of the OTP block, called TSTD, can be written permanently in order to prevent the change of any configuration bit.

9.2 Power supply

The supply pins for the analog part are V_{CC} and V_{SS}. The V_{CC} is the power input of the 1.8 V low drop regulator, band-gap reference and bias generators.

From the V_{CC} pin a linear regulator generates the +1.8 V voltage supply level (V_{DD}) which is used to power the OTP module and digital core. The V_{SS} pin represents the reference point for all the internal signals. 100 nF low ESR capacitors should be connected between V_{CC} and V_{SS}, and 1 µF between V_{DD} and V_{SSA}. All these capacitors must be placed very close to the device.

The STPMC1 contains a power on reset (POR) detection circuit. If the V_{CC} supply is less than 2.5 V then the STPMC1 goes into an inactive state, all the functions are blocked asserting a reset condition. This is useful to ensure correct device operation at power-up and during power-down. The power supply monitor has built-in hysteresis and filtering, which gives a high degree of immunity from false triggering due to noisy supplies.
A bandgap voltage reference (VBG) of 1.23 V ±1% is used as a reference voltage level

source for the linear regulator. Also, this module produces several bias currents and voltages for all other analog modules and for the OTP module.

9.3 Resetting the STPMC1 (status bit *HLT*)

The STPMC1 has no reset pin. The device is automatically reset by the power-on-reset detection circuit (POR) when the V_{CC} crosses the 2.5 V value, but it can be reset also through the SPI interface through a dedicated remote reset request (RRR) command (see paragraph *9.21* for RRR details).

The reset through SPI is used during production testing or in an application with some on-board microprocessors when a malfunction of the device is detected.

Resetting the STPMC1 causes all the functional modules of STPMC1 to be cleared, including the OTP shadow latches (see paragraph *9.19* for an OTP shadow latch memory description). In case of reset through SPI the mode signals (see paragraph *9.20* for a description of the mode signals) are not cleared.

In cases of reset caused by the POR circuit all blocks of the digital part, except the SPI interface, are held in a reset state for 125 ms after the reset condition. When the reset is performed through SPI, no delayed turn-on is generated.

During the device reset, the status bit *HLT* is held high, meaning that data read from the device register are not valid.

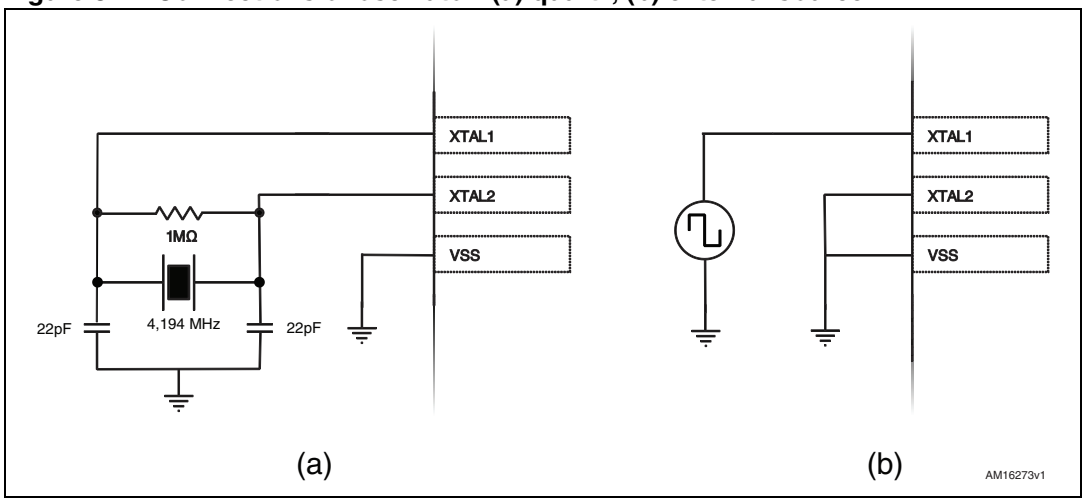
9.4 Clock generator (bits MDIV, FR1, HSA)

All the internal timing of the STPMC1 is based on the XTAL1 signal. This signal can be generated in two different ways:

- Quartz: the oscillator works with an external crystal.
- External clock: the clock is provided by an external source connected to XTAL1.

The suggested circuits are depicted in *Figure 8*.

Figure 8. Connections of oscillator: (a) quartz, (b) external source



The clock generator is responsible for two tasks.
The first is to retard the turn-on of some functional blocks after POR in order to help a smooth start of external power supply circuitry by keeping off all major loads. For this

reason, all blocks of the digital part, except the SPI interface, are held in a reset state for 125 ms after a power on reset (see *Section 9.3*).
The second task of the clock generator is to provide all necessary clocks for the digital part. In this task, a MDIV and FR1 programming bits are used to inform the device about the nominal frequency value from XTAL1 (f_{XTAL1}).
Four nominal frequencies are possible through proper setting of the MDIV and FR1 bits (see *Table 10*).

The internal master clock f_{MCLK} is derived from f_{XTAL1} as shown in *Table 10*.

Table 10. Frequency settings through MDIV and FR1 (1)

f_{XTAL1}	MDIV (1 bit)	FR1 (1 bit)	f_{MCLK}
4.194 MHz	0	0	8.389 MHz
4.915 MHz	0	1	9.830 MHz
8.192 MHz	1	0	8.192 MHz
9.830 MHz	1	1	9.830 MHz

1. 4 MHz and 8 MHz clock are also supported. MDIV and FR1 have to be set as for 4.194 MHz and 8.192 MHz respectively.

Through the HSA bit the frequency of the output pin CLK (f_{CLK}), which provides the clock for the STPMSx devices, can be derived as reported in *Table 11*.

Table 11. CLK pin frequency settings through HSA

HSA (1 bit)	f_{CLK} STPMC1
0	f_{XTAL1} / 4
1	f_{XTAL1} / 2

To properly work with STPMS2, the clock configurations in *Table 12* must be used. Moreover, with STPMS2 companion chip the PM bit must always be set.

Table 12. STPMC1 configuration for STPMS2

MDIV (1 bit)	HSA (1 bit)	f_{CLK}
0	0	f_{XTAL1} / 4
1	0	f_{XTAL1} / 4
0	1	f_{XTAL1} / 2

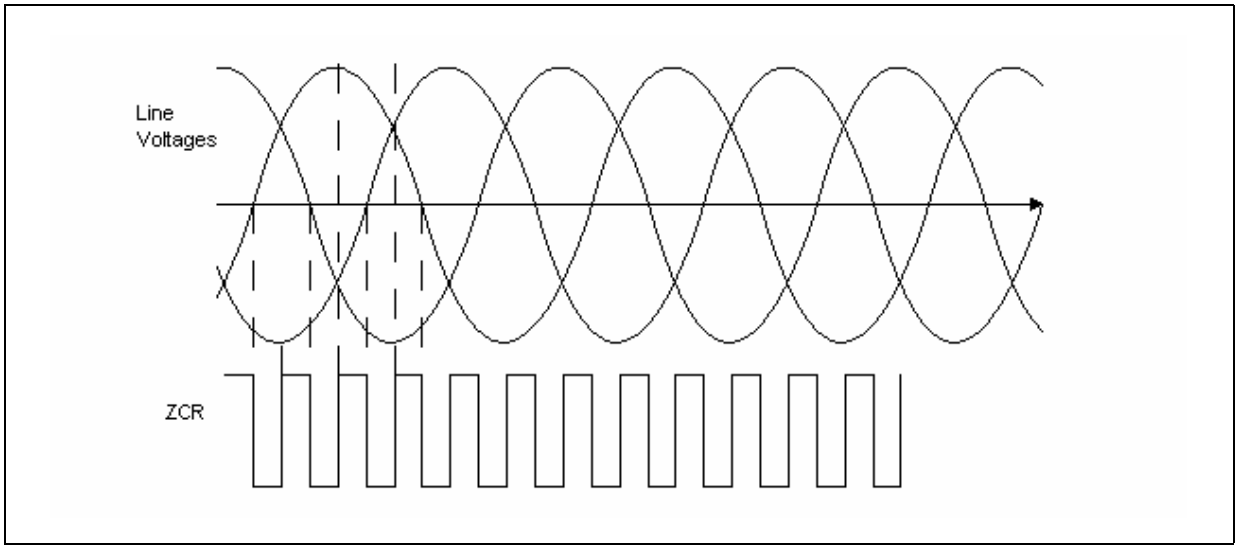
9.5 Zero crossing detection (signal *ZCR*)

The STPMC1 has a zero crossing detection circuit on the voltage channel that can be used to synchronize some utility equipment to zero crossing or max of line voltage events. This circuit produces the internal signal *ZCR* that has a falling edge every zero crossing of one of the line voltages and a rising edge every peak (positive or negative) of one of the line voltages.

The *ZCR* signal is a 3-phase voltage zero cross signal. It is the result of a XNOR of the *ZCR* of each phase. The *ZCR* of each of the three-phases is a 100 Hz signal, so a 3-phase *ZCR*

is 300 Hz signal. The *ZCR* signal is available on the MOP pin only when the STPMC1 works as a peripheral with the configuration bit APL=0.

Figure 9. *ZCR* signal



9.6 Period and line voltage measurement (status bits: *LIN*, *BFR*, *LOW*, *BFF*)

From voltage channels, a base frequency signal *LIN* is obtained, which is high when the line voltage is rising and it is low when the line voltage is falling, so that, *LIN* signal represents the sign of dv/dt. With further elaboration, the *ZCR* signal is also produced.

A period meter, which is counting up pulses of $f_{MCLK}/8$ reference signal, measures the period of voltage channel base frequency and checks if the voltage signal frequency is in the band going from $f_{MCLK}/(2^{18} - 2^3) \approx f_{MCLK}/2^{18}$ to $f_{MCLK}/2^{16}$.

This is done, phase by phase, by means of the signal *LIN*, which trailing edge is extracted and it is used to reset the period meter.

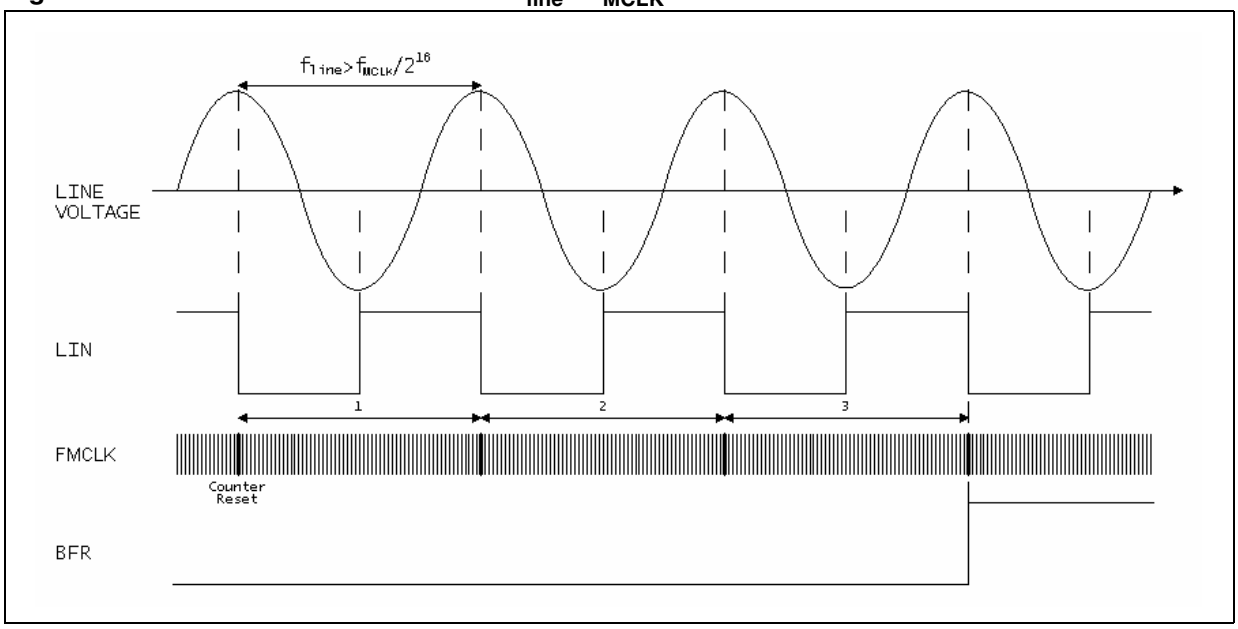
Table 13. Good frequency ranges for different clock source values

f_{XTAL}	f_{MCLK}	freq. min. = $f_{MCLK}/2^{18}$	freq. max. = $f_{MCLK}/2^{16}$
4.194 MHz	8.389 MHz	32.0 Hz	128.0 Hz
4.915 MHz	9.830 MHz	37.5 Hz	150.0 Hz
8.192 MHz	8.192 MHz	31.3 Hz	125.0 Hz
9.830 MHz	9.830 MHz	37.5 Hz	150.0 Hz

If the counted number of $f_{MCLK}/8$ pulses between two trailing edges of *LIN* is higher than the 2^{18} equivalent pulses or if the counting is never stopped (no more *LIN* trailing edge), the base frequency exceeds the lower limit and an error flag *BFR* is set. This error flag is part of the 8-bit status byte of each phase (see *Table 32*).

If the counted number of $f_{MCLK}/8$ pulses between two trailing edges of *LIN* is lower than the 2^{16} equivalent pulses, the base frequency exceeds the upper limit. In this case, such error must be repeated three times, in order to set the error flag *BFR*, as shown in *Figure 10*.

Figure 10. *LIN* and *BFR* behavior when $f_{line} > f_{MCLK}/2^{16}$



The in-band base frequency resets the flag *BFR*. If *BFR* is cleared, the measured period value is latched, otherwise a default value of period is used as a stable data to compute frequency needed to adapt the decimation filter and to perform frequency compensation of reactive energy and RMS current I_X in case of non Rogowski current sensor.

The *BFR* flag is also set if the register value of the RMS is too low. In this case also the status bit *LOW* is set.

The condition for setting *LOW* and consequently *BFR* of each phase is $U_X < U_{Xmax}/32$ ($U_{Xmax} = 2^{12}$) it means if the U_X register drops below 128 *LOW* and *BFR* are cleared when the register value goes above 256 ($U_X > U_{Xmax}/16$). *BFR*, then, gives also information about the presence of the line voltage.

When the *BFR* error is set, the computation of power is zero and the energy registers (active, reactive and fundamental) are blocked, unless single wire mode operation is entered (see *Section 9.7*).

When the MOP, MON and LED pins are configured to provide the pulsed energy information they are held low if *BFR* is set.

The 3-ph status bit *BFF* is the OR of each phase bit *BFR*.

9.7 Single wire operation mode: SWM (status bits: *NAH*, *BFR*, configuration bit FRS)

The STPMC1 supports single wire meter (SWM) operation. In this condition, since there is no voltage information, the current RMS values, instead of the energies, are accumulated in 20-bit dedicated registers located in ACR, ACS, ACT (20-bit accumulator of RMS I_X per hour [Ah]).