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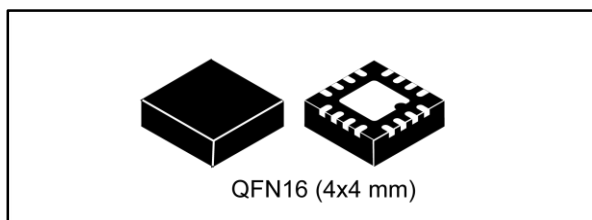
Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



Smart sensor II dual-channel 1-bit, 4 MHz, second-order sigma-delta modulator with embedded PGLNA

Datasheet - production data



Features

- V_{CC} supply range 3.2 V to 5.5 V
- Two second-order sigma-delta ($\Sigma\Delta$) modulators
- Programmable chopper-stabilized low noise and low offset amplifier
- Supports 50-60 Hz, EN 50470-1, EN 50470-3, IEC 62053-21, IEC 62053-22 and IEC 62053-23 standard specs for class 1, class 0.5 and class 0.2 AC watt meters
- STPMS2L-PUR: less than 0.5% error over 1:5000 range
- Precision voltage reference: 1.23 V with programmable TC
- Internal low drop regulator @ 3 V (typ.)

Applications

- Power metering
- Motor control
- Industrial process control
- Weight scales
- Pressure transducers

Description

The STPMS2 also called “smart sensor” device, is an ASSP designed for effective measurement in power line systems utilizing the Rogowski coil, current transformer and Hall or shunt sensors. This device is designed as a building block for single-phase or multi-phase energy meters along with the STPMC1 device, a digital signal processor designed for energy measurement. This device can be used in medium and high resolution measurement applications where single or double inputs must be monitored at the same time. The STPMS2 is a mixed signal IC consisting of an analog and digital section. The analog section consists of a programmable gain, low noise chopper amplifier, two second-order $\Delta\Sigma$ modulator blocks, a bandgap voltage reference, a low drop voltage regulator and DC buffers, while the digital section consists of a clock generator and output multiplexer.

Table 1: Device summary

Oder code	Package	Packing
STPMS2L-PUR	QFN16 (4x4 mm)	4500 pieces per reel

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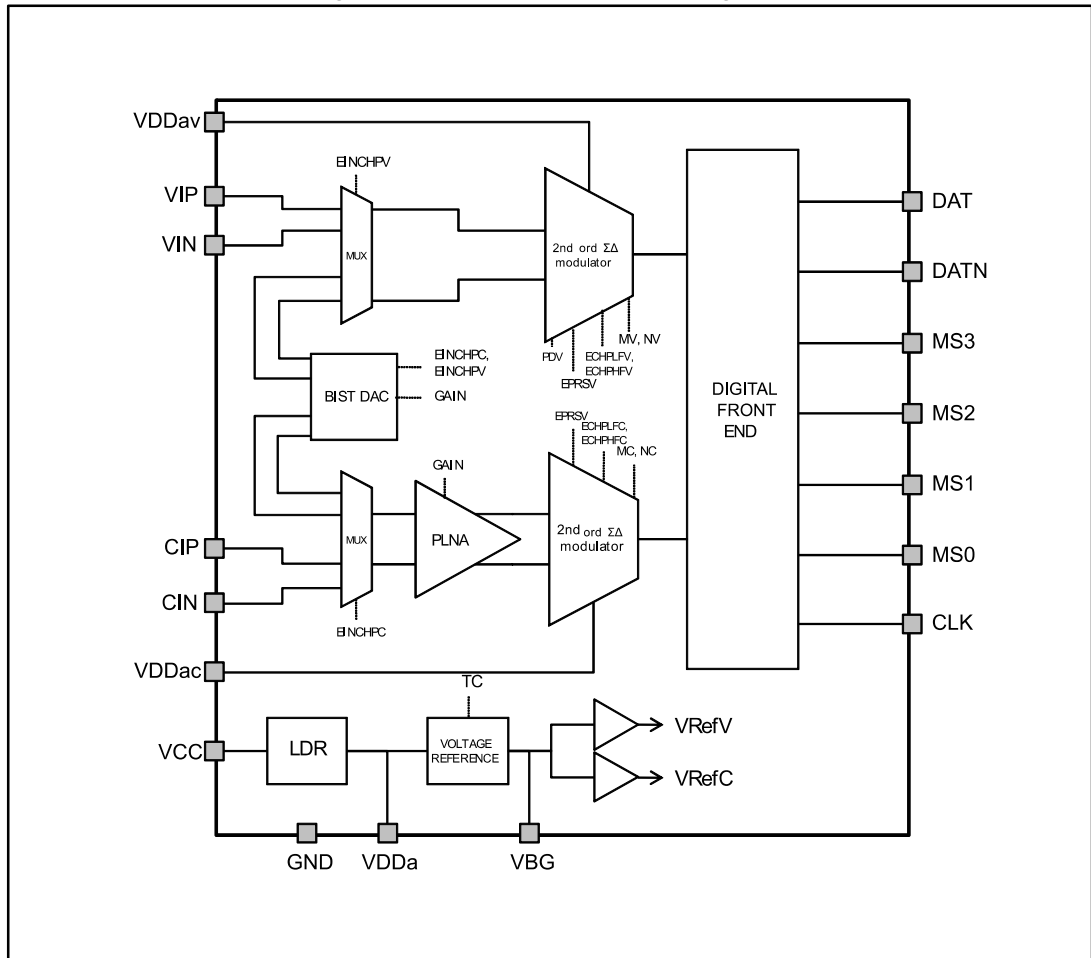
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1 Introduction

The STPMS2 is a device designed to measure electrical line parameters (voltage and current) via analog signals from voltage sensors (current divider) and current sensors (inductive Rogowski coil, current transformer or shunt resistors). The device is used together with a digital signal processing circuit to implement an effective measuring system for multi-phase power meters. The device consists of two analog measuring channels, consisting of second-order sigma-delta modulators with an appropriate non-overlapping control signal generator. The STPMS2 also includes a temperature compensated bandgap reference voltage generator, a low drop supply voltage stabilizer and a minimal digital circuitry that includes BIST (built-in self-test) structures. In a current signal processing channel, a low-noise preamplifier is included in front of the sigma-delta converter. All reference voltages (bandgap, AGND) are internally buffered to eliminate channel crosstalk. The STPMS2 can operate in fast or low-power mode. In fast mode, a nominal clock frequency of 4.1 or 4.9 MHz is applied to the clock input. In this mode, signal bandwidth is specified between 0 and 4 kHz. In low-power mode, the nominal clock is four times slower in order to reduce the power consumption of the circuit. In low-power mode, the quiescent bias currents of the preamplifier and sigma-delta integrators are lowered and the signal bandwidth is narrowed to the frequency bandwidth from 0 to 1 kHz.

2 Internal block diagram

Figure 1: STPMS2 internal block diagram



3 Pin configuration

Figure 2: Pin connections

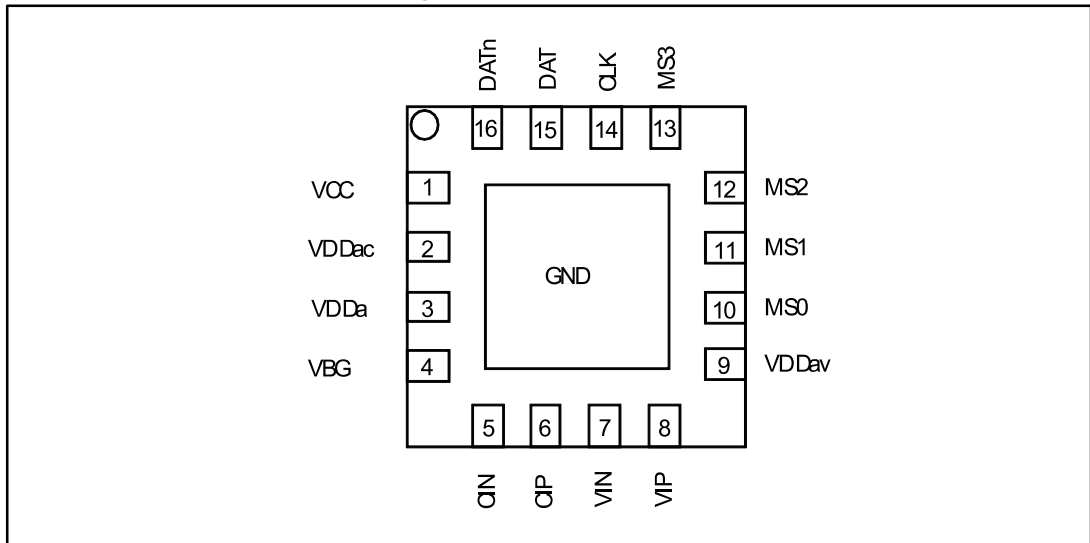


Table 2: Pin description

Pin	Symbol	Description
1	VCC	Unregulated supply voltage for pad ring, bandgap, low drop and level shifters
2	VDDac	Current channel modulator supply input
3	VDDa	Output of internal + 3.0 V low drop regulated power supply
4	VBG	Output of internal + 1.23 V bias generator
5	CIN	Current channel -
6	CIP	Current channel +
7	VIN	Voltage channel -
8	VIP	Voltage channel +
9	VDDav	Voltage channel modulator supply input
10	MS0	Input for configurator 0
11	MS1	Input for configurator 1
12	MS2	Input for configurator 2
13	MS3	Input for configurator 3
14	CLK	Input for external measurement clock
15	DAT	Output of multiplexed $\Sigma\Delta$ signal. Output of current $\Sigma\Delta$ signal
16	DATn	Output of inverted multiplexed $\Sigma\Delta$ signal. Output of voltage $\Sigma\Delta$ signal
17	GND	Ground level for signals and pin protection

4 Maximum ratings

Table 3: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{CC}	DC input voltage	- 0.3 to 6	V
I _{PIN}	Current on any pin (sink/source)	±150	mA
V _{ID}	Input voltage on any pin	-0.3 to V _{CC} +0.3	V
V _{IA}	Input voltage at analog pins (VIP, VIN, IIP, IIN)	-0.7 to 0.7	V
ESD	Human body model	±2	kV
T _{OP}	Operating ambient temperature	- 40 to 85	°C
T _J	Maximum operating junction temperature	-40 to 150	°C
T _{STG}	Storage temperature	-55 to 150	°C



Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

Table 4: Thermal data

Symbol	Parameter	Value	Unit
R _{thJA} ⁽¹⁾	Thermal resistance junction-ambient	38.66	°C/W

Notes:

⁽¹⁾This value is referred to single-layer PCB, JEDEC standard test board.

5 Electrical characteristics

$V_{CC} = 5\text{ V}$, $T_{AMB} = 25\text{ }^{\circ}\text{C}$, $1\text{ }\mu\text{F}$ between V_{CC} , V_{DDa} , V_{DDAc} , V_{DDAv} and GND, 100 nF between VBG and GND, $f_{CLK} = 4.19\text{ MHz}$ unless otherwise specified.

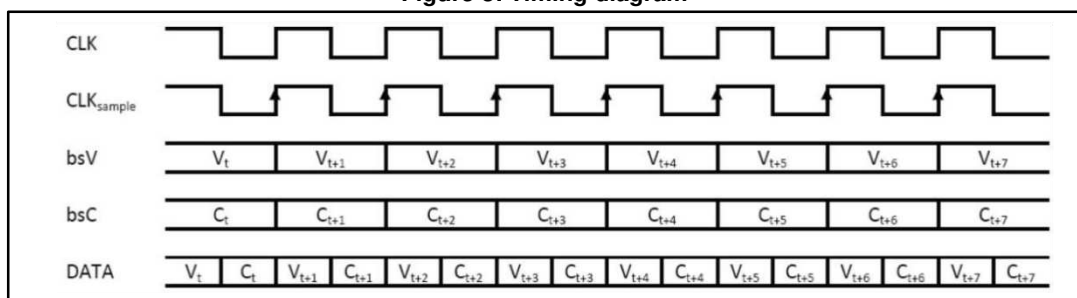
Table 5: Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
General section						
V_{CC}	Operating supply voltage		3.135		5.25	V
I_{CC}	Quiescent current	LP, 1.229 MHz; $V_{CC} = 3.3\text{ V}$; CL = 100 nF; no loads		1.2	1.5	mA
		HP, 4.915 MHz; $V_{CC} = 3.2\text{ V}$; CL = 100 nF; no loads		4	5	
V_{POR}	Power-on-reset on V_{CC}			2.5		V
V_{DD}	Regulated supply voltage	1.049 MHz; $V_{CC} = 3.2\text{ V}$; CL = 100 nF; no loads	2.95	3.00	3.05	V
I_{LATCH}	Current injection latch-up immunity				300	mA
f_{BW}	Effective bandwidth	Limited by chopper	0		4091	Hz
DC measurement accuracy						
	Resolution		11		16	Bit
INL	Integral non linearity	Result referred to a 16-bit word of CIP-CIN channel, HP mode, $f_{CLK} = 2.047\text{ MHz}$		3.3		LSB
		Result referred to a 12-bit word of VIP-VIN channel, HP mode, $f_{CLK} = 2.047\text{ MHz}$		3.9		
DNL	Differential linearity	Result referred to a 16-bit word of CIP-CIN channel, HP mode, $f_{CLK} = 2.047\text{ MHz}$		0.3		LSB
		Result referred to a 12-bit word of VIP-VIN channel, HP mode, $f_{CLK} = 2.047\text{ MHz}$		0.5		
	Offset error	Result referred to a 16-bit word of CIP-CIN channel, HP mode, $f_{CLK} = 2.047\text{ MHz}$		0.02		LSB
		Result referred to a 12-bit word of VIP-VIN channel, HP mode, $f_{CLK} = 2.047\text{ MHz}$		0.005		
	Gain error	Result referred to a 16-bit word of CIP-CIN channel, HP mode, $f_{CLK} = 2.047\text{ MHz}$	0.04		0.4	LSB/ μV
		Result referred to a 12-bit word of VIP-VIN channel, HP mode, $f_{CLK} = 2.047\text{ MHz}$		0.003		

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
NF	Noise floor	CIP-CIN channel gain 2x		120		dB
		CIP-CIN channel gain 16x		118		
		VIP-VIN channel		95		
PSRR _{DC}	Power supply DC rejection	Voltage signal: 200 mVrms/50 Hz Current signal: 10 mVrms/50 Hz f _{CLK} = 2.048 MHz V _{CC} = 3.3 V ±10%, 5 V ±10%	90			dB
AC measurement accuracy						
SNR	Signal-to-noise ratio	CIP-CIN channel – Vin = ±230 mV @ 55 Hz gain 2x over 4 kHz bandwidth		82		dB
		VIP-VIN channel – Vin = ±230 mV @ 55 Hz over 4 kHz bandwidth		52		
SINAD	Signal-to-noise ratio + distortion	CIP-CIN channel – Vin = ±230 mV @ 55 Hz gain 2x over 4 kHz bandwidth		82		dB
		VIP-VIN channel – Vin = ±230 mV @ 55 Hz over 4 kHz bandwidth		52		
THD	Total harmonic distortion	CIP-CIN channel – Vin = ±230 mV @ 55 Hz gain 2x over 4 kHz bandwidth		-105		dB
		VIP-VIN channel – Vin = ±230 mV @ 55 Hz over 4 kHz bandwidth		-78		
SFDR	Spurious free dynamic range	CIP-CIN channel – Vin = ±230 mV @ 55 Hz gain 2x over 4 kHz bandwidth		90		dB
		VIP-VIN channel – Vin = ±230 mV @ 55 Hz over 4 kHz bandwidth		68		
PSRR _{AC}	Power supply AC rejection	Voltage signal: 200 mVrms/50 Hz Current signal 10 mVrms/50 Hz f _{CLK} = 2.048 MHz V _{CC} = 3.3 V+0.2 Vrms1@100 Hz V _{CC} = 5.0 V+0.2 Vrms1@100 Hz	120			dB
Analog inputs (CIP, CIN, VIP, VIN)						
V _{MAX}	Maximum input signal levels	VIP-VIN channel	-0.3		+0.3	V
		CIP-CIN channel: gain 2x	-0.3		+0.3	V
		CIP-CIN gain 4x	-0.15		+0.15	
		CIP-CIN gain 8x	-0.075		+0.075	
		CIP-CIN gain 16x	-0.0375		+0.0375	
f _{SPL}	A/D sampling frequency			f _{CLK}		Hz

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{off}	Amplifier offset				±20	mV
Z _{IP}	VIP, VIN impedance	Over total operating voltage range	100		400	kΩ
Z _{IN}	CIP, CIN impedance	Over total operating voltage range	35		50	kΩ
G _{ERR}	Gain error of current channels			±10		%
I _{ILV}	Voltage channel leakage current	V _{CC} = 5.25 V, f _{CLK} = 4.19 MHz	-1		1	μA
I _{ILI}	Current channel leakage current	V _{CC} = 5.25 V, f _{CLK} = 4.19 MHz	-1		1	μA
		V _{CC} = 5.25 V, f _{CLK} = 4.19 MHz input enabled	-10		10	μA
	Crosstalk between channels			130		dB
Digital I/O (CLK, DAT, DATN, MS0, MS1, MS2, MS3)						
V _{IH}	Input high voltage		0.75 V _{CC}		5.3	V
V _{IL}	Input low voltage		-0.3		0.25 V _{CC}	V
V _{OH}	Output high voltage	I _O = -1 mA, CL = 50 pF, V _{CC} = 3.2 V	V _{CC} -0.4			V
V _{OL}	Output low voltage	I _O = +1 mA, CL = 50 pF, V _{CC} = 3.2 V			0.4	V
I _{UP}	Pull-up current			15		μA
t _{TR}	Transition time	C _{LOAD} = 50 pF		10		ns
t _L	Latency	From 50% of CLK to 50% to DAT			40	ns
Clock input						
f _{CLK}	Nominal frequencies	Low precision mode	1.0		1.228	MHz
		High precision mode	2.0		2.458	
		High precision mode	4.0		4.915	
On-chip reference voltage						
V _{REF}	Reference voltage		1.21	1.23	1.25	V
Z _{out}	Output impedance		30		200	kΩ
I _L	Maximum load current			0		μA
T _C	Temperature coefficient	After calibration		30	50	ppm/°C

Figure 3: Timing diagram



CLK - clock signal on CLK pin

CLK_{sample} - sigma-delta sampling frequency

bsV - sigma-delta bit stream of voltage signal

bsC - sigma-delta bit stream of current signal

DATA - multiplexed data of voltage and current signal on DAT pin

6 Applications

The choice of external components is a crucial point in the application design, affecting the precision and the resolution of the entire system. Among the several considerations, a compromise should be found among the following requirements:

1. Maximize the signal-to-noise ratio in the voltage and current channel.
2. Choose the current-to-voltage conversion ratio k_s and the voltage divider ratio so that calibration can be achieved.
3. Choose k_s to take advantage of the whole current dynamic range in accordance with the desired maximum current and resolution.

To maximize the signal-to-noise ratio of the current channel, the voltage divider resistor ratio should be as close as possible to those shown in [Table 6](#). [Figure 4](#) below provides a reference application schematic diagram:

- $P = 64000 \text{ imp/kWh}$
- $I_{\text{NOM}} = 5 \text{ A}$
- $I_{\text{MAX}} = 60 \text{ A}$

Typical sensitivity values for the current sensors are indicated in [Table 6: "Recommended external components in metering applications"](#).

Figure 4: Detailed application schematic

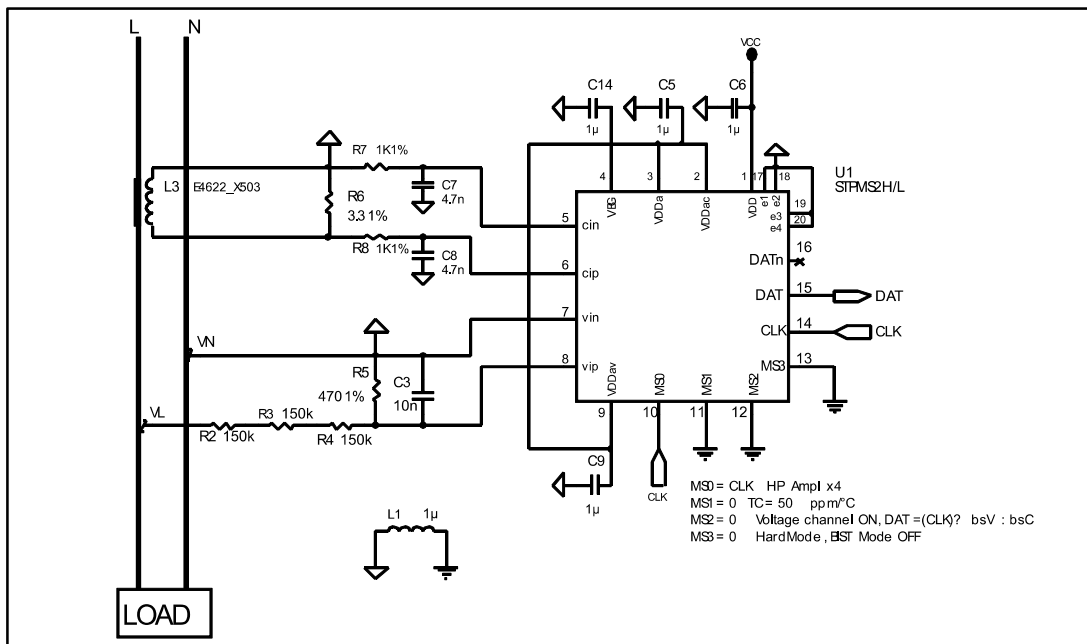


Table 6: Recommended external components in metering applications

Function	Component	Description	Value	Tolerance	Unit	
	Calculator	STPMC1				
Line voltage interface	Resistor divider	R-to-R ratio $V_{RMS} = 230\text{ V}$	1:1650	$\pm 1\%$	50 ppm/ $^{\circ}\text{C}$	V/V
		R-to-R ratio $V_{RMS} = 110\text{ V}$	1:830			
Line current interface	Rogowski coil	Current-to-voltage ratio k_S	0.15	$\pm 5\%$	50 ppm/ $^{\circ}\text{C}$	mV/A
	CT		1.7			
	Shunt		0.43			



Above listed components refer to a typical metering application. The STPMS2 operation is not limited to the choice of these external components.

Figure 5: Simplified application schematics for the STPMC1 energy metering-based

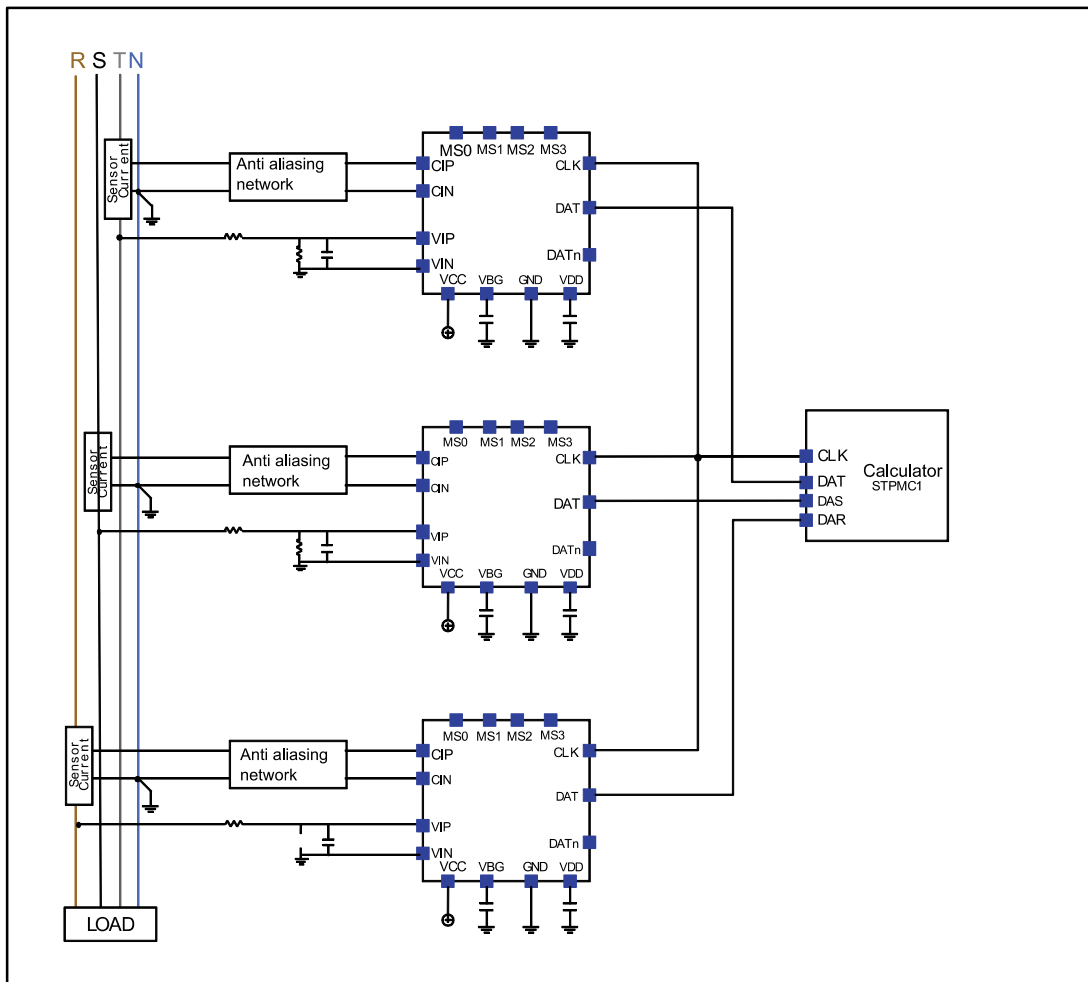
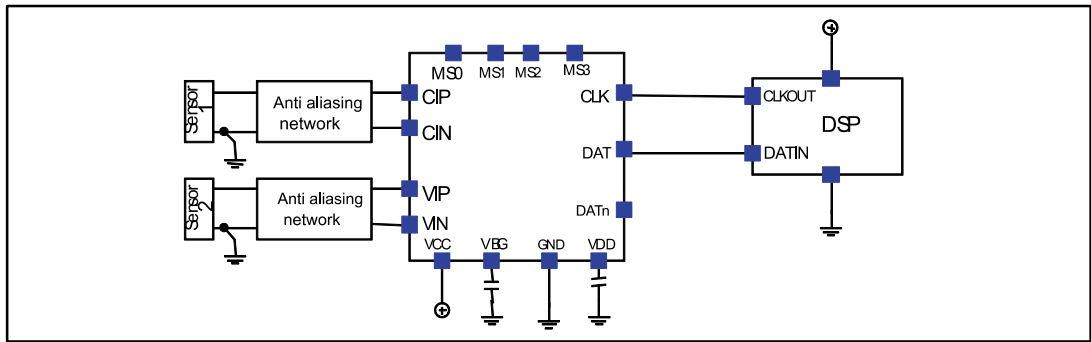


Figure 6: Connection schematics for DSP-based applications



7 Terminology

7.1 Conventions

The lowest analog and digital power supply voltage is called GND, which represents the system ground. All voltage specifications for digital input/output pins are referred to GND. The highest power supply voltage is called V_{CC} . The highest core power supply is internally generated and is called V_{DD} . Positive currents flow into a pin. Sinking current means that the current flows into the pin and thus it is positive. Sourcing current means that the current flows out of the pin and thus it is negative. A positive logic convention is used in all equations.

7.2 Notations

Output bit streams of the modulator are indicated as bsV and bsC for voltage and current channels, respectively.

8 Typical performance characteristics

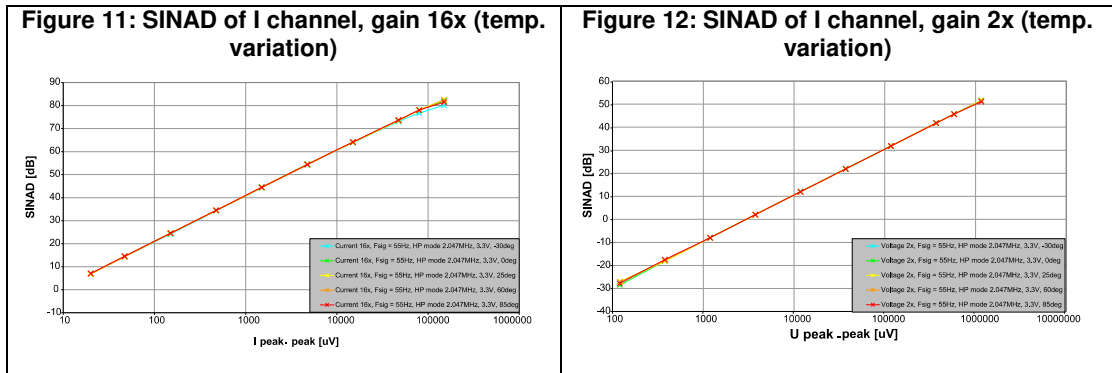
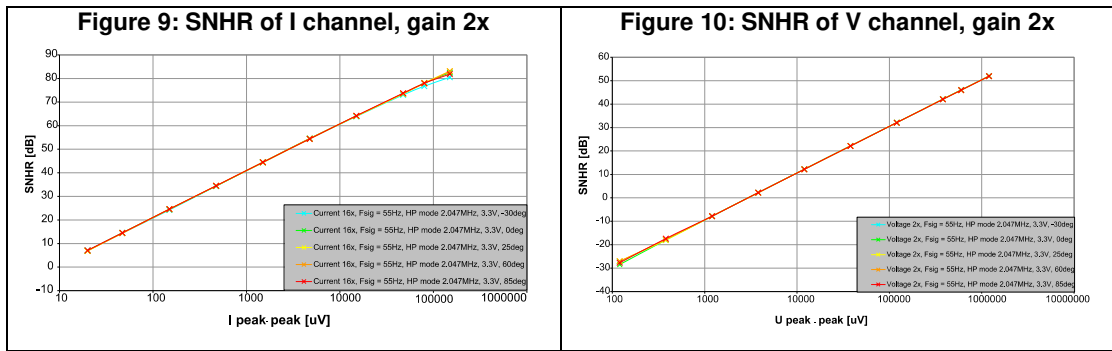
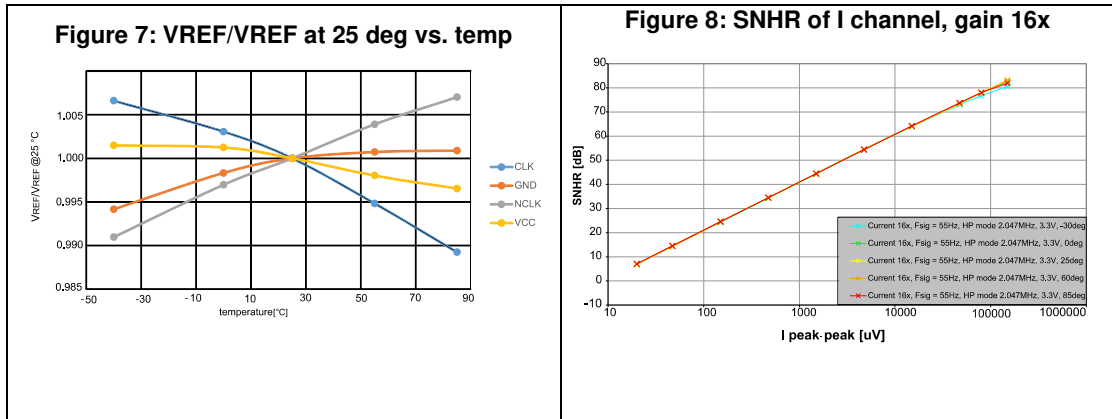


Figure 13: Relative gain error of I channel, gain 16x

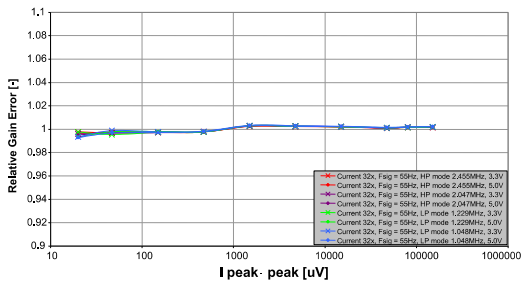


Figure 14: Relative gain error of I channel, gain 2x

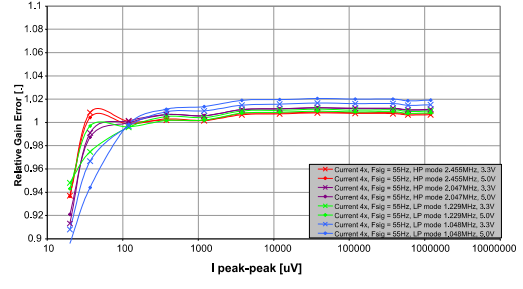
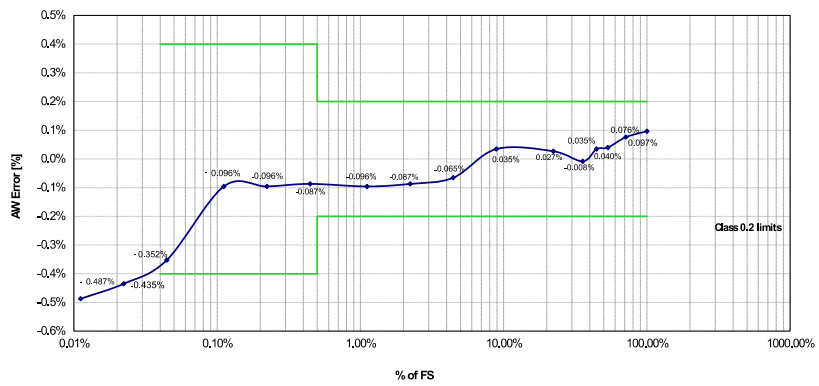


Figure 15: Accuracy over dynamic range



9 Theory of operation

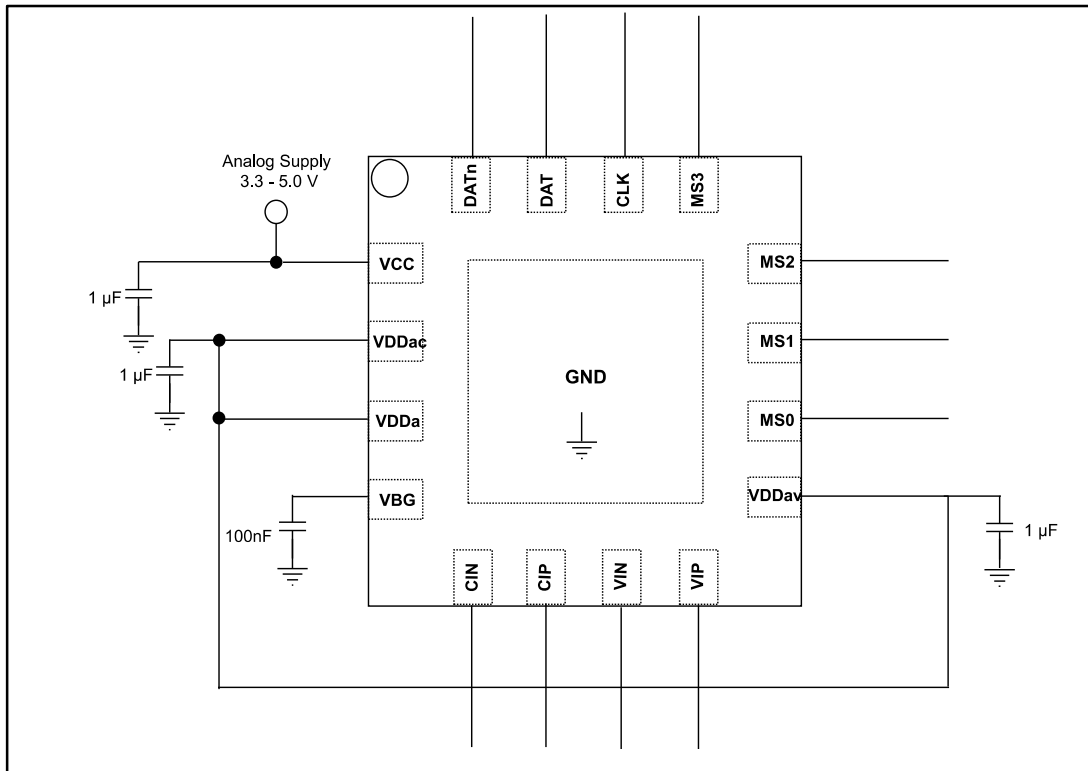
9.1 General operation description

The STPMS2 performs the second-order analog modulation of two channels in parallel, with appropriate non-overlapping control signal generator, of signals with frequencies varying from DC to 4 kHz on two independent channels in parallel. The outputs of the converters provide two digital streams of ones and zeroes, which can be then multiplexed to reduce the number of external connections. The STPMS2 converts analog signals on two independent channels in parallel via delta-sigma ($\Sigma\Delta$) analog-to-digital converters into a binary stream of sigma-delta signals. The device is particularly suitable to measure electrical line parameters (voltage and current) via analog signals from voltage sensors (current divider) and current sensors (inductive Rogowski coil, current transformer or shunt resistors). There is a current channel for line current and a voltage channel for line voltage. The current channel input is connected through an external anti-aliasing RC filter to a Rogowski coil, current transformer (CT) or shunt current sensor which converts line current into an appropriate voltage signal. The current channel includes a low-noise voltage preamplifier with programmable gain. The voltage channel is connected directly through a resistor voltage divider and anti-aliasing filter to a line voltage modulator (ADC). Both channels have quiescent zero signal point at GND, so the STPMS2 is able to sample differential signals on both channels with their zero point around GND. The converted $\Sigma\Delta$ signals are multiplexed so to reduce the number of external connections. The conversion and the multiplex are driven by external clock signal CLK. The device is used with a digital signal processing circuit to implement a measuring system of a multi-phase power meter. The STPMS2 also includes a temperature compensated bandgap reference voltage generator, low drop supply voltage regulator and minimal digital circuitry that includes BIST (built-in self-test) structures. In a current signal processing channel, a low-noise preamplifier is included upstream of the sigma-delta converter. All reference voltages are designed to eliminate channel crosstalk. The STPMS2 can operate in fast (HP) or low-power (LP) mode (see also [Table 7](#)). In fast mode, a nominal clock frequency of 4.1 or 4.9 MHz is applied to the clock input. In this mode, signal bandwidth is specified between 0 and 4 kHz. In low-power mode, the nominal clock is four times slower (1 MHz) to lower the power consumption of the circuit. In low-power mode, the quiescent bias currents of the preamplifier and sigma-delta integrators are reduced and the signal bandwidth is narrowed to the frequency bandwidth from 0 to 1 kHz. The mode of operation and configuration of the device can be selected by wiring configuration pins (MS0, MS1, MS2 and MS3) to VCC, GND, CLK or NCLK signal. This approach can be used to change the settings of a current channel, sigma-delta stream output mode and temperature compensation curve of an internal bandgap reference. These pins can act as a serial port to change the configuration of the device.

9.2 Functional description of the analog part

The supply pins for the analog part are VCC, VDDa, VDDac, VDDav, VBG and GND. The GND pin also represents a reference point. The VDDa is an analog I/O pin of the internal +3.0 V low drop voltage regulator and the VDDac and VDDav are the modulator supply inputs. A capacitor of 1 μ F should be connected between VDDxx and GND. The input of the regulator is VCC, which also powers the bandgap and bias generators. The bandgap output pin is VBG, which should be connected to GND via a capacitor of 100 nF.

Figure 16: Power supply external connection scheme



The analog part of the STPMS2 consists of:

- Preamplifier in the current channel
- 1.23 V reference voltage generator
- +3 V low drop supply voltage regulator
- Two sigma-delta 2nd order modulators
- BIST DAC
- AGND and V_{REF} reference buffers
- Bias current generators

The voltage channel has a preamplification gain of 2, which defines the maximum differential voltage on voltage channel inputs to ± 300 mV. The relative gain of the current channel is selectable among 2, 4, 8 or 16, which defines the maximum differential voltage on the current channel to ± 300 mV, ± 150 mV, ± 75 mV or ± 37.5 mV, respectively. The full range of gains is available in soft mode only, while in hard mode 2 and 16 are the only selectable. The temperature-compensated reference voltage generator produces $V_{REF} = 1.23$ V. This generator is implemented as a bandgap generator, whose temperature compensation curve can be selected through configuration. The low drop regulator fixes and stabilizes the core supply voltage to $VDDa = 3$ V. All digital pads tolerate 5 V logic levels. The STPMS2 is clocked by an external clock signal connected to pin CLK. The STPMS2 sigma-delta modulators work in several operating modes, shown in [Table 7: "Operating modes"](#) below.

Table 7: Operating modes

Operating mode		f _{CLK}	Current consumption
LP (low power)	LPR (low precision)	1 MHz	1.2 mA typ.
HP (fast)	HPR (high precision)	2 MHz – 4 MHz	4 mA typ.

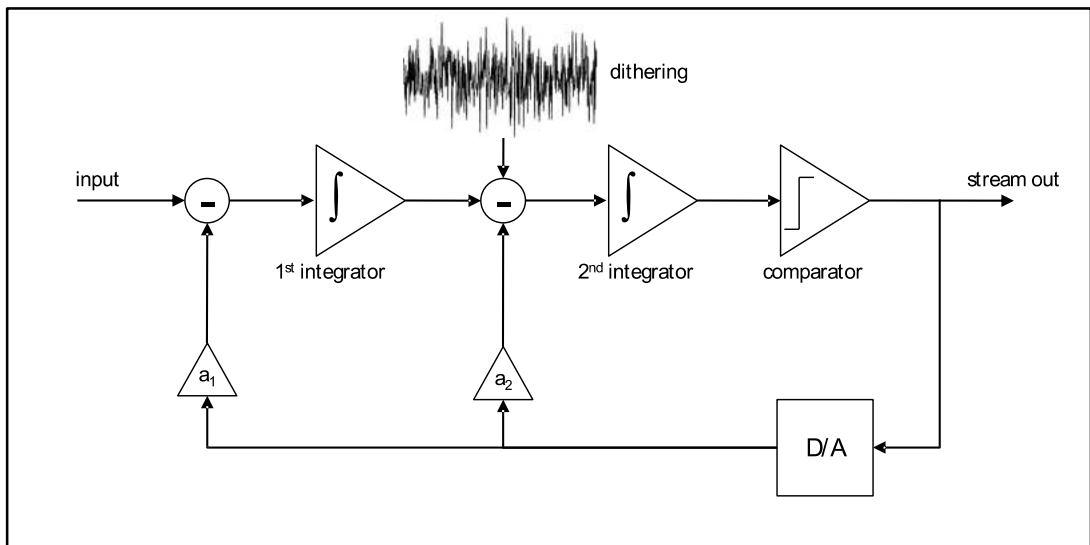
LPR (low precision): $f_{CLK} = 1$ MHz and settings defined by MS0 through MS3

HPR (high precision): the normal mode of operation with $f_{CLK} = 2$ MHz to 4 MHz

The STPMS2 performs operations in 2 basic modes: hard mode and soft mode. In hard mode the configuration is set through external pins MS0, MS1, MS2 and MS3. In soft mode, 40 configuration bits can be accessed through CFG[39:0], via serial communication. The pins used for serial communication are: MS0, MS1 and MS2. Switching between hard and soft mode is achieved through pin MS3.

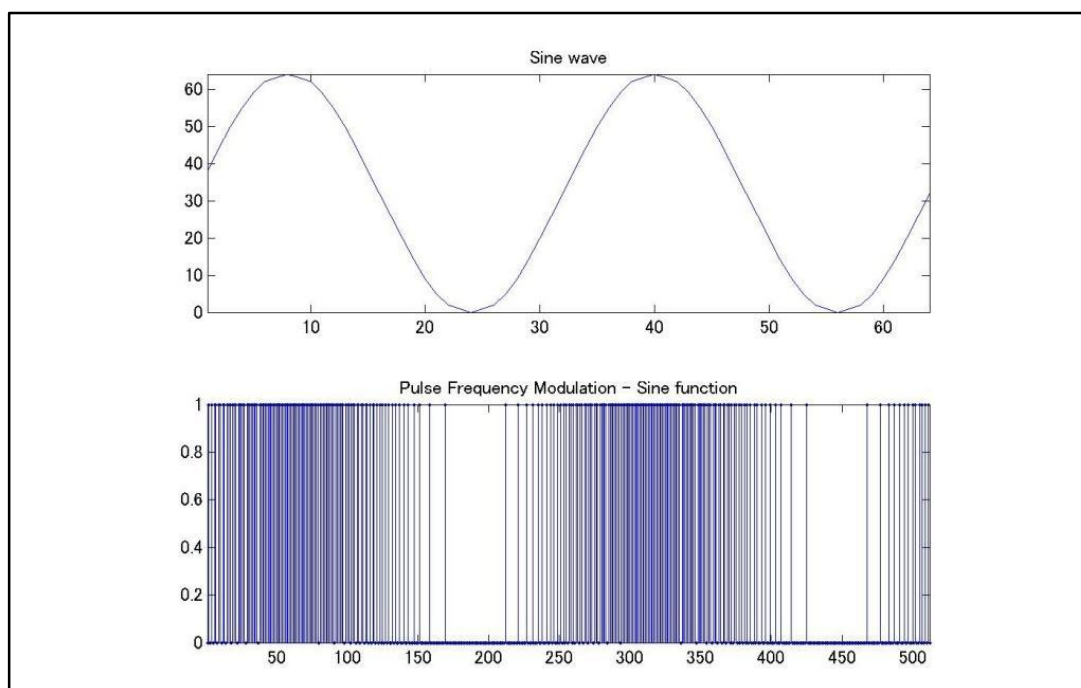
- Hard mode: in this case the device configuration is bootstrapped at startup and signals come from VIN and VIP for voltage channels, and CIP and CIN for current channels or from internal BIST DAC.
- Soft mode: in this mode all possible settings from hard mode are accessible, as well as the additional settings.

Figure 17: Block diagram of the modulator



The STPMS2 sends selected signals based on the configuration to the DAT and DATn pins. Both outputs have cross-current and slew rate limiters to prevent excessive current spikes on supply lines.

Figure 18: Example of sigma-delta modulator output in case of sinusoidal waveform

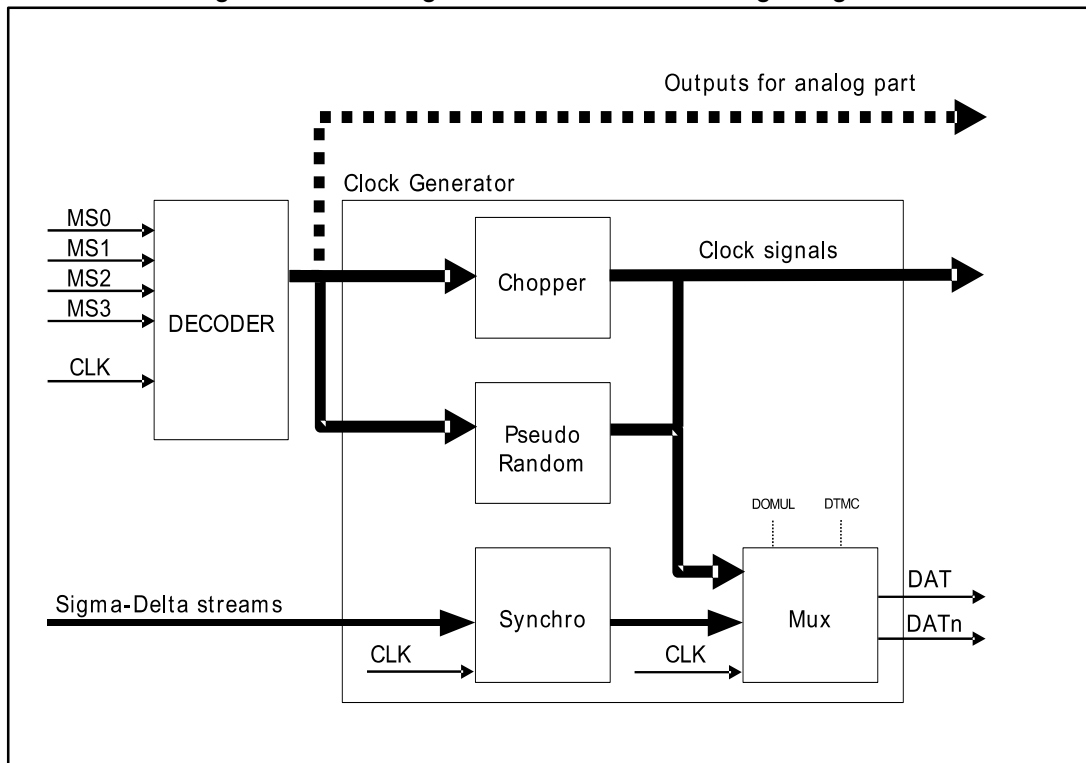


9.3 Functional description of the digital part

The digital section (DFE) includes:

- A decoder for different modes of operation
- A generator for clock frequency
- Level shifters, pull-up stages and power buffers outside the DFE block

Figure 19: Block diagram and definition of DFE digital signals



9.3.1 Decoder for different modes of operations

The decoder defines the operating mode according to the state of the bootstrap MS0, MS1, MS2 and MS3 pins. Two different operational modes can be defined:

- Hard mode: in this case the device configuration is bootstrapped at startup and signals come from VIN and VIP for voltage channels, and CIP and CIN for current channels or from internal BIST DAC.
- Soft mode: in this mode all possible settings from hard mode are accessible, as well as additional settings such as dither and chopper signal frequencies and operation.

9.3.2 Generator for clock frequency

Chopper and BIST frequency generator

The chopper block generates the chopper frequencies and BIST signals for the voltage and current channels. The BIST DAC output levels are appropriately adjusted for the current channel according to the gain selection, while for the voltage channel the max. DC voltage is used. The levels are 300 mV for the voltage channel and 300 mV / 150 mV / 75 mV / 37.5 mV for the current channel, in accordance with gain settings 2/4/8/16, respectively in soft mode, while 300 mV / 37.5 mV based on gain settings 2/16 in hard mode.

Pseudo random

The pseudo random block generates pseudo random signals for the voltage and current channels. These random signals are used to implement a dithering technique to decorrelate the output of the modulators and avoid accumulation points on the frequency spectrum.

Synchro

In synchro block the synchronization of sigma-delta input streams with strobe signals from analog part and clock signal is performed.

Mux

In the mux block signals, connected to output pins DAT and DATn, are selected. In hard mode, the output signals are selected by input pin MS2. In soft mode, the output signals are selected by 8 configuration bits.

9.4 Hard mode

The STPMS2 works in hard mode when input pin MS3 is connected to GND or VCC, as described in [Table 11](#). In hard mode, the STPMS2 has four digital input pins (MS0, MS1, MS2 and MS3) to configure the basic operating parameters:

- BIST DAC enable
- Temperature curve of reference voltage
- Current and voltage channel settings
- Output mode settings

In this manner, 128 different combinations are available and they are controlled by MS0, MS1, MS2 and MS3 pins. MS0 sets the operating mode and amplifier gain selection as described in [Table 8: "Precision mode and input amplifier gain selection"](#).

- MS0 = GND or CLK to select LPR (low precision); $f_{CLK} = 1$ MHz is the typical input clock frequency and low power mode is selected.
- MS0 = NCLK or VCC to select HPR (high precision); $f_{CLK} = 2$ or 4 MHz are the typical input clock frequencies and accuracy is enhanced.

The relative gain of the current channel is selectable between 2 or 16, which defines the maximum differential voltage on the current channel to ± 300 mV or ± 37.5 mV, respectively. The voltage channel gain setting is fixed at 2, which defines the maximum differential voltage on the voltage channel inputs to ± 300 mV.

Table 8: Precision mode and input amplifier gain selection

MS0	Mode	Description
GND	0	LPR, amplifier GAIN selection $g3 = 16$
CLK	1	LPR, amplifier GAIN selection $g0 = 2$
NCLK	2	HPR, amplifier GAIN selection $g0 = 2$
VCC	3	HPR, amplifier GAIN selection $g3 = 16$

MS1 defines the temperature compensation (TC) curve of the internal voltage reference of the STPMS2, as described in [Table 9: "TC of the bandgap reference"](#) (characterized by application). The temperature-compensated reference voltage generator produces $V_{REF} = 1.23$ V. This generator is implemented as a bandgap generator, whose temperature compensation curve can be selected by MS1 configuration pin.

Table 9: TC of the bandgap reference

MS1	Mode	Description
GND	0	TC = 50 ppm/°C
CLK	1	TC = -140 ppm/°C
NCLK	2	TC = 130 ppm/°C
VCC	3	TC = -40 ppm/°C

MS2 defines the outputs of the device. The STPMS2 sends the sigma-delta stream synchronous to the CLK signal. The output mode can be configured according to [Table 10: "Control of voltage channel and output signals"](#) as follows:

- Sigma-delta stream of the output current channel on DAT and the sigma-delta stream of the voltage channel on DATn.
- Output multiplexed signals, so when CLK = 0, the current channel output sigma-delta value is set on the DAT pin, and when CLK = 1, the voltage channel output sigma-delta value is set on the DAT pin. The DATn pin tracks DAT, so DATn = ~DAT.
- Sigma-delta stream of the output current channel on DAT and the sigma-delta stream of the current channel negated on DATn.

Table 10: Control of voltage channel and output signals

MS2	Mode	Description
GND	0	Voltage channel ON, DATn = ~ [DAT =(CLK) ? bsV : bsC]]
CLK	1	Voltage channel OFF, DATn = bsCn, DAT = bsC
NCLK	2	Voltage channel OFF, DATn = bsCn, DAT = bsC
VCC	3	Voltage channel ON, DATn = bsC, DAT = bsV

MS3 enables or disables the BIST DAC output levels. If enabled (MS3=VCC), the input of the modulators, disconnected from VIP pin, VIN, CIP and CIN, and connected to the output of BIST DAC, generates 2 different levels appropriately adjusted for the current channel 300 mV / 37.5 mV depending on gain settings 2/16, while for the voltage channel, 300 mV is used. This mode is used as auto diagnostic methodology of good behavior of the two modulators. When disabled (MS3=GND), the input of the modulators comes from pins VIP, VIN, CIP and CIN. This is the normal operating condition.

Table 11: Selection of hard, soft or test mode and enable of BIST

MS3	Mode	Description
GND	0	Hard mode, BIST mode OFF
CLK	1	Soft mode
NCLK	2	Reserved
VCC	3	Hard mode, BIST mode ON

9.5 Soft mode

The STPMS2 switches to soft mode when MS3 is connected to CLK. In soft mode, input pins (MS0, MS1 and MS2) control the serial communication port, as described in [Table 12: "Pins for SPI communication"](#). All settings of the 40 internal configuration bits can be changed. The old values remain in the registers until they are overwritten.