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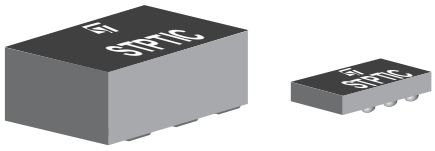
STPTIC

Parascan™ tunable integrated capacitor

Datasheet - production data



µQFN Flip Chip

Features

- High power capability (+36 dBm)
- High tuning range (3.5/1)
- High quality factor (Q)
- High linearity device
- Low leakage current
- Capacitor bias is DC blocked
- Frequency of operation from DC to 3 GHz
- 8 values available: 1.2 pF, 2.7 pF, 3.3 pF, 3.9 pF, 4.7 pF, 5.6 pF, 6.8 pF and 8.2 pF
- Analog control voltage
- Compatible with high voltage control IC (STHVDAC series)
- Available in plastic molded package:
  - µQFN package 1.2 x 1.6 x 0.9 mm
  - Flip Chip 0.65 x 1.0 x 0.3 mm
  - Flip Chip 0.65 x 1.2 x 0.3 mm
- ECOPACK®2 compliant component

Benefit

- RF tunable passive implementation in mobile phones to optimize antenna radiated performances.

Applications

- Cellular Antenna open loop tunable matching network in multi-band GSM/WCDMA/LTE mobile phone
- Open loop tunable RF filters

Description

The ST integrated tunable capacitor, offers excellent RF performance, low power consumption and high linearity required in adaptive RF tuning applications. The fundamental building block of PTIC is a tunable material called Parascan, which is a version of barium strontium titanate (BST) developed by Paratek microwave.

BST capacitances are tunable capacitances intended for use in mobile phone application, and dedicated to RF tunable applications. These tunable capacitances are controlled through a bias voltage ranging from 2 to 20 V. The use of BST tunable capacitance in mobile phones enables significant improvement in terms of radiated performances making the performance almost insensitive to the external environment.

TM: Parascan is a trade mark of Paratek microwave Inc.

1 Functional characteristics

Figure 1. PTIC functional block diagram

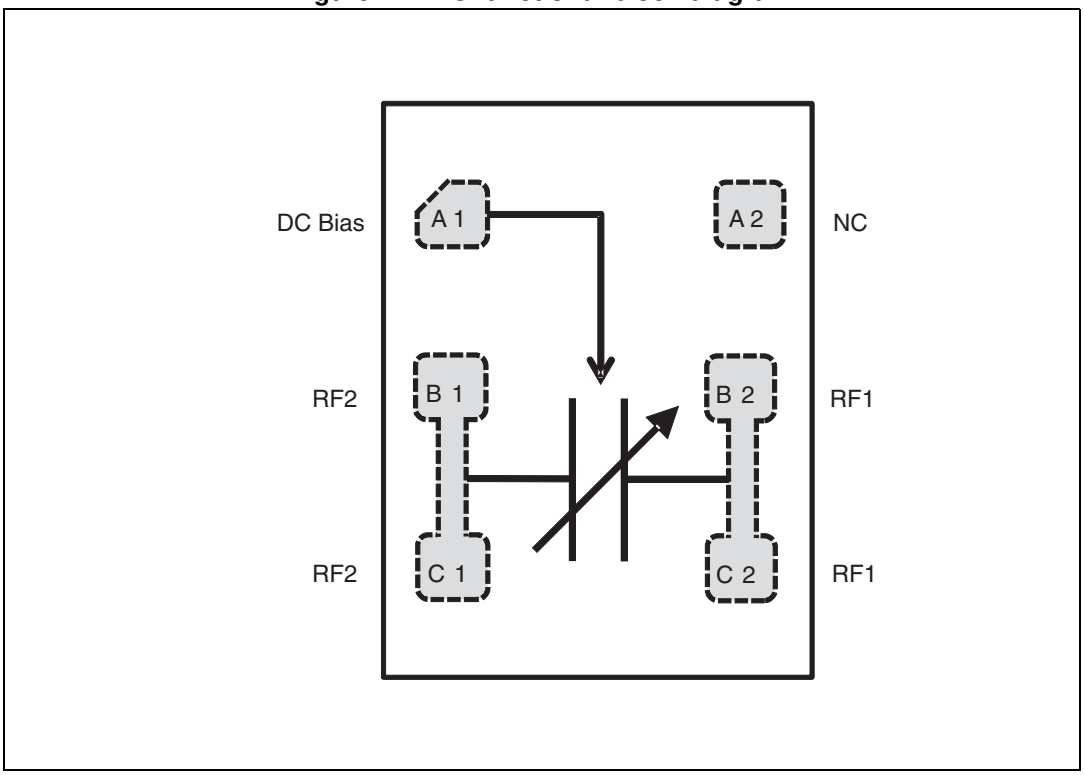


Table 1. Signal descriptions

Ball/Pad number	Pin name	Description
A1	DC BIAS	DC bias voltage
B1	RF2	RF input / output
C1	RF2	RF input / output
A2	NC	Not connected
B2	RF1	RF input / output
C2	RF1	RF input / output

2 Electrical characteristics

Table 2. Absolute maximum ratings (limiting values)

Symbol	Parameter		Rating	Unit
P_{IN}	Input peak power RF_{IN} (CW mode)/all RF ports		+36	dBm
$V_{ESD(HBM)}$	Human body model, JESD22-A114-B, all I/O	STPTIC-12	500	V
		STPTIC-27	400(1)	
		STPTIC-33	400(1)	
		STPTIC-39	500	
		STPTIC-47	500	
		STPTIC-56	500	
		STPTIC-68	500	
		STPTIC-82	500	
$V_{ESD(MM)}$	Machine model, JESD22-A114-B, all I/O		100	V
T_{device}	Device temperature		+125	°C
T_{stg}	Storage temperature		-55 to +150	
V_x	Bias voltage		25	V

1. Currently failing around 400 V, improvement on going to withstand 500 V on 2p7 and 3p3.

Table 3. Recommended operating conditions

Symbol	Parameter	Rating			Unit
		Min.	Typ.	Max.	
P_{IN}	RF input power (50% duty cycle mode) RF_{IN} (LB) RF_{IN} (HB)			 +35 +33	dBm
F_{OP}	Operating frequency	700		3000	MHz
T_{device}	Device temperature			+100	°C
T_{OP}	Operating temperature	-30		+85	
V_x	Bias voltage	2		20	V

Table 4. Representative performances (T_{amb} = 25 °C)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
C_{2V}	Capacitance at 2V bias	STPTIC-12	1.08	1.20	1.32	pF
		STPTIC-27	2.43	2.7	2.97	pF
		STPTIC-33	2.97	3.3	3.63	pF
		STPTIC-39	3.51	3.9	4.29	pF
		STPTIC-47	4.23	4.7	5.17	pF
		STPTIC-56	5.04	5.6	6.16	pF
		STPTIC-68	6.12	6.8	7.48	pF
		STPTIC-82	7.38	8.2	9.02	
I_L	Leakage current	Measured with V_{bias} = 20 V			100	nA
ΔC	Tuning range	Ratio between C_{2V}/C_{20V} measured at 100 kHz	3/1	3.5/1		
Q_{LB}	Quality factor	Measured at 900 MHz		65		
Q_{HB}	Quality factor	Measured at 1800 MHz		45		
IP3	Third order intercept point	V_{bias} = 2 V(1) and (3)		60		dBm
		V_{bias} = 20 V(1) and (3)		70		dBm
H2	Second harmonic	V_{bias} = 2 V(2) and (3)		-65		dBm
		V_{bias} = 20 V(2) and (3)		-65		dBm
H3	Third harmonic	V_{bias} = 2 V(2) and (3)		-45		dBm
		V_{bias} = 20 V(2) and (3)		-45		dBm
t_T	Transition time	From C_{min} to C_{max} (4)		135		µs
		From C_{max} to C_{min}(4)		100		µs

1. F_1 = 894 MHz, F_2 = 849 MHz, P_1 = 20 dBm, P_2 = -15 dBm, $2f_1 - f_2$ = 939 MHz
2. 894 MHz, P_{in} = 34 dBm
3. IP3 and harmonics are measured in the shunt/series configuration in a 50 Ω environment
4. One or both of RF_{in} and RF_{out} must be connected to DC ground

3 Package information

- Epoxy meets UL94, V0
- Lead-free package

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 2. µQFN-6L package dimension

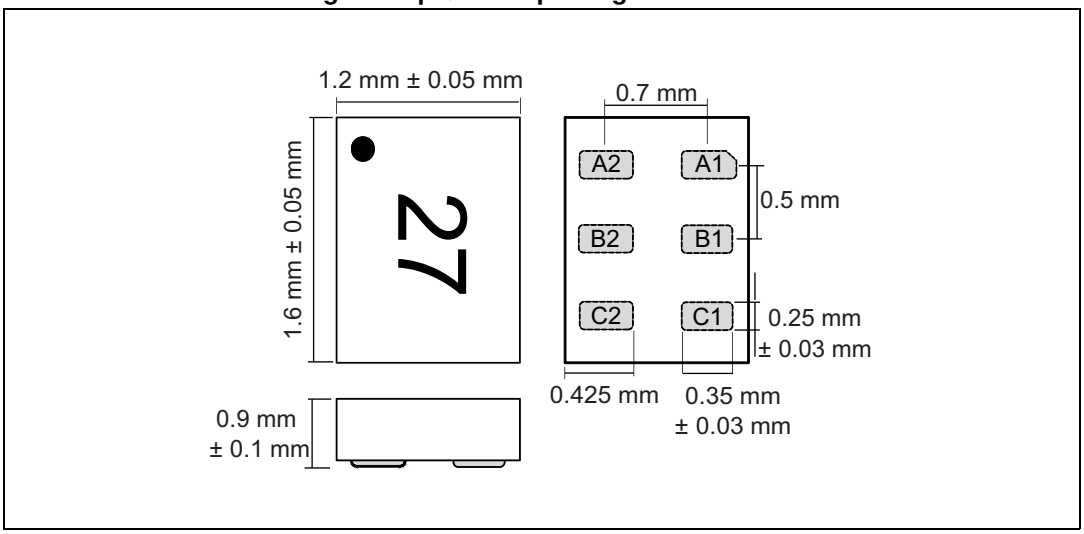


Figure 3. Recommended PCB land pattern for µQFN-6L package

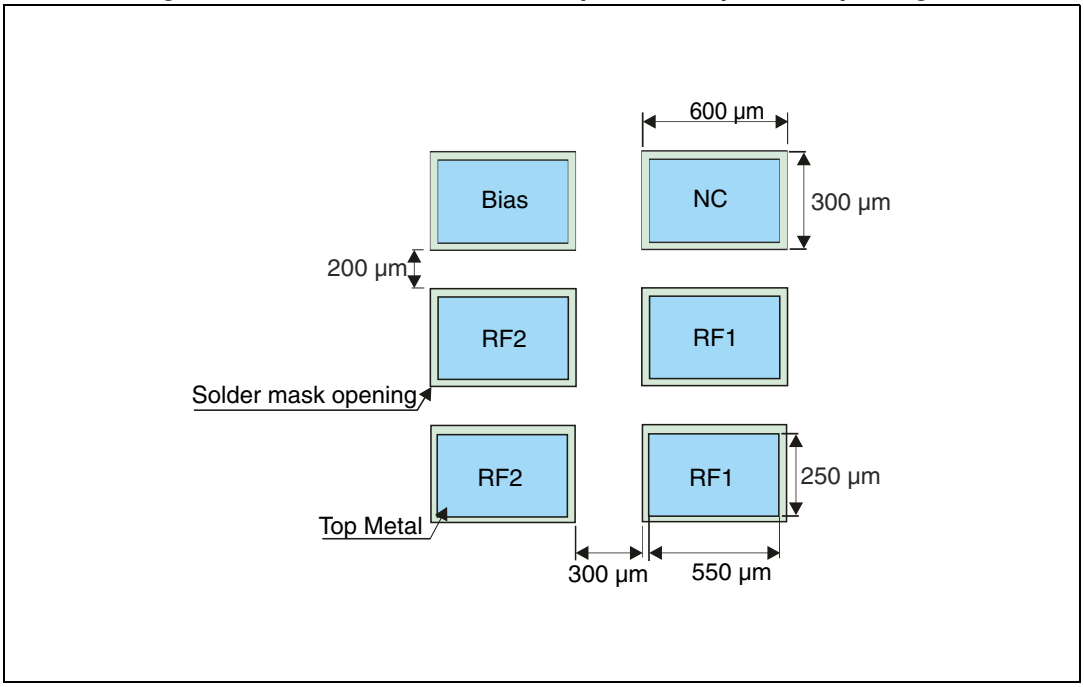


Figure 4. Flip Chip dimensions (size for 1p5)

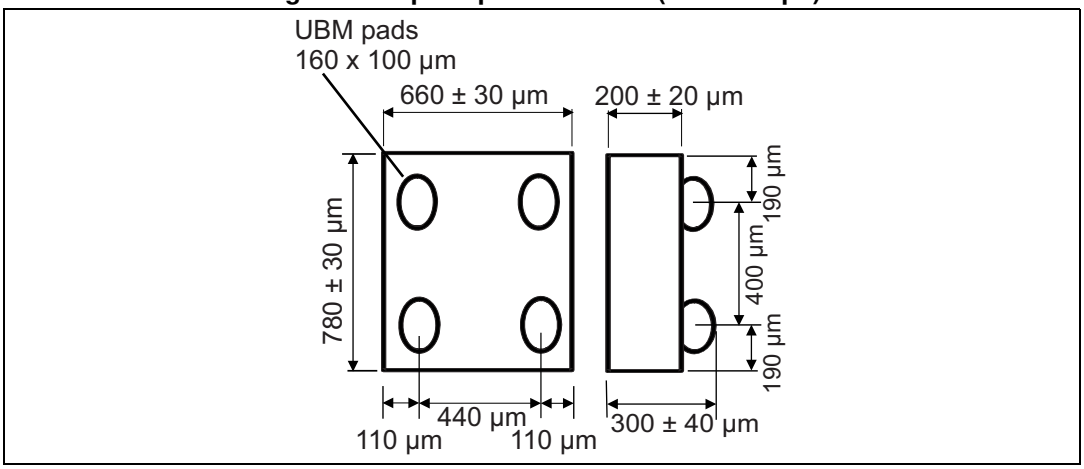


Figure 5. Flip Chip dimensions (size for 2p7, 3p3, 3p9, and 4p7)

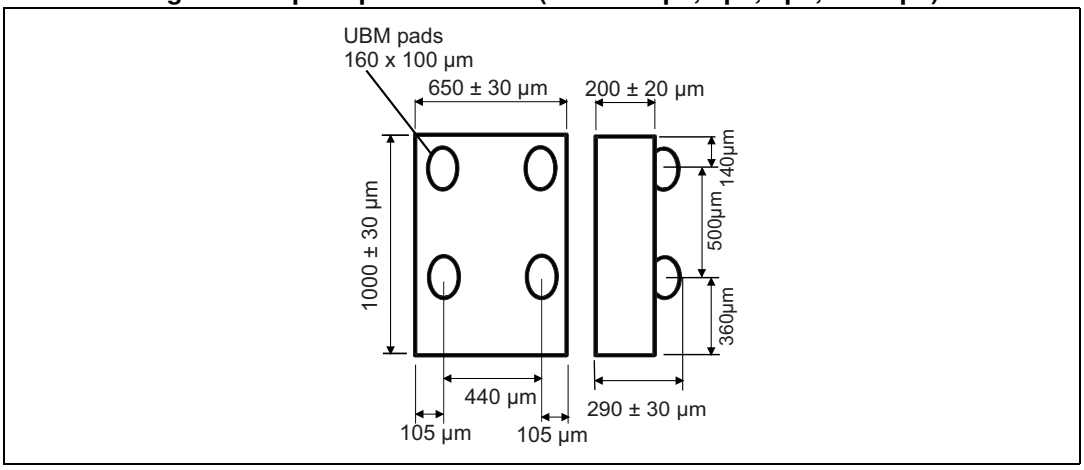


Figure 6. Flip Chip dimensions (size for 5p6, 6p8, 8p2)

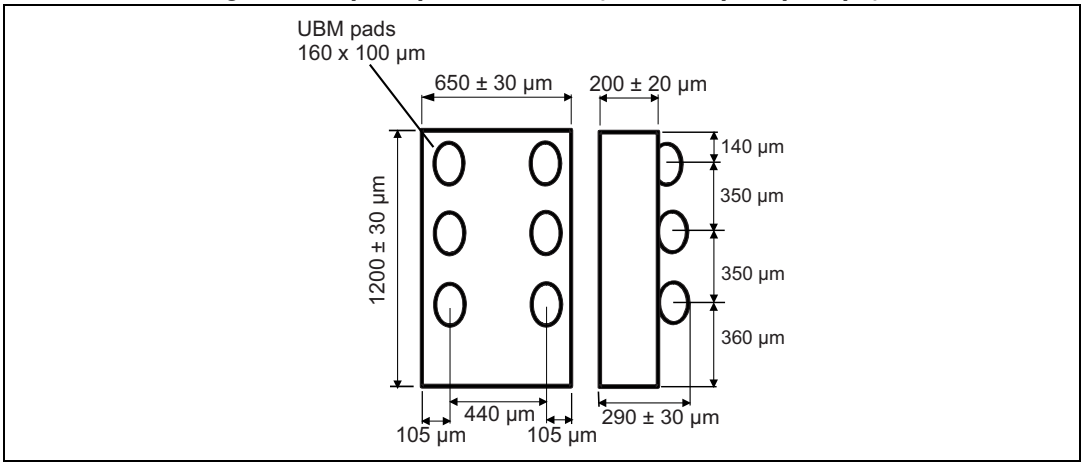


Figure 7. Recommended PCB land pattern for Flip Chip package (metal defined pads, solder mask 25 µm larger)

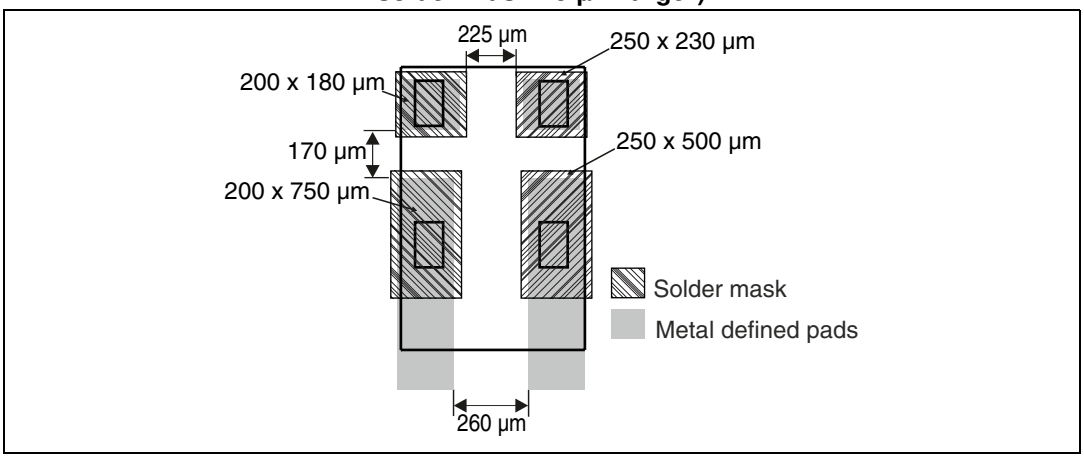


Figure 8. Recommended PCB land pattern for Flip Chip PTIC (die size 650 x 1200)

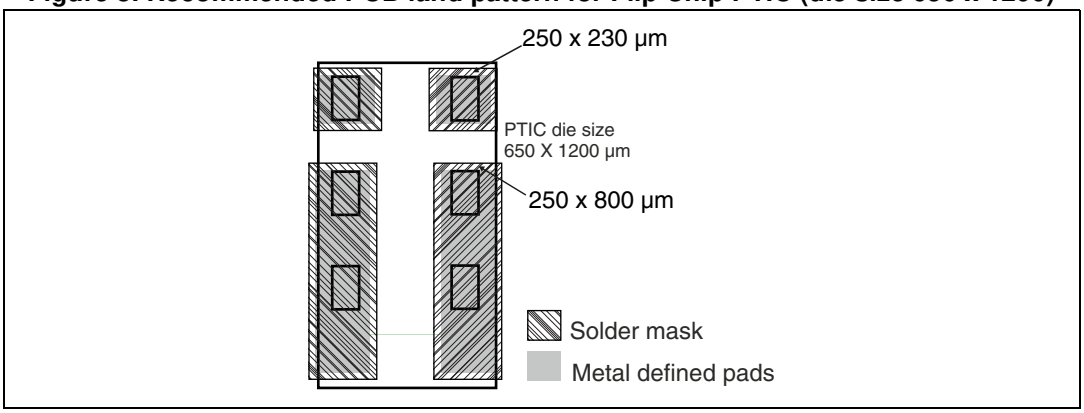


Figure 9. µQFN-6L tape and reel specification

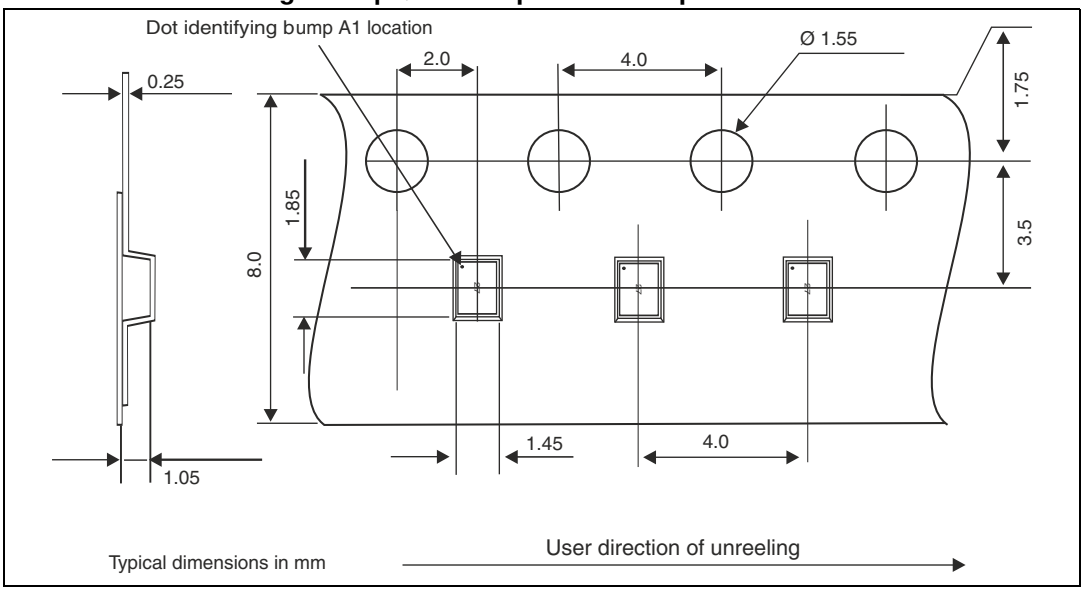


Figure 10. Flip Chip tape and reel specification

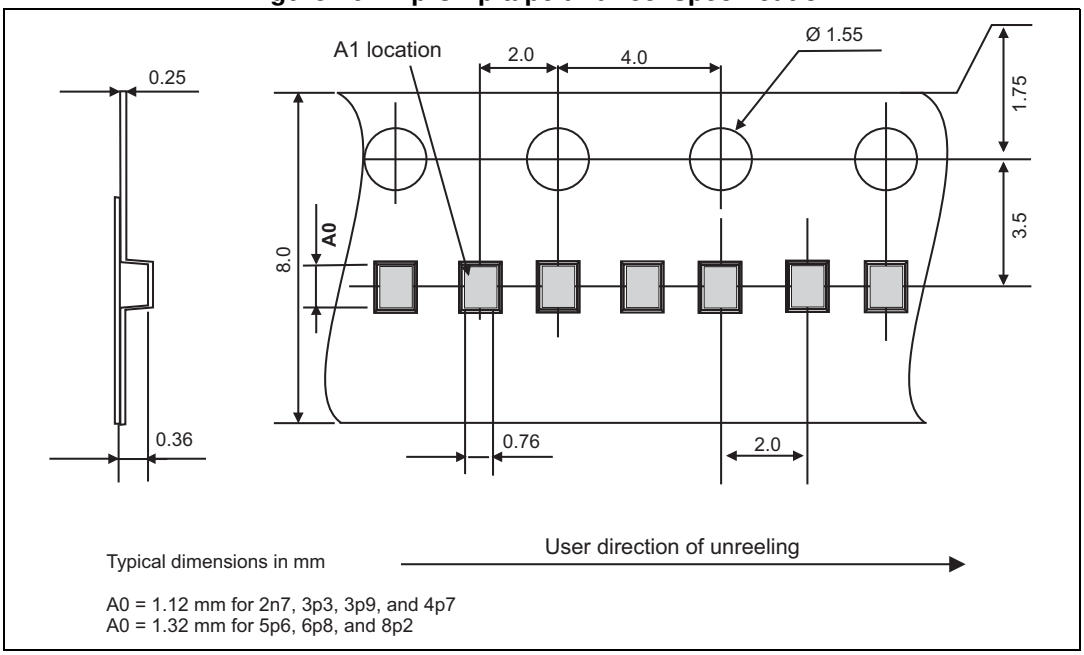


Figure 11. µQFN marking

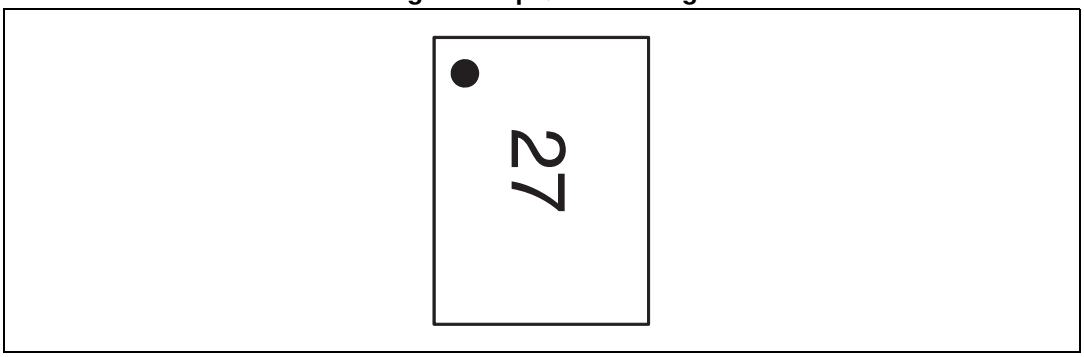
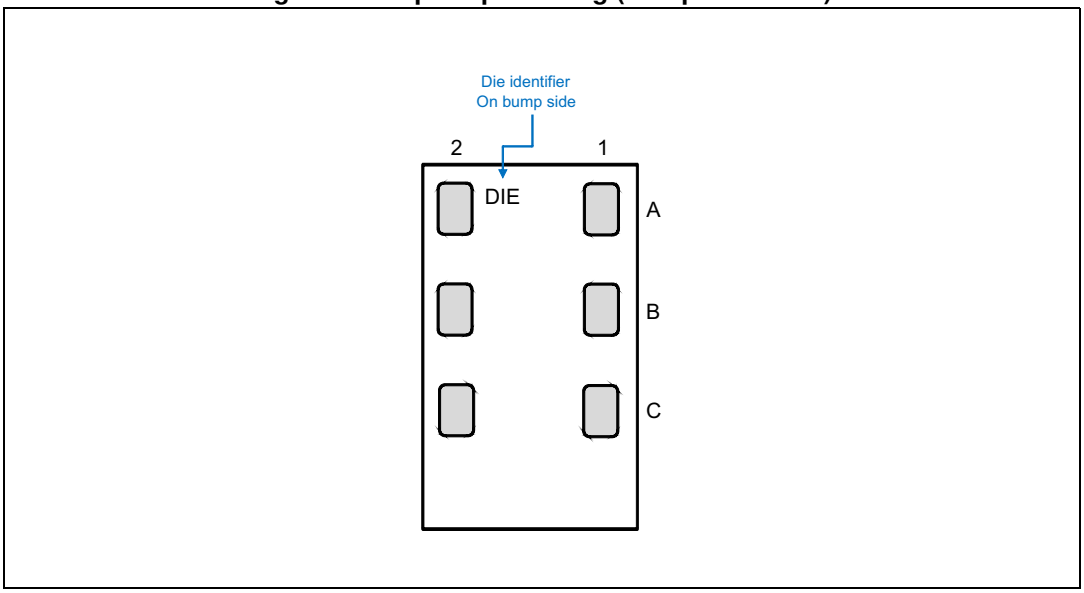
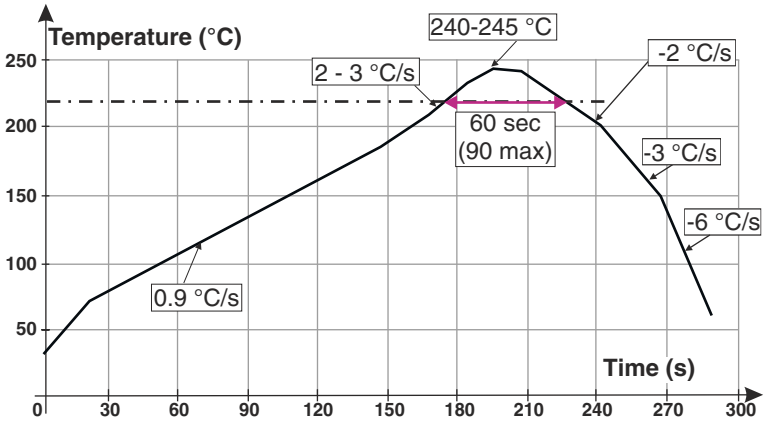


Figure 12. Flip Chip marking (bump side view)



4 Reflow profile

Figure 13. ST ECOPACK® recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement.

Table 5. Recommended values for soldering reflow

Profile	Value	
	Typical	Max.
Temperature gradient in preheat (T = 70-180 °C)	0.9 °C/s	3 °C/s
Temperature gradient (T = 200-225 °C)	2 °C/s	3 °C/s
Peak temperature in reflow	240-245 °C	260 °C
Time above 220 °C	60 s	90 s
Temperature gradient in cooling	-2 to -3 °C/s	-6 °C/s
Time from 50 to 220 °C	160 to 220 s	

5 Ordering information

Figure 14. Ordering information scheme

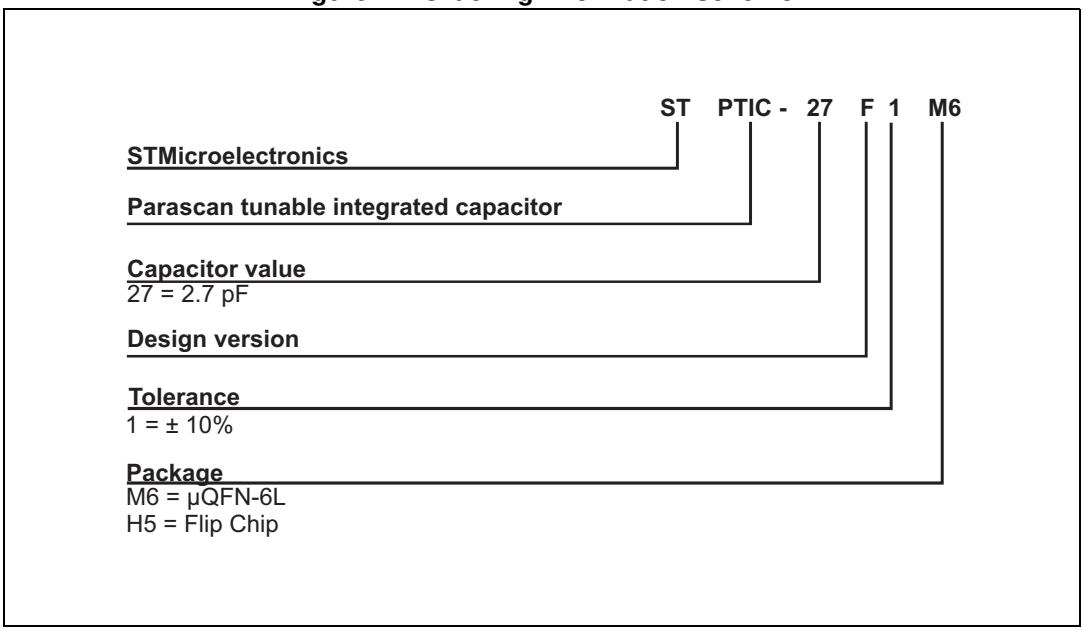


Table 6. Ordering information

Part Number	Marking	Weight	Base Qty	Delivery Mode
STPTIC-12F1M6	12	4.8 mg	3000	Tape and reel
STPTIC-27F1M6	27	4.8 mg	3000	Tape and reel
STPTIC-33F1M6	33	4.8 mg	3000	Tape and reel
STPTIC-39F1M6	39	4.8 mg	3000	Tape and reel
STPTIC-47F1M6	47	4.8 mg	3000	Tape and reel
STPTIC-56F1M6	56	4.8 mg	3000	Tape and reel
STPTIC-68F1M6	68	4.8 mg	3000	Tape and reel
STPTIC-82F1M6	82	4.8 mg	3000	Tape and reel
STPTIC-12G1H5	TBD	0.7 mg	15000	Tape and reel
STPTIC-27G1H5	I1x	0.7 mg	15000	Tape and reel
STPTIC-33G1H5	I3x	0.7 mg	15000	Tape and reel
STPTIC-39G1H5	I2x	0.7 mg	15000	Tape and reel
STPTIC-47G1H5	I5x	0.7 mg	15000	Tape and reel
STPTIC-56G1H5	I4x	0.7 mg	15000	Tape and reel
STPTIC-68G1H5	I7x	0.7 mg	15000	Tape and reel
STPTIC-82G1H5	I6x	0.7 mg	15000	Tape and reel

6 Revision history

Table 7. Document revision history

Date	Revision	Changes
02-Nov-2012	1	Initial release.
03-Jul-2013	2	Removed 6-pad 650 x 1000 Flip-Chip package.
10-Jan-2014	3	updated: *Features*, *Table 2*, *Table 4*, *Table 6* and added new *Figure 4*.
13-Feb-2014	4	Updated *Applications*.