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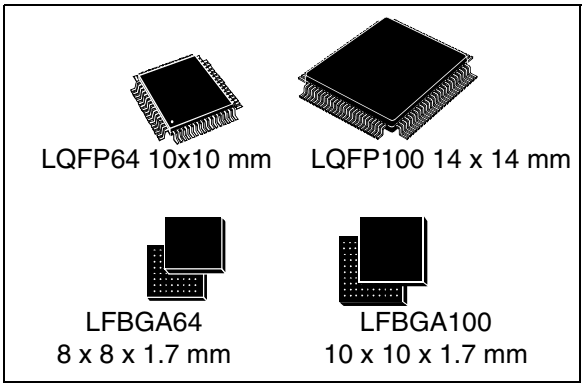
STR750Fxx STR751Fxx STR752Fxx STR755Fxx

ARM7TDMI-S™ 32-bit MCU with Flash, SMI, 3 std 16-bit timers, PWM timer, fast 10-bit ADC, I2C, UART, SSP, USB and CAN

Features

- Core
  - ARM7TDMI-S 32-bit RISC CPU
  - 54 DMIPS @ 60 MHz
- Memories
  - Up to 256 KB Flash program memory (10k W/E cycles, retention 20 yrs @ 85°C)
  - 16 KB Read-While-Write Flash for data (100k W/E cycles, retention 20 yrs@ 85°C)
  - Flash Data Readout and Write Protection
  - 16KBytes embedded high speed SRAM
  - Memory mapped interface (SMI) to ext. Serial Flash (64 MB) w. boot capability
- Clock, reset and supply management
  - Single supply 3.3V ±10% or 5V ±10%
  - Embedded 1.8V Voltage Regulators
  - Int. RC for fast start-up and backup clock
  - Up to 60 MHz operation using internal PLL with 4 or 8 MHz crystal/ceramic osc.
  - Smart Low Power Modes: SLOW, WFI, STOP and STANDBY with backup registers
  - Real-time Clock, driven by low power internal RC or 32.768 kHz dedicated osc, for clock-calendar and Auto Wake-up
- Nested interrupt controller
  - Fast interrupt handling with 32 vectors
  - 16 IRQ priorities, 2 maskable FIQ sources
  - 16 external interrupt / wake-up lines
- DMA
  - 4-channel DMA controller
  - Circular buffer management
  - Support for UART, SSP, Timers, ADC
- 6 Timers
  - 16-bit watchdog timer (WDG)
  - 16-bit timer for system timebase functions
  - 3 synchronizable timers each with up to 2 input captures and 2 output compare/PWMs.



  - 16-bit 6-ch. synchronizable PWM timer
  - Dead time generation, edge/center-aligned waveforms and emergency stop
  - Ideal for induction/brushless DC motors
- 8 Communications interfaces
  - 1 I^2C interface
  - 3 HiSpeed UARTs w. Modem/LIN capability
  - 2 SSP interfaces (SPI or SSI) up to 16 Mb/s
  - 1 CAN interface (2.0B Active)
  - 1 USB full-speed 12 Mb/s interface with 8 configurable endpoint sizes
- 10-bit A/D converter
  - 16/11 chan. with prog. Scan Mode & FIFO
  - Programmable Analog Watchdog feature
  - Conversion time: min. 3.75 µs
  - Start conversion can be triggered by timers
- Up to 72/38 I/O ports
  - 72/38 GPIOs with High Sink capabilities
  - Atomic bit SET and RES operations

Table 1. Device summary

Reference	Part number
STR750Fxx	STR750FV0, STR750FV1, STR750FV2
STR751Fxx	STR751FR0, STR751FR1, STR751FR2
STR752Fxx	STR752FR0, STR752FR1, STR752FR2
STR755Fxx	STR755FR0, STR755FR1, STR755FR2 STR755FV0, STR755FV1, STR755FV2

Contents

1 Description

The STR750 family of 32-bit microcontrollers combines the industry-standard ARM7TDMI® 32-bit RISC core, featuring high performance, very low power, and very dense code, with a comprehensive set of peripherals and ST's latest 0.18µ embedded Flash technology. The STR750 family comprises a range of devices integrating a common set of peripherals as well as USB, CAN and some key innovations like clock failure detection and an advanced motor control timer. It supports both 3.3V and 5V, and it is also available in an extended temperature range (-40 to +105°C). This makes it a genuine general purpose microcontroller family, suitable for a wide range of applications:

- Appliances, brushless motor drives
- USB peripherals, UPS, alarm systems
- Programmable logic controllers, circuit breakers, inverters
- Medical and portable equipment

2 Device overview

Table 2. Device overview

Features	STR755FR0 STR755FR1 STR755FR2	STR751FR0/ STR751FR1/ STR751FR2	STR752FR0/ STR752FR1/ STR752FR2	STR755FV0 STR755FV1/ STR755FV2	STR750FV0/ STR750FV1/ STR750FV2
Flash - Bank 0 (bytes)	64K/128K/256K				
Flash - Bank 1 (bytes)	16K RWW				
RAM (bytes)	16K				
Operating Temperature.	Ambient temp.:-40 to +85°C / -40 to +105°C (see *Table 49*) Junction temp. -40 to + 125 °C (see *Table 10*)				
Common Peripherals	3 UARTs, 2 SSPs, 1 I2C, 3 timers 1 PWM timer, 38 I/Os 13 Wake-up lines, 11 A/D Channels			3 UARTs, 2 SSPs, 1 I^2C, 3 timers 1 PWM timer, 72 I/Os 15 Wake-up lines, 16 A/D Channels	
USB/CAN peripherals	None	USB	CAN	None	USB+CAN
Operating Voltage	3.3V or 5V	3.3V	3.3V or 5V		
Packages (**x**)	**T**=LQFP64 10x10, **H**=LFBGA64			**T**=LQFP100 14x14, **H**=LFBGA100	

3 Introduction

This Datasheet contains the description of the STR750F family features, pinout, Electrical Characteristics, Mechanical Data and Ordering information.

For complete information on the Microcontroller memory, registers and peripherals. Please refer to the STR750F Reference Manual.

For information on the ARM7TDMI-S core please refer to the ARM7TDMI-S Technical Reference Manual available from Arm Ltd.

For information on programming, erasing and protection of the internal Flash memory please refer to the STR7 Flash Programming Reference Manual

For information on third-party development tools, please refer to the http://www.st.com/mcu website.

3.1 Functional description

The STR750F family includes devices in 2 package sizes: 64-pin and 100-pin. Both types have the following common features:

ARM7TDMI-S™ core with embedded Flash & RAM

STR750F family has an embedded ARM core and is therefore compatible with all ARM tools and software. It combines the high performance ARM7TDMI-S™ CPU with an extensive range of peripheral functions and enhanced I/O capabilities. All devices have on-chip high-speed single voltage FLASH memory and high-speed RAM.

Figure 1 shows the general block diagram of the device family.

Embedded Flash memory

Up to 256 KBytes of embedded Flash is available in Bank 0 for storing programs and data. An additional Bank 1 provides 16 Kbytes of RWW (Read While Write) memory allowing it to be erased/programmed on-the-fly. This partitioning feature is ideal for storing application parameters.

- When configured in burst mode, access to Flash memory is performed at CPU clock speed with 0 wait states for sequential accesses and 1 wait state for random access (maximum 60 MHz).
- When not configured in burst mode, access to Flash memory is performed at CPU clock speed with 0 wait states (maximum 32 MHz)

Embedded SRAM

16 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states.

Enhanced interrupt controller (EIC)

In addition to the standard ARM interrupt controller, the STR750F embeds a nested interrupt controller able to handle up to 32 vectors and 16 priority levels. This additional hardware block provides flexible interrupt management features with minimal interrupt latency.

Serial memory interface (SMI)

The Serial Memory interface is directly able to access up to 4 serial FLASH devices. It can be used to access data, execute code directly or boot the application from external memory. The memory is addressed as 4 banks of up to 16 Mbytes each.

Clocks and start-up

After RESET or when exiting from Low Power Mode, the CPU is clocked immediately by an internal RC oscillator (FREEOSC) at a frequency centered around 5 MHz, so the application code can start executing without delay. In parallel, the 4/8 MHz Oscillator is enabled and its stabilization time is monitored using a dedicated counter.

An oscillator failure detection is implemented: when the clock disappears on the XT1 pin, the circuit automatically switches to the FREEOSC oscillator and an interrupt is generated.

In Run mode, the AHB and APB clock speeds can be set at a large number of different frequencies thanks to the PLL and various prescalers: up to 60 MHz for AHB and up to 32 MHz for APB when fetching from Flash (64 MHz and 32 MHz when fetching from SRAM).

In SLOW mode, the AHB clock can be significantly decreased to reduce power consumption.

The built-in Clock Controller also provides the 48 MHz USB clock directly without any extra oscillators or PLL. For instance, starting from the 4 MHz crystal source, it is possible to obtain in parallel 60 MHz for the AHB clock, 48 MHz for the USB clock and 30 MHz for the APB peripherals.

Boot modes

At start-up, boot pins are used to select one of five boot options:

- Boot from internal flash
- Boot from external serial Flash memory
- Boot from internal boot loader
- Boot from internal SRAM

Booting from SMI memory allows booting from a serial flash. This way, a specific boot monitor can be implemented. Alternatively, the STR750F can boot from the internal boot loader that implements a boot from UART.

Power supply schemes

You can connect the device in any of the following ways depending on your application.

- **Power Scheme 1: Single external 3.3V power source**. In this configuration the V_{CORE} supply required for the internal logic is generated internally by the main voltage regulator and the V_{BACKUP} supply is generated internally by the low power voltage regulator. This scheme has the advantage of requiring only one 3.3V power source.
- **Power Scheme 2: Dual external 3.3V and 1.8V power sources.** In this configuration, the internal voltage regulators are switched off by forcing the VREG_DIS pin to high level. V_{CORE} is provided externally through the V_{18} and V_{18REG} power pins and V_{BACKUP} through the V_{18_BKP} pin. This scheme is intended to save power consumption for applications which already provide an 1.8V power supply.
- **Power Scheme 3: Single external 5.0V power source.** In this configuration the V_{CORE} supply required for the internal logic is generated internally by the main voltage

regulator and the V_{BACKUP} supply is generated internally by the low power voltage regulator. This scheme has the advantage of requiring only one 5.0V power source.

- **Power Scheme 4: Dual external 5.0V and 1.8V power sources.** In this configuration, the internal voltage regulators are switched off, by forcing the VREG_DIS pin to high level. V_{CORE} is provided externally through the V_{18} and V_{18REG} power pins and V_{BACKUP} through the V_{18_BKP} pin. This scheme is intended to provide 5V I/O capability.

Caution: When powered by 5.0V, the USB peripheral cannot operate.

Low power modes

The STR750F supports 5 low power modes, SLOW, PCG, WFI, STOP and STANDBY.

- SLOW MODE: the system clock speed is reduced. Alternatively, the PLL and the main oscillator can be stopped and the device is driven by a low power clock (f_{RTC}). The clock is either an external 32.768 kHz oscillator or the internal low power RC oscillator.
- PCG MODE (Peripheral Clock Gating MODE): When the peripherals are not used, their APB clocks are gated to optimize the power consumption.
- WFI MODE (Wait For Interrupts): only the CPU clock is stopped, all peripherals continue to work and can wake-up the CPU when IRQs occur.
- STOP MODE: all clocks/peripherals are disabled. It is also possible to disable the oscillators and the Main Voltage Regulator (In this case the V_{CORE} is entirely powered by V_{18_BKP}). This mode is intended to achieve the lowest power consumption with SRAM and registers contents retained. The system can be woken up by any of the external interrupts / wake-up lines or by the RTC timer which can optionally be kept running. The RTC can be clocked either by the 32.768 kHz Crystal or the Low Power RC Oscillator.
  Alternatively, STOP mode gives flexibility to keep the either main oscillator, or the Flash or the Main Voltage Regulator enabled when a fast start after wake-up is preferred (at the cost of some extra power consumption).
- STANDBY MODE: This mode (only available in single supply power schemes) is intended to achieve the lowest power consumption even when the temperature is increasing. The digital power supply (V_{CORE}) is completely removed (no leakage even at high ambient temperature). SRAM and all register contents are lost. Only the RTC remains powered by V_{18_BKP}. The STR750F can be switched back from STANDBY to RUN mode by a trigger event on the WKP_STDBY pin or an alarm timeout on the RTC counter.

Caution: It is important to bear in mind that it is forbidden to remove power from the V_{DD_IO} power supply in any of the Low Power Modes (even in STANDBY MODE).

DMA

The flexible 4-channel general-purpose DMA is able to manage memory to memory, peripheral to memory and memory to peripheral transfers. The DMA controller supports circular buffer management avoiding the generation of interrupts when the controller reaches the end of the buffer.

The DMA can be used with the main peripherals: UART0, SSP0, Motor control PWM timer (PWM), standard timer TIM0 and ADC.

RTC (real-time clock)

The real-time clock provides a set of continuously running counters which can be used with suitable software to provide a clock calendar function, and provides an alarm interrupt and a

periodic interrupt. It is clocked by an external 32.768 kHz oscillator or the internal low power RC oscillator. The RC has a typical frequency of 300 kHz and can be calibrated.

WDG (watchdog timer)

The watchdog timer is based on a 16-bit downcounter and 8-bit prescaler. It can be used as watchdog to reset the device when a problem occurs, or as free running timer for application time out management.

Timebase timer (TB)

The timebase timer is based on a 16-bit auto-reload counter and not connected to the I/O pins. It can be used for software triggering, or to implement the scheduler of a real-time operating system.

Synchronizable standard timers (TIM2:0)

The three standard timers are based on a 16-bit auto-reload counter and feature up to 2 input captures and 2 output compares (for external triggering or time base / time out management). They can work together with the PWM timer via the Timer Link feature for synchronization or event chaining. In reset state, timer Alternate Function I/Os are connected to the same
I/O ports in both 64-pin and 100-pin devices. To optimize timer functions in 64-pin devices, timer Alternate Function I/Os can be connected, or “remapped”, to other I/O ports as summarized in *Table 3* and detailed in *Table 6*. This remapping is done by the application via a control register.

Table 3. Standard timer alternate function I/Os

Standard timer functions		Number of alternate function I/Os		
		100-pin package	64-pin package	
			Default mapping	Remapped
TIM 0	Input Capture	2	1	2
	Output Compare/PWM	2	1	2
TIM 1	Input Capture	2	1	1
	Output Compare/PWM	2	1	1
TIM 2	Input Capture	2	2	2
	Output Compare/PWM	2	1	2

Any of the standard timers can be used to generate PWM outputs. One timer (TIM0) is mapped to a DMA channel.

Motor control PWM timer (PWM)

The Motor Control PWM Timer (PWM) can be seen as a three-phase PWM multiplexed on 6 channels. The 16-bit PWM generator has full modulation capability (0...100%), edge or centre-aligned patterns and supports dead-time insertion. It has many features in common with the standard TIM timers which has the same architecture and it can work together with the TIM timers via the Timer Link feature for synchronization or event chaining.The PWM timer is mapped to a DMA channel.

I²C bus

The I²C bus interface can operate in multi-master and slave mode. It can support standard and fast modes (up to 400KHz).

High speed universal asynch. receiver transmitter (UART)

The three UART interfaces are able to communicate at speeds of up to 2 Mbit/s. They provide hardware management of the CTS and RTS signals and have LIN Master capability.

To optimize the data transfer between the processor and the peripheral, two FIFOs (receive/transmit) of 16 bytes each have been implemented.

One UART can be served by the DMA controller (UART0).

Synchronous serial peripheral (SSP)

The two SSPs are able to communicate up to 8 Mbit/s (SSP1) or up to 16 Mbit/s (SSP0) in standard full duplex 4-pin interface mode as a master device or up to 2.66 Mbit/s as a slave device. To optimize the data transfer between the processor and the peripheral, two FIFOs (receive/transmit) of 8 x 16 bit words have been implemented. The SSPs support the Motorola SPI or TI SSI protocols.

One SSP can be served by the DMA controller (SSP0).

Controller area network (CAN)

The CAN is compliant with the specification 2.0 part B (active) with a bit rate up to 1Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. Up to 32 message objects are handled through an internal RAM buffer. In LQFP64 devices, CAN and USB cannot be connected simultaneously.

Universal serial bus (USB)

The STR750F embeds a USB device peripheral compatible with the USB Full speed 12Mbs. The USB interface implements a full speed (12 Mbit/s) function interface. It has software configurable endpoint setting and suspend/resume support. The dedicated 48 MHz clock source is generated from the internal main PLL. V_{DD} must be in the range 3.3V±10% for USB operation.

ADC (analog to digital converter)

The 10-bit Analog to Digital Converter, converts up to 16 external channels (11 channels in 64-pin devices) in single-shot or scan modes. In scan mode, continuous conversion is performed on a selected group of analog inputs. The minimum conversion time is 3.75 µs (including the sampling time).
The ADC can be served by the DMA controller.

An analog watchdog feature allows you to very precisely monitor the converted voltage of up to four channels. An IRQ is generated when the converted voltage is outside the programmed thresholds.

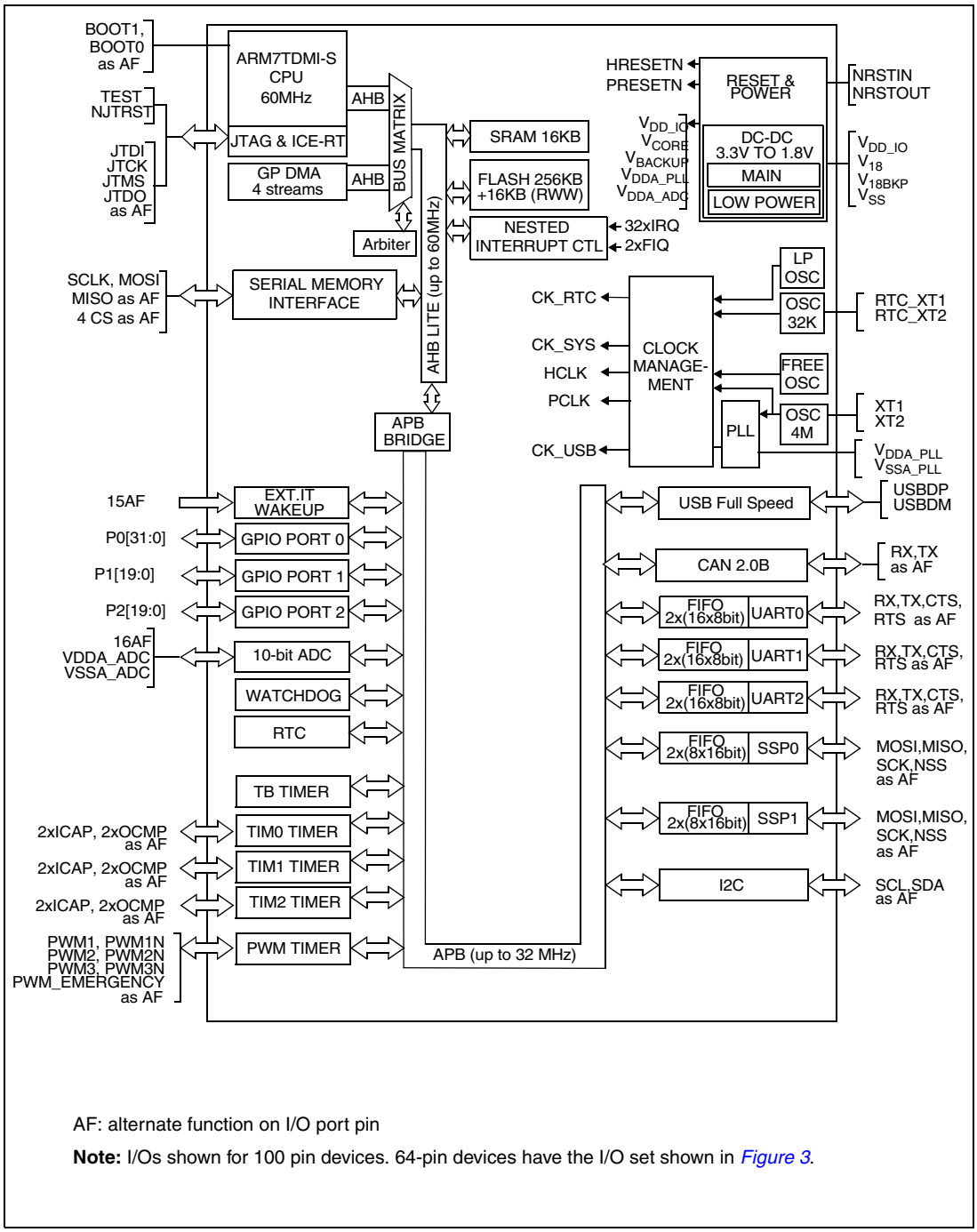
The events generated by TIM0, TIM2 and PWM timers can be internally connected to the ADC start trigger, injection trigger, and DMA trigger respectively, to allow the application to synchronize A/D conversion and timers.

GPIOs (general purpose input/output)

Each of the 72 GPIO pins (38 GPIOs in 64-pin devices) can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as Peripheral Alternate Function. Port 1.15 is an exception, it can be used as general-purpose input only or wake-up from STANDBY mode (WKP_STDBY). Most of the GPIO pins are shared with digital or analog alternate functions.

3.2 Block diagram

Figure 1. STR750 block diagram



AF: alternate function on I/O port pin

Note: I/Os shown for 100 pin devices. 64-pin devices have the I/O set shown in *Figure 3*.

4 Pin description

Figure 2. LQFP100 pinout

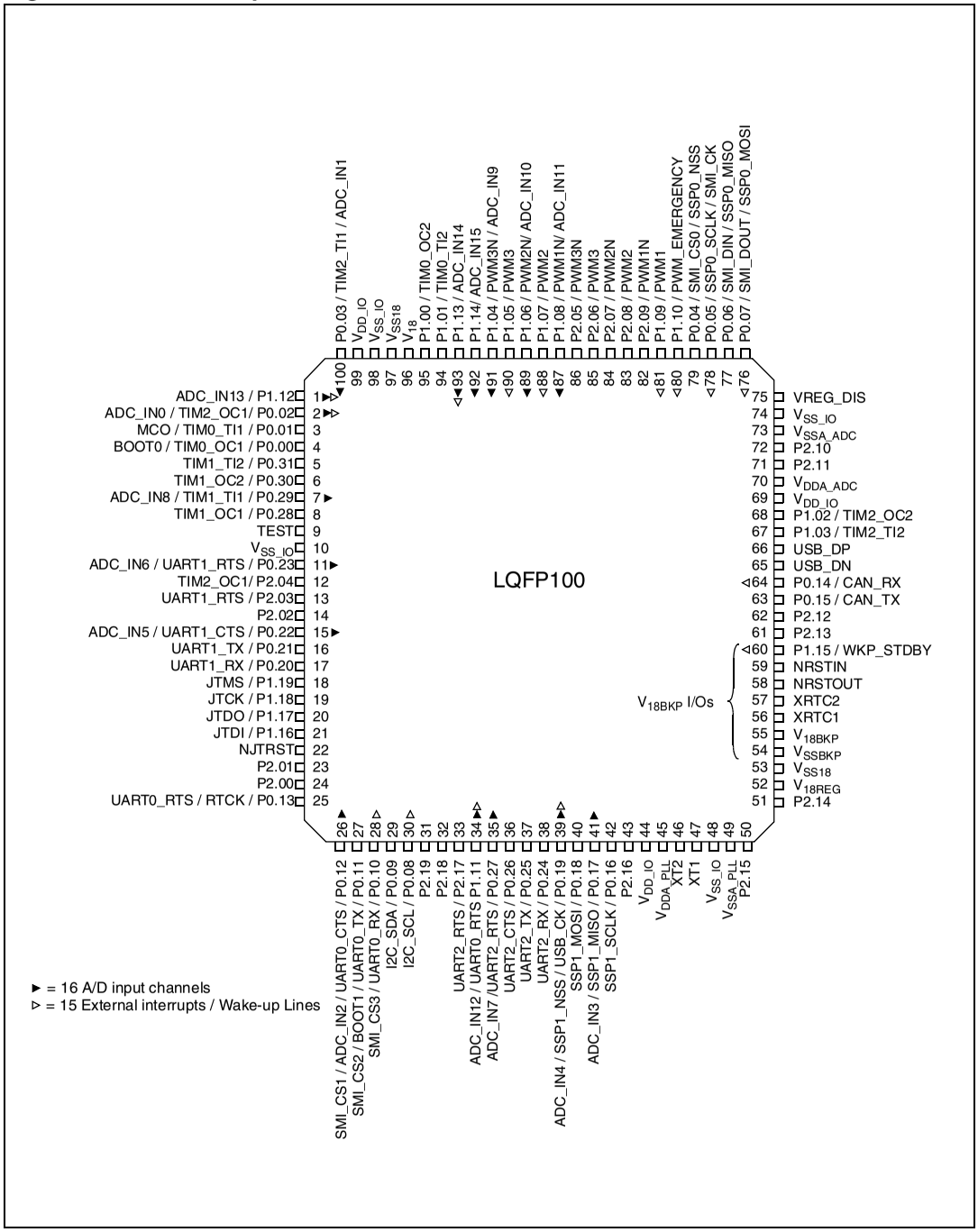


Figure 3. LQFP64 pinout

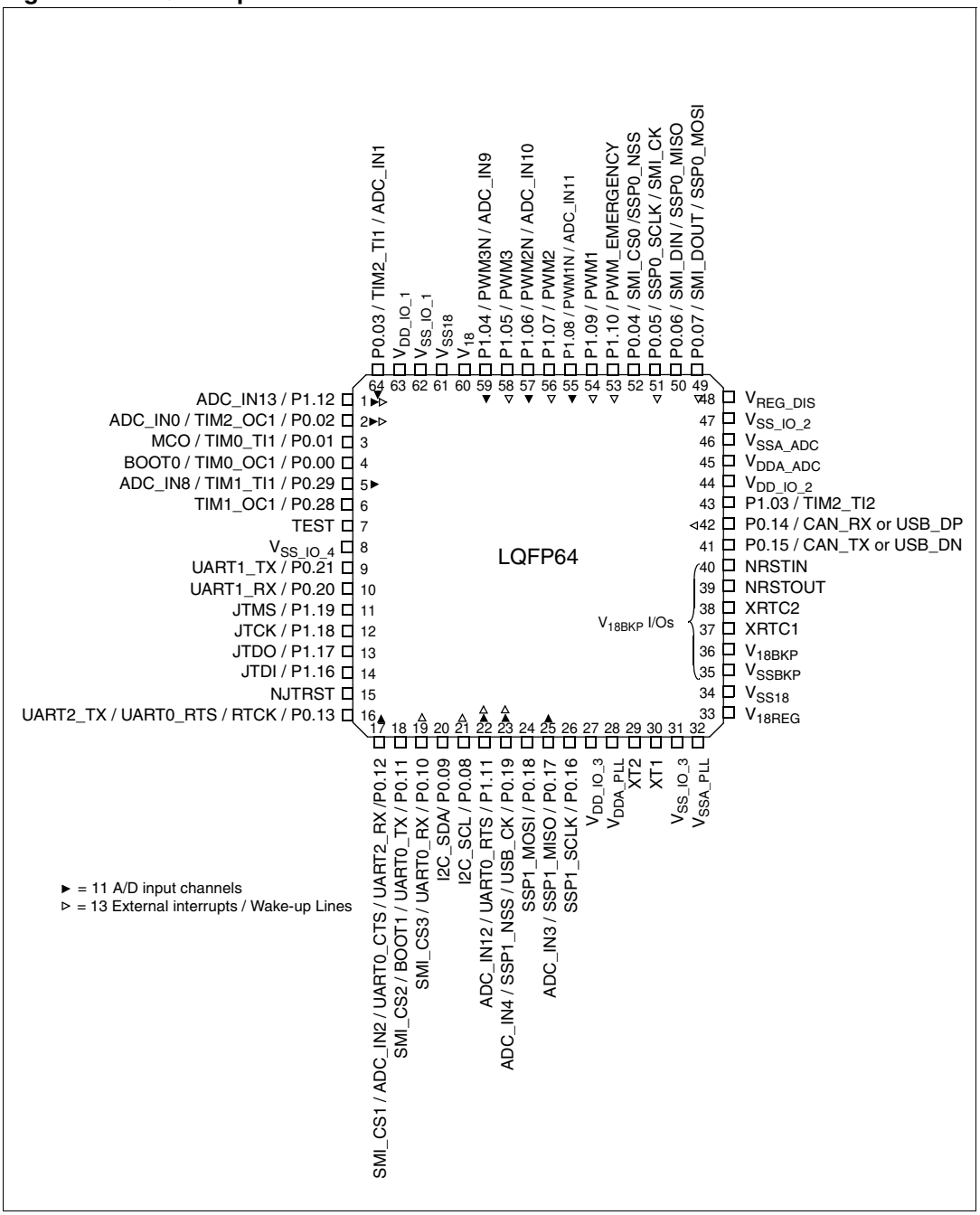


Table 4. LFBGA100 ball connections

	1	2	3	4	5	6	7	8	9	10
A	P0.03	P1.13	P1.14	P1.04	P1.06	P1.08	P0.05	P0.06	P0.07	P1.02
B	P1.12	P0.02	P0.01	P1.05	P1.07	P1.09	P0.04	P2.13	P1.03	P2.10
C	P0.31	P0.00	V_{DD_IO}	V_{18}	P1.10	P2.09	V_{SS_IO}	V_{SSA_ADC}	P2.11	USB_DP
D	P0.29	P0.30	V_{SS_IO}	V_{SS18}	P1.01	P1.15	V_{DD_IO}	V_{DDA_ADC}	P2.12	USB_DN
E	P0.28	P0.23	P0.22	V_{SS_IO}	TEST	P1.00	NRSTOUT	VREG_DIS	NRSTIN	P0.14
F	P2.03	P0.21	P0.20	P2.02	P2.04	P2.05	P2.06	V_{SS18}	V_{SSBKP}	P0.15
G	NJTRST	P1.18	P1.19	P2.01	P2.00	P2.07	2.08	V_{18REG}	V_{18BKP}	XRTC2
H	P0.13	P1.16	P1.17	P2.19	P2.18	P2.17	P0.24	P2.14	P2.16	XRTC1
J	P0.11	P0.12	P1.11	P0.27	P0.19	P0.26	P0.25	P2.15	V_{DD_IO}	V_{SS_IO}
K	P0.10	P0.09	P0.08	P0.18	P0.17	P0.16	XT1	XT2	V_{DDA_PLL}	V_{SSA_PLL}

Table 5. LFBGA64 ball connections

	1	2	3	4	5	6	7	8
A	P0.03	V_{SS_IO}	P1.04	P1.06	P1.08	P0.05	P0.06	P0.07
B	P1.12	V_{DD_IO}	P1.05	P1.07	P1.09	P0.04	P1.10	P1.03
C	P0.01	P0.02	P0.00	V_{18}	V_{SS18}	V_{DD_IO}	V_{SS_IO}	P0.14
D	P0.29	P0.28	TEST	V_{SS_IO}	VREG_DIS	V_{DDA_ADC}	V_{SSA_ADC}	P0.15
E	P1.18	P1.19	P0.20	P0.21	NRSTOUT	NRSTIN	V_{18BKP}	XRTC2
F	P0.13	NJTRST	P1.16	P1.17	V_{18REG}	V_{SS18}	V_{SSBKP}	XRTC1
G	P0.11	P0.12	P1.11	P0.19	V_{DD_IO}	V_{SS_IO}	V_{DDA_PLL}	V_{SSA_PLL}
H	P0.10	P0.09	P0.08	P0.17	P0.18	P0.16	XT2	XT1

4.1 Pin description table

Legend / abbreviations for *Table 6*:

Type: I = input, O = output, S = supply,

Input levels: All Inputs are LVTTL at V_{DD_IO} = 3.3V+/-0.3V or TTL at V_{DD_IO} = 5V± 0.5V. In both cases, T_T means V_{ILmax} =0.8V V_{IHmin}=2.0V

Inputs: All inputs can be configured as floating or with internal weak pull-up or pull down (pu/pd)

Outputs: All Outputs can be configured as Open Drain (OD) or Push-Pull (PP) (see also note 6 below *Table 6*). There are 3 different types of Output with different drives and speed characteristics:

– O8: f_{max} = 40 MHz on C_L=50pF and 8 mA static drive capability for V_{OL}=0.4V and up to 20 mA for V_{OL}=1.3V (see*Output driving current on page 55*)

– O4: f_{max} = 20 MHz on C_L=50pF and 4 mA static drive capability for V_{OL}=0.4V (see*Output driving current on page 55*)

– O2: f_{max} = 10 MHz on C_L=50pF and 2 mA static drive capability of for V_{OL}=0.4V (see*Output driving current on page 55*)

External interrupts/wake-up lines: EITx

Port reset state

The reset state of the I/O ports is GPIO input floating. Exceptions are P1[19:16] and P0.13 which are configured as JTAG alternate functions:

- The JTAG inputs (JTDI, JTMS and JTDI) are configured as input floating and are ready to accept JTAG sequences.
- The JTAG output JTDO is configured as floating when idle (no JTAG operation) and is configured in output push-pull only when serial JTAG data must be output.
- The JTAG output RTCK is always configured as output push-pull. It outputs '0' level during the reset phase and then outputs the JTCK input signal resynchronized 3 times by the internal AHB clock.
- The GPIO_PCx registers do not control JTAG AF selection, so the reset values of GPIO_PCx for P1[19:16] and P0. 13 are the same as other ports. Refer to the GPIO section of the STR750 Reference Manual for the register description and reset values.
- P0.11 and P0.00 are sampled by the boot logic after reset, prior to fetching the first word of user code at address 0000 0000h.
- When booting from SMI (and only in this case), the reset state of the following GPIOs is "SMI alternate function output enabled":
  - P0.07 (SMI_DOUT)
  - P0.05 (SMI_CLK)
  - P0.04 (SMI_CS0)
  - P0.06 (SMI_DIN)

  Note that the other SMI pins: SMI_CS1,2,3 (P0.12, P0.11, P0.10) are not affected.

To avoid excess power consumption, unused I/O ports must be tied to ground.

Table 6. STR750F pin description

Pin n°				Pin name	Type	Input				Output			Usable in Standby	Main function (after reset)	Alternate function	
LQFP100[1]	LFBGA100[1]	LQFP64[2]	LFBGA64[2]			Input Level	floating	pu/pd	Ext. int /Wake-up	Capability	OD [3]	PP				
1	B1	1	B1	P1.12 / ADC_IN13	I/O	T_T	**X**	X	EIT12	O8	X	X		**Port 1.12**	ADC: Analog input 13	
2	B2	2	C2	P0.02 / TIM2_OC1 / ADC_IN0	I/O	T_T	**X**	X	EIT0	O8	X	X		**Port 0.02**	TIM2: Output Compare 1[4]	ADC: Analog input 0
3	B3	3	C1	P0.01 / TIM0_TI1 / MCO	I/O	T_T	**X**	X		O8	X	X		**Port 0.01**	TIM0: Input Capture / trigger / external clock 1	Main Clock Output
4	C2	4	C3	P0.00 / TIM0_OC1 / BOOT0	I/O	T_T	**X**	X		O8	X	X		**Port 0.00 / Boot mode selection input 0**	TIM0: Output Compare 1	
5	C1			P0.31 / TIM1_TI2	I/O	T_T	**X**	X		O2	X	X		**Port 0.31**	TIM1: Input Capture / trigger / external clock 2	
6	D2			P0.30 / TIM1_OC2	I/O	T_T	**X**	X		O2	X	X		**Port 0.30**	TIM1: Output Compare 2	

Table 6. STR750F pin description (continued)

Pin n°				Pin name	Type	Input				Output			Usable in Standby	Main function (after reset)	Alternate function	
LQFP100(1)	LFBGA100(1)	LQFP64(2)	LFBGA64(2)			Input Level	floating	pu/pd	Ext. int /Wake-up	Capability	OD (3)	PP				
7	D1	5	D1	P0.29 / TIM1_TI1 / ADC_IN8	I/O	T_T	X	X		O2	X	X		**Port 0.29**	TIM1: Input Capture 1	ADC: Analog input 8
8	E1	6	D2	P0.28 / TIM1_OC1	I/O	T_T	X	X		O2	X	X		**Port 0.28**	TIM1: Output Compare 1	
9	E5	7	D3	TEST	I									Reserved, must be tied to ground		
10	E4	8	D4	VSS_IO	S									Ground Voltage for digital I/Os		
11	E2			P0.23 / UART1_RTS / ADC_IN6	I/O	T_T	X	X		O2	X	X		**Port 0.23**	UART1: Ready To Send output(4)	ADC analog input 6
12	F5			P2.04 / TIM2_OC1	I/O	T_T	X	X		O2	X	X		**Port 2.04**	TIM2: Output Compare 1(4)	
13	F1			P2.03 / UART1_RTS	I/O	T_T	X	X		O2	X	X		**Port 2.03**	UART1: Ready To Send output(4)	
14	F4			P2.02	I/O	T_T	X	X		O2	X	X		**Port 2.02**		
15	E3			P0.22 / UART1_CTS / ADC_IN5	I/O	T_T	X	X		O2	X	X		**Port 0.22**	UART1: Clear To Send input	ADC: Analog input 5
16	F2	9	E4	P0.21 / UART1_TX	I/O	T_T	X	X		O2	X	X		**Port 0.21**	UART1: Transmit data output (remappable to P0.15)(4)	
17	F3	10	E3	P0.20 / UART1_RX	I/O	T_T	X	X		O2	X	X		**Port 0.20**	UART1: Receive data input (remappable to P0.14)(4)	
18	G3	11	E2	P1.19 / JTMS	I/O	T_T	X	X		O2	X	X		**JTAG mode selection input(6)**	Port 1.19	
19	G2	12	E1	P1.18 / JTCK	I/O	T_T	X	X		O2	X	X		**JTAG clock input(6)**	Port 1.18	
20	H3	13	F4	P1.17 / JTDO	I/O	T_T	X	X		O8	X	X		**JTAG data output(6)**	Port 1.17	
21	H2	14	F3	P1.16 / JTDI	I/O	T_T	X	X		O2	X	X		**JTAG data input(6)**	Port 1.16	
22	G1	15	F2	NJTRST	I	T_T								JTAG reset input(5)		
23	G4			P2.01	I/O	T_T	X	X		O2	X	X		**Port 2.01**		
24	G5			P2.00	I/O	T_T	X	X		O2	X	X		**Port 0.00**		
25	H1	16	F1	P0.13 / RTCK / UART0_RTS UART2_TX	I/O	T_T	X	X		O8	X	X		**JTAG return clock output(6)**	Port 0.13 UART0: Ready To Send output(4)	UART2: Transmit Data output (when remapped)(8)

Table 6. STR750F pin description (continued)

Pin n°				Pin name	Type	Input				Output			Usable in Standby	Main function (after reset)	Alternate function	
LQFP100(1)	LFBGA100(1)	LQFP64(2)	LFBGA64(2)			Input Level	floating	pu/pd	Ext. int /Wake-up	Capability	OD (3)	PP				
26	J2	17	G2	P0.12 / UART2_RX / UART0_CTS / ADC_IN2 / SMI_CS1	I/O	T_T	X	X		O4	X	X		**Port 0.12**	UART0: Clear To Send input	ADC: Analog input 2
															Serial Memory Interface: chip select output 1	UART2: Receive Data input (when remapped)(8)
27	J1	18	G1	P0.11 / UART0_TX / BOOT1 / SMI_CS2	I/O	T_T	X	X		O4	X	X		**Port 0.11/Boot mode selection input 1**	UART0: Transmit data output	Serial Memory Interface: chip select output 2
28	K1	19	H1	P0.10 / UART0_RX / SMI_CS3	I/O	T_T	X	X	EIT4	O2	X	X		**Port 0.10**	UART0: Receive Data input	Serial Memory Interface: chip select output 3
29	K2	20	H2	P0.09 / I2C_SDA	I/O	T_T	X	X		O4	X	X		**Port 0.09**	I2C: Serial Data	
30	K3	21	H3	P0.08 / I2C_SCL	I/O	T_T	X	X	EIT3	O4	X	X		**Port 0.08**	I2C: Serial clock	
31	H4			P2.19	I/O	T_T	X	X		O2	X	X		**Port 2.19**		
32	H5			P2.18	I/O	T_T	X	X		O2	X	X		**Port 2.18**		
33	H6			P2.17 / UART2_RTS	I/O	T_T	X	X		O2	X	X		**Port 2.17**	UART2: Ready To Send output(4)	
34	J3	22	G3	P1.11 /UART0_RTS ADC_IN12	I/O	T_T	X	X	EIT11	O8	X	X		**Port 1.11**	UART0: Ready To Send output(4)	ADC: Analog input 12
35	J4			P0.27 / UART2_RTS / ADC_IN7	I/O	T_T	X	X		O2	X	X		**Port 0.27**	UART2: Ready To Send output(8)	ADC: Analog input 7
36	J6			P0.26 / UART2_CTS	I/O	T_T	X	X		O2	X	X		**Port 0.26**	UART2: Clear To Send input	
37	J7			P0.25 / UART2_TX	I/O	T_T	X	X		O2	X	X		**Port 0.25**	UART2: Transmit data output (remappable to P0.13)(8)	
38	H7			P0.24 / UART2_RX	I/O	T_T	X	X		O2	X	X		**Port 0.24**	UART2: Receive data input (remappable to P0.12)(8)	
39	J5	23	G4	P0.19 / USB_CK / SSP1_NSS / ADC_IN4	I/O	T_T	X	X	EIT6	O2	X	X		**Port 0.19**	SSP1: Slave select input (remappable to P0.11)(8)	ADC: Analog input 4
															USB: 48 MHz Clock input	
40	K4	24	H5	P0.18 / SSP1_MOSI	I/O	T_T	X	X		O2	X	X		**Port 0.18**	SSP1: Master out/slave in data (remappable to P0.10)(8)	
41	K5	25	H4	P0.17 / SSP1_MISO / ADC_IN3	I/O	T_T	X	X		O2	X	X		**Port 0.17**	SSP1: Master in/slave out data (remappable to P0.09)(8)	ADC: Analog input 3
42	K6	26	H6	P0.16 / SSP1_SCLK	I/O	T_T	X	X		O2	X	X		**Port 0.16**	SSP1: serial clock (remappable to P0.08)(8)	

Table 6. STR750F pin description (continued)

Pin n°				Pin name	Type	Input				Output			Usable in Standby	Main function (after reset)	Alternate function
LQFP100(1)	LFBGA100(1)	LQFP64(2)	LFBGA64(2)			Input Level	floating	pu/pd	Ext. int /Wake-up	Capability	OD (3)	PP			
43	H9			P2.16	I/O	T_T	**X**	X		O2	X	X		**Port 2.16**	
44	J9	27	G5	VDD_IO	S									Supply voltage for digital I/Os	
45	K9	28	G7	VDDA_PLL	S									Supply voltage for PLL	
46	K8	29	H7	XT2										4 MHz main oscillator	
47	K7	30	H8	XT1											
48	J10	31	G6	VSS_IO	S									Ground voltage for digital I/Os	
49	K10	32	G8	VSSA_PLL	S									Ground voltage for PLL	
50	J8			P2.15	I/O	T_T	**X**	X		O2	X	X		**Port 2.15**	
51	H8			P2.14	I/O	T_T	**X**	X		O2	X	X		**Port 2.14**	
52	G8	33	F5	V18REG	S									Stabilization for main voltage regulator. Requires external capacitors of at least 10µF between V18REG and VSS18. See *Figure 4.2*. To be connected to the 1.8V external power supply when embedded regulators are not used,	
53	F8	34	F6	VSS18	S									Ground Voltage for the main voltage regulator	
54	F9	35	F7	VSSBKP	S									Stabilization for low power voltage regulator.	
55	G9	36	E7	V18BKP	S									Ground Voltage for the low power voltage regulator. Requires external capacitors of at least 1µF between V18BKP and VSSBKP. See *Figure 4.2*. To be connected to the 1.8V external power supply when embedded regulators are not used,	
56	H10	37	F8	XRTC1									X	32 kHz oscillator for Realtime Clock	
57	G10	38	E8	XRTC2									X		
58	E7	39	E5	NRSTOUT	O								X	Reset output	
59	E9	40	E6	NRSTIN	I	T_T							X	Reset input	
60	D6			P1.15 / WKP_STDBY	I	T_T	**X**		EIT15				X	**Port 1.15**	Wake-up from STANDBY input pin
61	B8			P2.13	I/O	T_T	**X**	X		O2	X	X		**Port 2.13**	
62	D9			P2.12	I/O	T_T	**X**	X		O2	X	X		**Port 2.12**	
63	F10	41 (7)	D8 (7)	P0.15 / CAN_TX	I/O	T_T	**X**	X		O2	X	X		**Port 0.15**	CAN: Transmit data output
64	E10	42 (7)	C8 (7)	P0.14 / CAN_RX	I/O	T_T	**X**	X	EIT5	O2	X	X		**Port 0.14**	CAN: Receive data input
65	D10	41 (7)	D8 (7)	USB_DN	I/O									USB: bidirectional data (data -)	
66	C10	42 (7)	C8 (7)	USB_DP	I/O									USB: bidirectional data (data +)	
67	B9	43	B8	P1.03 / TIM2_TI2	I/O	T_T	**X**	X		O2	X	X		**Port 1.03**	TIM2: Input Capture / trigger / external clock 2 (remappable to P0.07)(8)

Table 6. STR750F pin description (continued)

Pin n°				Pin name	Type	Input				Output			Usable in Standby	Main function (after reset)	Alternate function	
LQFP100(1)	LFBGA100(1)	LQFP64(2)	LFBGA64(2)			Input Level	floating	pu/pd	Ext. int /Wake-up	Capability	OD (3)	PP				
68	A10			P1.02 / TIM2_OC2	I/O	T_T	X	X		O2	X	X		**Port 1.02**	TIM2: Output compare 2 (remappable to P0.06)(8)	
69	D7	44	C6	VDD_IO	S									Supply Voltage for digital I/Os		
70	D8	45	D6	VDDA_ADC	S									Supply Voltage for A/D converter		
71	C9			P2.11	I/O	T_T	X	X		O2	X	X		**Port 2.11**		
72	B10			P2.10	I/O	T_T	X	X		O2	X	X		**Port 2.10**		
73	C8	46	D7	VSSA_ADC	S									Ground Voltage for A/D converter		
74	C7	47	C7	VSS_IO	S									Ground Voltage for digital I/Os		
75	E8	48	D5	VREG_DIS	I	T_T								Voltage Regulator Disable input		
76	A9	49	A8	P0.07 / SMI_DOUT / SSP0_MOSI	I/O	T_T	X	X	EIT2	O4	X	X		**Port 0.07**	Serial Memory Interface: data output	SSP0: Master out Slave in data
77	A8	50	A7	P0.06 / SMI_DIN / SSP0_MISO	I/O	T_T	X	X		O4	X	X		**Port 0.06**	Serial Memory Interface: data input	SSP0: Master in Slave out data
78	A7	51	A6	P0.05 / SSP0_SCLK / SMI_CK	I/O	T_T	X	X	EIT1	O4	X	X		**Port 0.05**	SSP0: Serial clock	Serial Memory Interface: Serial clock output
79	B7	52	B6	P0.04 / SMI_CS0 / SSP0_NSS	I/O	T_T	X	X		O4	X	X		**Port 0.04**	Serial Memory Interface: chip select output 0	SSP0: Slave select input
80	C5	53	B7	P1.10 PWM_EMERGENCY	I/O	T_T	X	X	EIT10	O2	X	X		**Port 1.10**	PWM: Emergency input	
81	B6	54	B5	P1.09 / PWM1	I/O	T_T	X	X	EIT9	O4	X	X		**Port 1.09**	PWM: PWM1 output	
82	C6			P2.09 / PWM1N	I/O	T_T	X	X		O2	X	X		**Port 2.09**	PWM: PWM1 complementary output(4)	
83	G7			P2.08 / PWM2	I/O	T_T	X	X		O2	X	X		**Port 2.08**	PWM: PWM2 output(4)	
84	G6			P2.07 / PWM2N	I/O	T_T	X	X		O2	X	X		**Port 2.07**	PWM: PWM2 complementary output(4)	
85	F7			P2.06 / PWM3	I/O	T_T	X	X		O2	X	X		**Port 2.06**	PWM: PWM3 output(4)	
86	F6			P2.05 / PWM3N	I/O	T_T	X	X		O2	X	X		**Port 2.05**	PWM: PWM3 complementary output(4)	
87	A6	55	A5	P1.08 / PWM1N / ADC_IN11	I/O	T_T	X	X		O4	X	X		**Port 1.08**	PWM: PWM1 complementary output(8)	ADC: analog input 11
88	B5	56	B4	P1.07 / PWM2	I/O	T_T	X	X	EIT8	O4	X	X		**Port 1.07**	PWM: PWM2 output(4)	
89	A5	57	A4	P1.06 / PWM2N / ADC_IN10	I/O	T_T	X	X		O4	X	X		**Port 1.06**	PWM: PWM2 complementary output(4)	ADC: analog input 10
90	B4	58	B3	P1.05 / PWM3	I/O	T_T	X	X	EIT7	O4	X	X		**Port 1.05**	PWM: PWM3 output(4)	

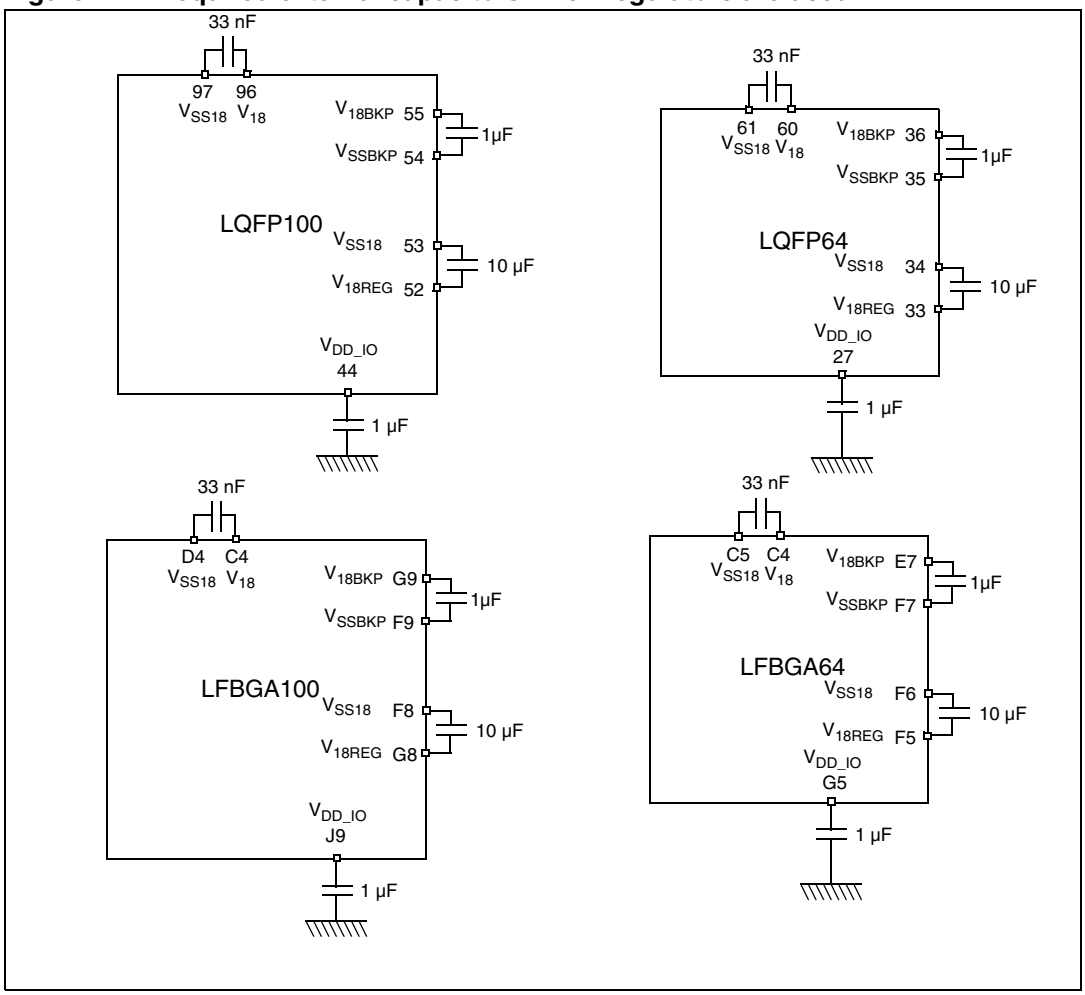
Table 6. STR750F pin description (continued)

Pin n°				Pin name	Type	Input				Output			Usable in Standby	Main function (after reset)	Alternate function	
LQFP100(1)	LFBGA100(1)	LQFP64(2)	LFBGA64(2)			Input Level	floating	pu/pd	Ext. int /Wake-up	Capability	OD (3)	PP				
91	A4	59	A3	P1.04 / PWM3N / ADC_IN9	I/O	T_T	**X**	X		O4	X	X		**Port 1.04**	PWM: PWM3 complementary output(4)	ADC: analog input 9
92	A3			P1.14 / ADC_IN15	I/O	T_T	**X**	X		O8	X	X		**Port 1.14**	ADC: analog input 15	
93	A2			P1.13 / ADC_IN14	I/O	T_T	**X**	X	EIT13	O8	X	X		**Port 1.13**	ADC: analog input 14	
94	D5			P1.01 / TIM0_TI2	I/O	T_T	**X**	X		O2	X	X		**Port 1.01**	TIM0: Input Capture / trigger / external clock 2 (remappable to P0.05)(8)	
95	E6			P1.00 / TIM0_OC2	I/O	T_T	**X**	X		O2	X	X		**Port 1.00**	TIM0: Output compare 2 (remappable to P0.04)(8)	
96	C4	60	C4	V18	S									Stabilization for main voltage regulator. Requires external capacitors 33nF between V18 and VSS18. See *Figure 4.2*. To be connected to the 1.8V external power supply when embedded regulators are not used.		
97	D4	61	C5	VSS18	S									Ground Voltage for the main voltage regulator.		
98	D3	62	A2	VSS_IO	S									Ground Voltage for digital I/Os		
99	C3	63	B2	VDD_IO	S									Supply Voltage for digital I/Os		
100	A1	64	A1	P0.03 / TIM2_TI1 / ADC_IN1	I/O	T_T	**X**	X		O2	X	X		**Port 0.03**	TIM2: Input Capture / trigger / external clock 1	ADC: analog input 1

1. For STR755FVx part numbers, the USB pins must be left unconnected.
2. The non available pins on LQPFP64 and LFBGA64 packages are internally tied to low level.
3. None of the I/Os are True Open Drain: when configured as Open Drain, there is always a protection diode between the I/O pin and VDD_IO.
4. In the 100-pin package, this Alternate Function is duplicated on two ports. You can configure one port to use this AF, the other port is then free for general purpose I/O (GPIO), external interrupt/wake-up lines, or analog input (ADC_IN) where these functions are listed in the table.
5. It is mandatory that the NJTRST pin is reset to ground during the power-up phase. It is recommended to connect this pin to NRSTOUT pin (if available) or NRSTIN.
6. After reset, these pins are enabled as JTAG alternate function see (*Port reset state on page 16*). To use these ports as general purpose I/O (GPIO), the DBGOFF control bit in the GPIO_REMAP0R register must be set by software (in this case, debugging these I/Os via JTAG is not possible).
7. There are two different TQFP and BGA 64-pin packages: in the first one, pins 41 and 42 are mapped to USB DN/DP while for the second one, they are mapped to P0.15/CAN_TX and P0.14/CAN_RX.
8. For details on remapping these alternate functions, refer to the GPIO_REMAP0R register description.

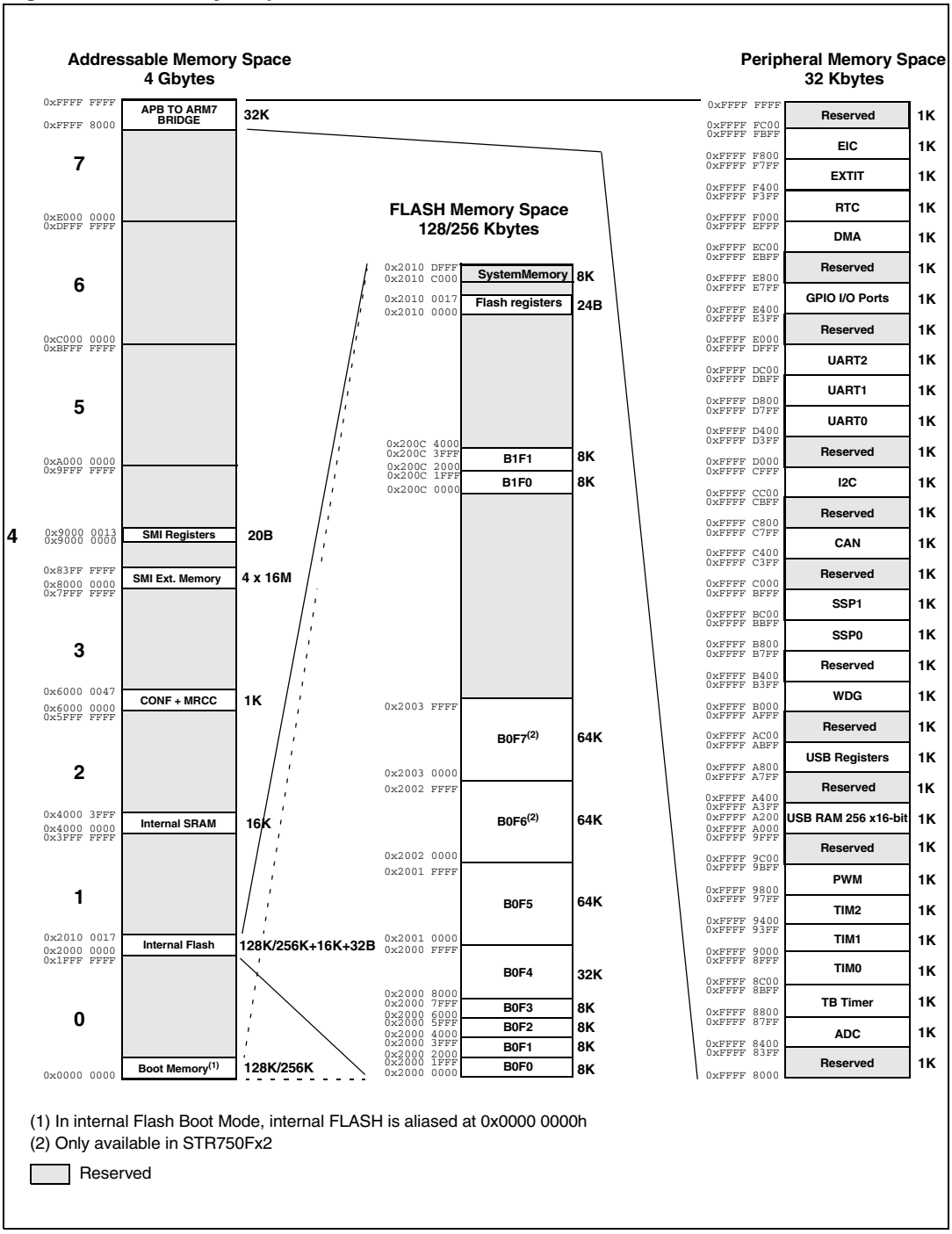
4.2 External components

Figure 4. Required external capacitors when regulators are used



5 Memory map

Figure 5. Memory map



(1) In internal Flash Boot Mode, internal FLASH is aliased at 0x0000 0000h
(2) Only available in STR750Fx2

Reserved

6 Electrical parameters

6.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at $T_A$max (given by the selected temperature range).

Data based on product characterisation, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3Σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A=25° C, V_{DD_IO}=3.3 V (for the 3.0 V≤V_{DD_IO}≤3.6 V voltage range) and V_{18}=1.8 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2Σ).

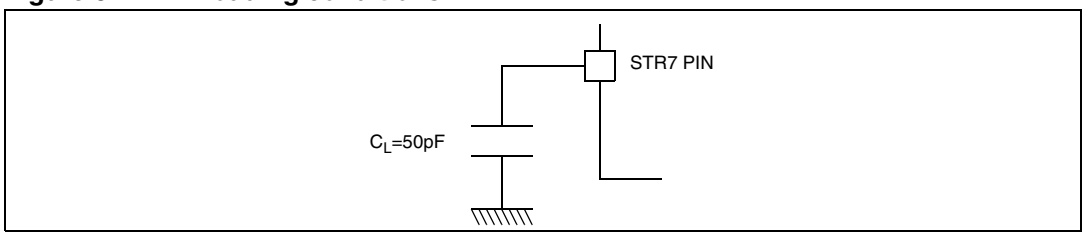
6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 6*.

Figure 6. Pin loading conditions



6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 7*.

Figure 7. Pin input voltage