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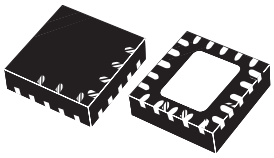
STS1TX

Low data-rate, low power sub-1GHz transmitter

Datasheet - production data



QFN20

Features

- Frequency bands: 150-174 MHz, 300-348 MHz, 387-470 MHz, 779-956 MHz
- Modulation schemes: 2-FSK, GFSK, MSK, GMSK, OOK, and ASK
- Air data rate from 1 to 500 kbps
- Very low power consumption (21 mA TX at +11 dBm)
- Programmable channel spacing (12.5 kHz min.)
- Programmable output power up to +16 dBm
- Fast startup and frequency synthesizer settling time (6 µs)
- Integrated temperature sensor
- Battery indicator and low battery detector
- TX FIFO buffer (96 bytes each)
- Configurability via SPI interface
- AES 128-bit encryption co-processor
- Fully integrated ultra low power RC oscillator
- Wakeup on internal timer and on external event
- Flexible packet length with dynamic payload length
- Automatic CRC handling
- FEC with interleaving
- Whitening of data
- Wireless M-BUS, EN 300 220, FCC CFR47 15 (15.205, 15.209, 15.231, 15.247, 15.249), and ARIB STD T-67, T93, T-108 compliant
- QFN20 4x4 mm RoHS package
- Operating temperature range from -40 °C to 85 °C

Applications

- AMR (automatic meter reading)
- Home and building automation
- WSN (wireless sensors network)
- Industrial monitoring and control
- Wireless fire and security alarm systems
- Point-to-point wireless link

Table 1. Device summary

Order code	Package	Packing
STS1TXQTR	QFN20	Tape and reel

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1 Description

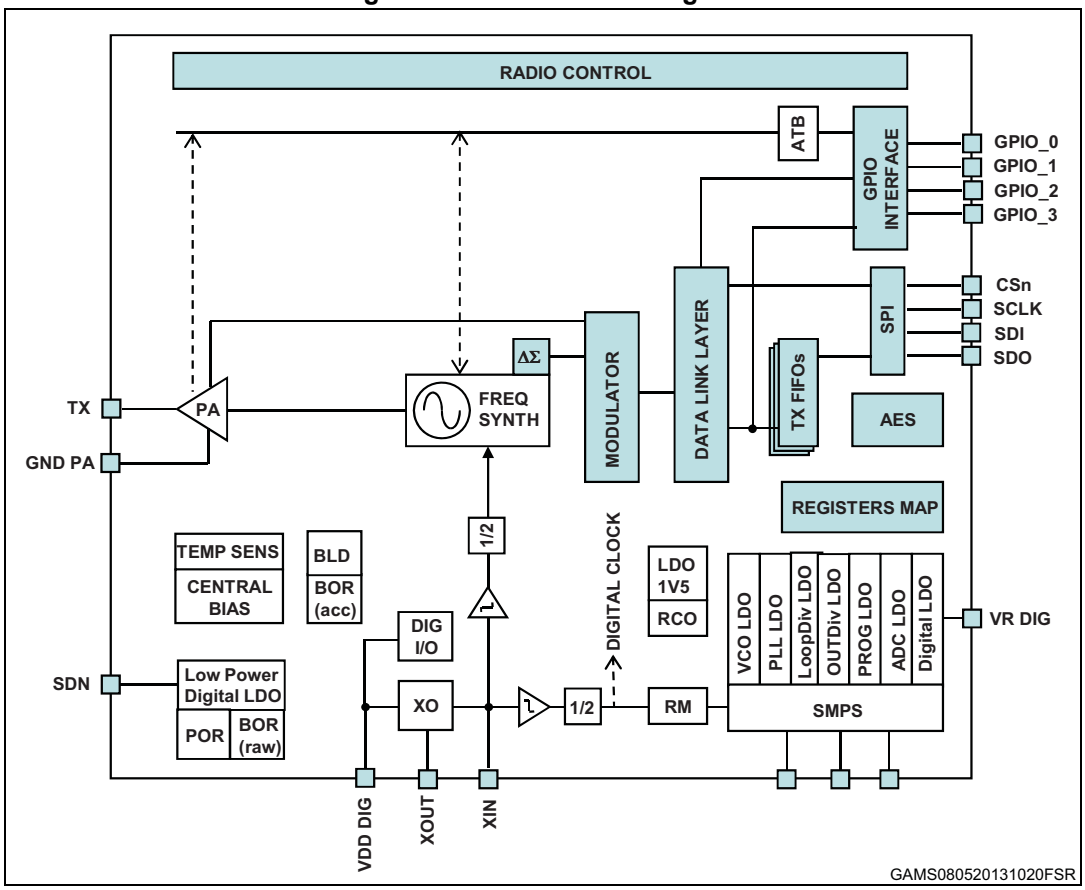
The STS1TX is a very low-power RF transmitter intended for RF wireless applications in the sub-1 GHz band. It is designed to operate both in the license-free ISM and SRD frequency bands at 169, 315, 433, 868, and 915 MHz, but can also be programmed to operate at other frequencies in the 300-348, 387-470, and 779-956 MHz bands. The air data rate is programmable from 1 to 500 kbps, and the STS1TX can be used in systems with channel spacing of 12.5/25 kHz, complying with the EN 300 220 standard. It uses very few discrete external components and integrates a configurable baseband modem, which supports data management and modulation. The data management handles the data in the proprietary fully-programmable packet format, and also allows the M-Bus standard compliance format (all performance classes).

An AES 128-bit encryption co-processor is available for secure data transfer. The STS1TX supports different modulation schemes: 2-FSK, GFSK, OOK, ASK, and MSK. Transmitted data bytes are buffered in FIFO (TX FIFO), accessible via the SPI interface for host processing.

2 Introduction

A simplified block diagram of the STS1TX is shown in *Figure 1*.

Figure 1. STS1TX block diagram



The transmitter part of the STS1TX is based on direct synthesis of the RF frequency. The power amplifier (PA) input is the LO generated by the RF synthesizer, while the output level can be configured between -30 dBm and +11 dBm in 0.5 dB steps. The data to be transmitted can be provided by an external MCU either through the 96-byte TX FIFO writable via SPI, or directly using a programmable GPIO pin. The STS1TX supports frequency hopping, extending the link range and improving performance.

The STS1TX has a very efficient power management (PM) system.

An integrated switched mode power supply (SMPS) regulator allows operation from a battery voltage ranging from +1.8 V to +3.6 V, and with power conversion efficiency of at least 80%.

A crystal must be connected between XIN and XOUT. It is digitally configurable to operate with different crystals. As an alternative, an external clock signal can be used to feed XIN for proper operation. The STS1TX also has an integrated low-power RC oscillator, generating the 34.7 kHz signal used as a clock for the slowest timeouts (i.e. sleeping and backoff).

A standard 4-pin SPI bus is used to communicate with the external MCU. Four configurable general purpose I/Os are available.

3 Typical application diagram and pin description

3.1 Typical application diagram

This section describes different application diagrams for the STS1TX that can be used based on customer requirements. In particular, *Figure 2* shows the default configuration and *Figure 3* shows the TX boost mode configuration. The default configuration provides the best power consumption figures. The TX boost mode configuration is used to increase TX output power.

Figure 2. Suggested application diagram

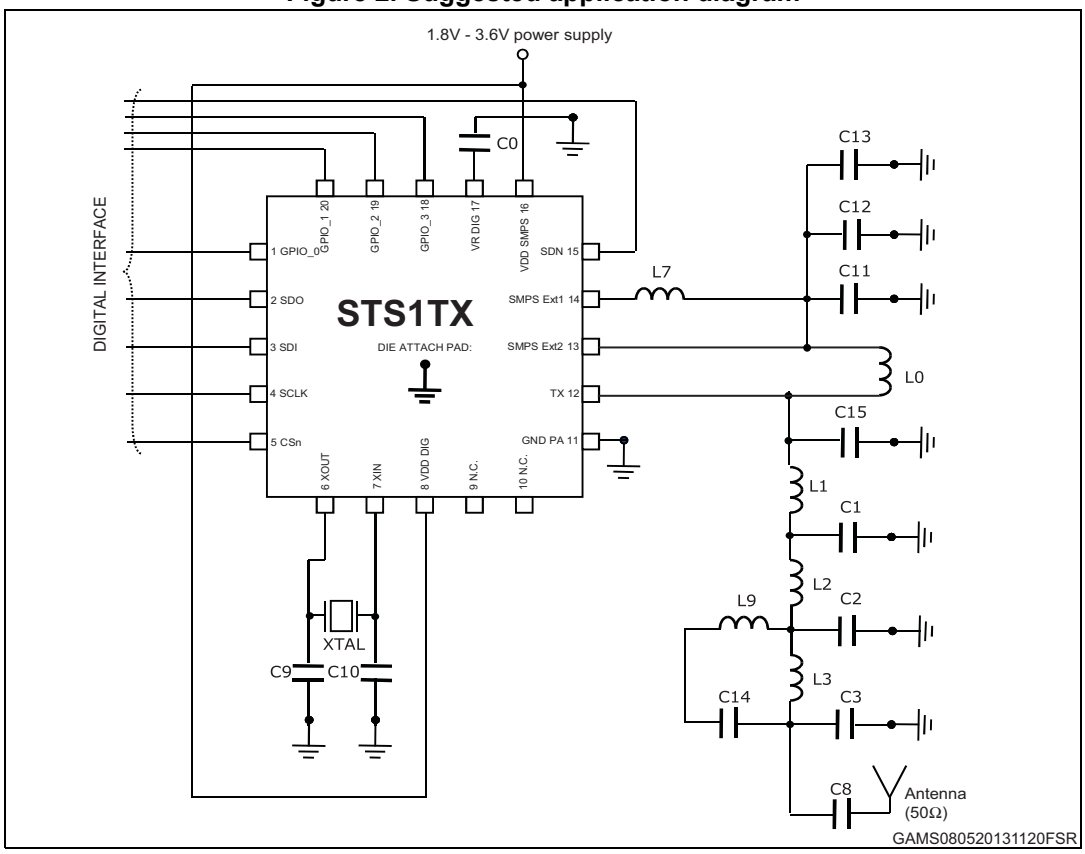


Figure 3. Application diagram for TX boost mode

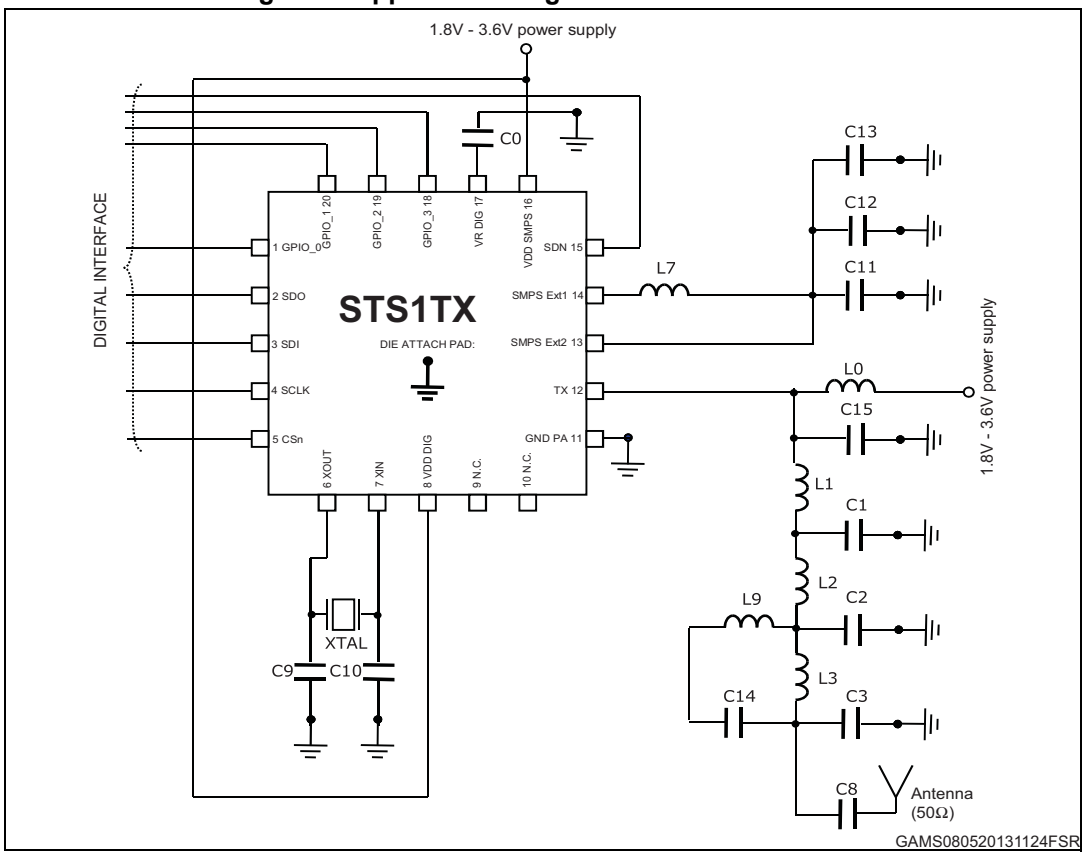


Table 2. Description of the external components of the typical application diagram

Components	Description
C0	Decoupling capacitor for on-chip voltage regulator to digital part
C1, C2, C3, C14, C15	RF LC filter/matching capacitors
C8	Matching DC blocking capacitors
C9, C10	Crystal loading capacitors
C11, C12, C13	SMPS LC filter capacitor
L0	RF choke inductor
L1, L2, L3, L9	RF LC filter/matching inductors
XTAL	24, 26, 48, 52 MHz

Table 2 covers all the frequency bands using a set of different external components as shown in *Table 3: BOM for different bands*.

Table 3. BOM for different bands

Ref design (1)	170 MHz band		315 MHz band		433 MHz band		868 MHz band		915/922 MHz band	
	STEVAL-IKRV001V1		STEVAL-IKRV001V2		STEVAL-IKRV001V3		STEVAL-IKRV001V4		STEVAL-IKRV001V5	
Comp.	Supplier	Value	Supplier	Value	Supplier	Value	Supplier	Value	Supplier	Value
C0	Murata	100nF	Murata	100nF	Murata	100nF	Murata	100nF	Murata	100nF
C1	Murata	18pF	Murata	12pF	Murata	8.2pF		NE	Murata	7pF
C2	Murata	27pF	Murata	27pF	Murata	18pF	Murata	8.2pF	Murata	2.4pF
C3	Murata	4.3pF	Murata	15pF	Murata	10pF	Murata	5.6pF	Murata	3.6pF
C8	Murata	390pF	Murata	220pF	Murata	220pF	Murata	220pF	Murata	220pF
C9	Murata	12pF	Murata	12pF	Murata	12pF	Murata	12pF	Murata	12pF
C10	Murata	10pF	Murata	10pF	Murata	10pF	Murata	10pF	Murata	10pF
C11	Murata	1µF	Murata	1µF	Murata	1µF	Murata	470nF	Murata	1µF
C12	Murata	100nF	Murata	100nF	Murata	100nF	Murata	100nF	Murata	100nF
C13	Murata	560pF	Murata	330pF	Murata	330pF	Murata	330pF	Murata	330pF
C14	Murata	220pF	Murata	1.8pF	Murata	1.8pF	Murata	1.2pF		NE
C15	Murata	6.2pF	Murata	1.2pF		NE		NE		NE
L0	Murata	200nH	Murata	220nH	Murata	150nH	Murata	100nH	Murata	100nH
L1	Coilcraft	39nH	Murata	12nH	Murata	8.2nH	Murata	3nH	Murata	3.6nH
L2	Coilcraft	56nH	Murata	12nH	Murata	10nH		0R0 (resistor)	Murata	5.1nH
L3	Murata	3.6pF (cap.)	Murata	15nH	Murata	10nH	Murata	4.3nH	Tyco Electronics	0R0
L9	Coilcraft	51nH	Murata	15nH	Murata	6.2nH	Murata	2.7nH		NE
XTAL	NDK	25 MHz	NDK	50 MHz	NDK	50 or 52 MHz	NDK	50 or 52 MHz	NDK	50 or 52 MHz

1. For complete BOM including part numbers, please check the corresponding reference design.

4 Pinout

Table 4. Pinout description

Pin	Name	I/O	Description
1	GPIO_0	I/O	See description of GPIOs below
2	MISO	O	SPI data output pin
3	MOSI	I	SPI data input pin
4	SCLK	I	SPI clock input pin
5	CSn	I	SPI chip select
6	XOUT	O	Crystal oscillator output. Connect to an external 26 MHz crystal or leave floating if driving the XIN pin with an external signal source
7	XIN	I	Crystal oscillator input. Connect to an external 26 MHz crystal or to an external source. If using an external clock source with no crystal, DC coupling with a nominal 0.2 VDC level is recommended with minimum AC amplitude of 400 mVpp. The instantaneous level at input cannot exceed the 0 - 1.4 V range.
8	VBAT	VDD	+1.8 V to +3.6 V input supply voltage
9	NC	-	
10	NC	-	
11	GND_PA	GND	Ground for PA. To be carefully decoupled from other grounds.
12	TX	O	RF output signal
13	SMPS Ext2	I	Regulated DC-DC voltage input
14	SMPS Ext1	O	DC-DC output pin
15	SDN	I	Shutdown input pin. 0-VDD V digital input. SDN should be = ‘0’ in all modes except shutdown mode. When SDN =’1’ the STS1TX is completely shut down and the contents of the registers are lost.
16	VBAT	VDD	+1.8 V to +3.6 V input supply voltage
17	VREG(1)	VDD	Regulated output voltage. A 100 nF decoupling capacitor is required
18	GPIO3	I/O	General purpose I/O that may be configured through the SPI registers to perform various functions, including: – MCU clock output – FIFO status flags – Wakeup input – Battery level detector – Temperature sensor output
19	GPIO2	I/O	
20	GPIO1	I/O	
21	GND	GND	Exposed pad ground pin

1. This pin is intended for use with the STS1TX only. It cannot be used to provide supply voltage to other devices.

5 Absolute maximum ratings and thermal data

Absolute maximum ratings are those values above which damage to the device may occur. Functional operation under these conditions is not implied. All voltages are referred to GND.

Table 5. Absolute maximum ratings

Pin	Parameter	Value	Unit
8,14,16	Supply voltage and SMPS output	-0.3 to +3.9	V
17	DC voltage on VREG	-0.3 to +1.4	V
1,3,4,5,15,18,19,20	DC voltage on digital input pins	-0.3 to +3.9	V
2	DC voltage on digital output pins	-0.3 to +3.9	V
11	DC voltage on analog pins	-0.3 to +3.9	V
6,7	DC voltage on XTAL pins	-0.3 to +1.4	V
13	DC voltage on SMPS Ext2 pin	-0.3 to +1.8	V
12	DC voltage on TX pin	-0.3 to +3.9	V
T_{STG}	Storage temperature range	-40 to +125	°C
$V_{ESD-HBM}$	Electrostatic discharge voltage	±1.0	KV

Table 6. Thermal data

Symbol	Parameter	QFN20	Unit
$R_{thj-amb}$	Thermal resistance junction-ambient	45	°C/W

Table 7. Recommended operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{BAT}	Operating battery supply voltage	1.8	3	3.6	V
T_A	Operating ambient temperature range	-40		85	°C

6 Characteristics

6.1 General characteristics

Table 8. General characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
FREQ	Frequency range	150	-	174	MHz
		300		348	MHz
		387		470	MHz
		779		956	MHz
DR	Air data rate for each modulation scheme. Note that if “Manchester”, “3-out-of-6” and/or FEC encoding/decoding options are selected, the effective bit rate will be lower.				
	2-FSK	1	-	500	kBaud
	GMSK (BT=1, BT=0.5)	1		500	kBaud
	GFSK (BT=1, BT=0.5)	1		500	kBaud
	MSK	1		500	kBaud
	OOK/ASK	1		250	kBaud

6.2 Electrical specifications

6.2.1 Electrical characteristics

Characteristics measured over recommended operating conditions unless otherwise specified. Typical values are referred to T_A = 25 °C, V_{BAT} = 3.0 V. All performance is referred to a 50 Ohm antenna connector, via the reference design using the application diagram as in *Figure 2*, unless otherwise noted.

Table 9. Power consumption static modes

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
IBAT	Supply current	Shutdown (1)	-	2.5	-	nA
		Standby (1)		600		
		Sleep (1)		850		
		Ready (default mode)(1)		400		µA
		Lock(1)		4.4		mA

1. See *Table 18*.

Table 10. Power consumption

Symbol	Parameter	Test conditions	SMPS ON	SMPS OFF	Unit
IBAT	Supply current	TX (1)(2) +16 dBm 169 MHz	54		mA
		TX (1)(2) +16 dBm 315 MHz	52		
		TX (1)(2) +16 dBm 433 MHz	49.3		
		TX (1)(2) +15.5 dBm 868 MHz	44		
		TX (1)(2) +16 dBm 920 MHz	45.2		
		TX (1) +11 dBm 169 MHz	18	33	
		TX (1) +11 dBm 315 MHz	22	37	
		TX (1) +11 dBm 433 MHz	19.5	33	
		TX (1) +11 dBm 868 MHz	21	41	
		TX (1) +11 dBm 920 MHz	20	39	
		TX (1) -8 dBm 169 MHz	6		
		TX (1) -8 dBm 315 MHz	6.5		
		TX (1) -7 dBm 433 MHz	7		
		TX (1) -7 dBm 868 MHz	7		

1. See table *Table 18*.
2. TX boost mode configuration V_{BAT} = 3.6 V.

6.2.2 Digital SPI

Table 11. Digital SPI input and output (SDO, SDI, SCLK, CSn, and SDN) and GPIO specification (GPIO_1-4)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
f_{clk}	Clock frequency				10	MHz
C_{IN}	Port I/O capacitance			1.4		pF
T_{RISE}	Rise time	0.1*VDD to 0.9*VDD, CL=20 pF (low output current programming)		6.0		ns
		0.1*VDD to 0.9*VDD, CL=20 pF (high output current programming)		2.5		
T_{FALL}	Fall time	0.1*VDD to 0.9*VDD, CL=20 pF (low output current programming)		7.0		ns
		0.1*VDD to 0.9*VDD, CL=20 pF (high output current programming)		2.5		
V_{IH}	Logic high level input voltage		VDD/2 +0.3			V

Table 11. Digital SPI input and output (SDO, SDI, SCLK, CSn, and SDN) and GPIO specification (GPIO_1-4) (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{IL}	Logic low level input voltage				VDD/8 +0.3	V
V_{OH}	High level output voltage	IOH = -2.4 mA (-4.2 mA if high output current capability is programmed).	(5/8)* VDD+ 0.1			V
V_{OL}	Low level output voltage	IOL = +2.4 mA (+4 mA if high output current capability is programmed).			0.5	V

6.2.3 RF transmitter

Characteristics measured over recommended operating conditions unless otherwise specified. All typical values are referred to T_A = 25 °C, V_{BAT} = 3.0 V. All performance is referred to a 50 Ohm antenna connector, via the reference design.

Table 12. RF transmitter characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$P_{MAX\_TX\_BOOST}$	Maximum output power(1)	Delivered to a 50 Ohm single-ended load via reference design using TX boost mode configuration	-	16		dBm
P_{MAX}	Maximum output power(1)	Delivered to a 50 Ohm single-ended load via reference design	-	11		dBm
P_{MIN}	Minimum output power	Delivered to a 50 Ohm single-ended load via reference design	-	-30		dBm
P_{STEP}	Output power step		-	0.5		dB

Table 12. RF transmitter characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$P_{SPUR,ETSI}$	Unwanted emissions according to ETSI EN300 220-1(harmonic included, using reference design)	RF = 170 MHz, frequencies below 1 GHz	-		-36	dBm
		RF = 170 MHz, Frequencies above 1 GHz	-		< -60	dBm
		RF = 170 MHz, frequencies within 47-74, 87.5-108,174-230,470-862 MHz	-		-55	dBm
		RF = 434 MHz, frequencies below 1 GHz	-		-42	dBm
		RF = 434 MHz, Frequencies above 1 GHz	-		-46	dBm
		RF = 434 MHz, frequencies within 47-74, 87.5-108,174-230,470-862 MHz	-		-61	dBm
		RF = 868 MHz, frequencies below 1 GHz	-		-51	dBm
		RF = 868 MHz, Frequencies above 1 GHz	-		-40	dBm
		RF = 868 MHz, frequencies within 47-74, 87.5-108,174-230,470-862 MHz	-		-54	dBm

Table 12. RF transmitter characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$P_{SPUR,FCC}$	Unwanted emissions according to FCC part 15(harmonic included, using reference design)	RF = 310-320 MHz, harmonics (measured with max output power)	-		-37	dBm
		RF = 310-320 MHz, 1.705 MHz <f< 30 MHz	-		<-60	dBm
		RF = 310-320 MHz, 30 MHz <f< 88 MHz	-		<-60	dBm
		RF = 310-320 MHz, 88 MHz <f< 216 MHz	-		<-60	dBm
		RF = 310-320 MHz, 216 MHz <f< 960 MHz	-		<-60	dBm
		RF = 310-320 MHz, 960 MHz <f	-		<-60	dBm
		RF = 902-928 MHz, 1.705 MHz <f< 30 MHz (@ max output power)	-		<-70	dBm
		RF = 902-928 MHz, 30 MHz <f< 88 MHz (@ max output power)	-		<-70	dBm
		RF = 902-928 MHz, 88 MHz <f< 216 MHz (@ max output power)	-		<-70	dBm
		RF = 902-928 MHz, 216 MHz <f< 960 MHz (@ max output power)	-		-52	dBm
		RF = 902-928 MHz, 960 MHz <f (@ max output power)	-		-41	dBm
		2^{nd} and 7^{th} harmonics	-		-25	dBc

Table 12. RF transmitter characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$P_{SPUR,ARIB}$	Unwanted emissions according to ARIB	RF = 312-315 MHz, frequency below 1 GHz (@ max output power, according to ARIB STD-T93)	-		-41	dBm
		RF = 312-315 MHz, frequency above 1 GHz (@ max output power, according to ARIB STD-T93)	-		-48	dBm
		RF = 426-470 MHz (@ max output power, according to ARIB STD-T67)	-		<-40	dBm
		RF = 915-917 MHz and RF = 920-930 MHz, f< 710 MHz (@ max output power, according to ARIB STD-T108)	-		<-55	dBm
		RF = 915-917 MHz and RF = 920-930 MHz, 710 MHz <f< 915 MHz (@ max output power, according to ARIB STD-T108)	-		-55	dBm
		RF = 915-917 MHz and RF = 924-930 MHz, 915 MHz <f< 930 MHz (@ max output power, according to ARIB STD-T108)	-		-36	dBm
		RF = 920-924 MHz, 915 MHz <f< 920.3 MHz (@ max output power, according to ARIB STD-T108)	-		<-36	dBm
		RF = 920-924 MHz, 920.3 MHz <f< 924.3 MHz (@ max output power, according to ARIB STD-T108)	-		-55	dBm
		RF = 920-924 MHz, 924.3 MHz <f< 930 MHz (@ max output power, according to ARIB STD-T108)	-		-36	dBm
		RF = 915-917 MHz and RF = 920-930 MHz, 930 MHz <f< 1000 MHz (@ max output power, according to ARIB STD-T108)	-		-55	dBm
		RF = 915-917 MHz and RF = 920-930 MHz, 1000 MHz <f< 1215 MHz (@ max output power, according to ARIB STD-T108)	-		<-60	dBm
		RF = 915-917 MHz and RF = 920-930 MHz, 1215 MHz <f (@ max output power, according to ARIB STD-T108)	-		-38	dBm

Table 12. RF transmitter characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
P_{HARM}	Harmonics level	RF = 170 MHz, 2nd harmonic (max power level)	-		-36	dBm
		RF = 170 MHz, 3rd harmonic (max power level)	-		-55	
		RF = 315 MHz, 2nd harmonic (max power level)	-		-52	dBc
		RF = 315 MHz, 3rd harmonic (max power level)	-		-52	
		RF = 433 MHz, 2nd harmonic (max power level)	-		-43	dBm
		RF = 433 MHz, 3rd harmonic (max power level)	-		-46	
		RF = 868 MHz, 2nd harmonic (max power level)	-		-40	
		RF = 868 MHz, 3rd harmonic (max power level)	-		-42	
		RF = 915 MHz, 2nd harmonic (max power level)	-		-28	dBc
		RF = 915 MHz, 3rd harmonic (max power level)	-		-42	dBm
		RF = 922 MHz, 2nd harmonic (max power level)	-		-39	
		RF = 922 MHz, 3rd harmonic (max power level)	-		-60	
PA_{LOAD}	Optimum load impedance (simulated values)	170 MHz, using reference design	-	46 + j36		Ohm
		315 MHz, using reference design	-	25 + j27		Ohm
		433 MHz, using reference design	-	29 + j19		Ohm
		868 MHz, using reference design	-	34 - j7		Ohm
		915 MHz, using reference design	-	15 + j28		Ohm
		922 MHz, using reference design	-	42 - j15		Ohm

1. In ASK/OOK modulation, indicated value represents peak power.

6.2.4 Crystal oscillator

Characteristics measured over recommended operating conditions unless otherwise specified. All typical values are referred to T_A = 25 °C, V_{BAT} = 3.0 V. Frequency synthesizer characteristics are referred to 915 MHz band.

Table 13. Crystal oscillator characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$XTAL_F$	Crystal frequency	Range 1 Range 2	24 48		26 52	MHz
F_{TOL}	Frequency tolerance(1)			± 40		ppm
PN_{XTAL}	Minimum requirement on external reference phase noise mask (Fxo=26 MHz), to avoid degradation on synthesizer phase/noise	100 Hz			-90	dBc/Hz
		1 kHz			-120	dBc/Hz
		10 kHz			-135	dBc/Hz
		100 kHz			-140	dBc/Hz
		1 MHz			-140	dBc/Hz
T_{START}	Startup time(2)	V_{BAT}=1.8 V, Fxo= 52 MHz	60	120	220	µs

1. Including initial tolerance, crystal loading, aging, and temperature dependence. The acceptable crystal tolerance depends on RF frequency and channel spacing/bandwidth.
2. Startup times are crystal dependent. The crystal oscillator transconductance can be tuned to compensate the variation of crystal oscillator series resistance.

Table 14. Ultra low power RC oscillator

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
RC_F	Calibrated frequency	Calibrated RC oscillator frequency is derived from crystal oscillator frequency. Digital clock domain 26 MHz	-	34.7		kHz
RC_{TOL}	Frequency accuracy after calibration				±1	%

Table 15. N-Fractional ΣΔ frequency synthesizer characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
F_{RES}	Frequency resolution	Fxo = 26 MHz high band	-	33		Hz
PN_{SYNTH}	RF carrier phase noise (915 MHz band)	10 kHz	-100	-97	-94	dBc/Hz
		100 kHz	-104	-101	-99	dBc/Hz
		200 kHz	-105	-102	-100	dBc/Hz
		500 kHz	-112	-110	-107	dBc/Hz
		1 MHz	-120	-118	-116	dBc/Hz
		2 MHz	-123	-121	-119	dBc/Hz
TO_{TIME}	PLL turn-on/hop time			60	80	µs
CAL_{TIME}	PLL calibration time			54		µs

6.2.5 Sensors

Characteristics measured over recommended operating conditions unless otherwise specified. All typical values are referred to T_A = 25 °C, V_{BAT} = 3.0 V.

Table 16. Analog temperature sensor characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
T_{ERR}	Error in temperature	Across the temperature range	-	±2.5	-	°C
T_{SLOPE}	Temperature coefficient			2.5		mV/ °C
V_{TS-OUT}	Output voltage level			0.92		V
T_{ICC}	Current consumption	Buffered output (low output impedance; about 400 Ohm)		600		µA
		Not buffered output (high output impedance; about 100 kΩ)		10		µA

Table 17. Battery indicator and low battery detector(1)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{BLT}	Battery level thresholds		2.1		2.7	V
V_{BOT}	Brownout threshold	Measured in slow battery variation (static) conditions (inaccurate)		1.535		V
		Measured in slow battery variation (static) conditions (accurate)		1.684		V
BOT_{hyst}	Brownout threshold hysteresis			70		mV

1. For battery powered equipment, the TX does not transmit at incorrect frequencies under low battery voltage conditions. It either remains on channel or stops transmitting. The latter can of course be implemented by using a lock detect and/or by switching off the PA under control of the battery monitor. For testing purposes this control is enabled/disabled by SPI.

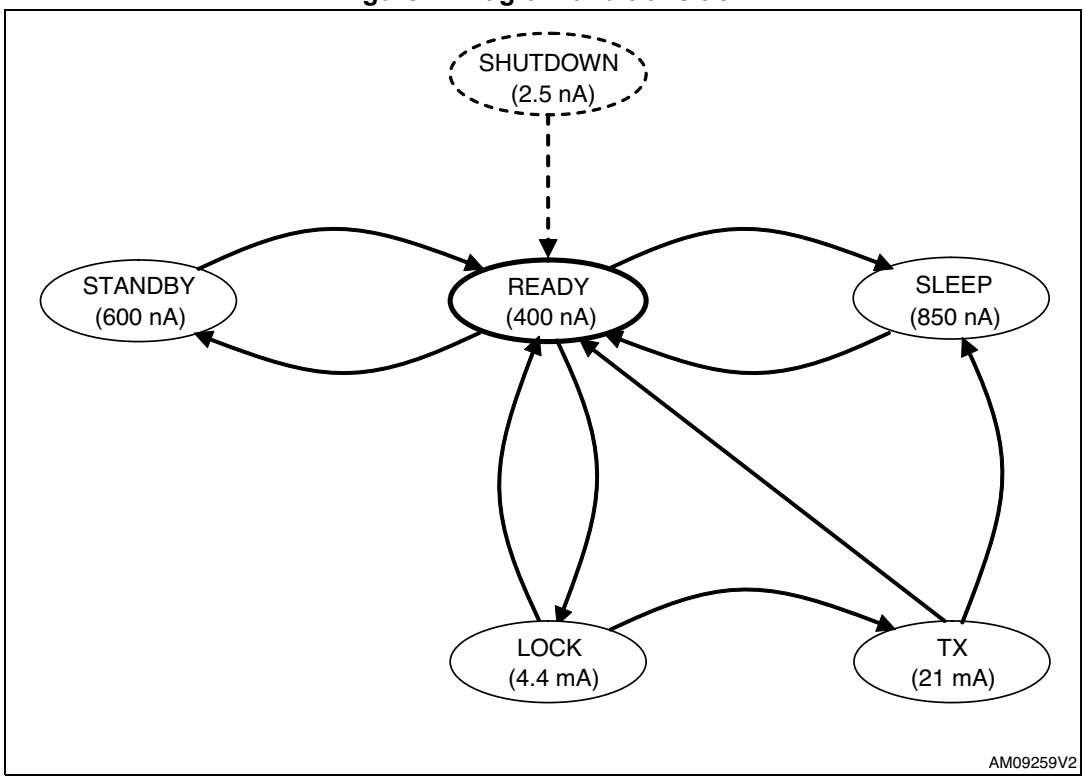
7 Operating modes

The STS1TX is equipped with a built-in main controller which controls the switching between the two main operating modes: transmit (TX).

In shutdown condition (the STS1TX can be switched on/off with the external pin SDN, all other functions/registers/commands are available through the SPI interface and GPIOs), no internal supply is generated (in order to minimize battery leakage), and hence, all stored data and configurations are lost. The GPIO and SPI ports during SHUTDOWN are in HiZ. From shutdown, the STS1TX can be switched on from the SDN pin and goes into READY state, which is the default, where the reference signal from XO is available.

From READY state, the STS1TX can be moved to LOCK state to generate the high precision LO signal and/or TX mode. At the end of the operations above, the STS1TX can return to its default state (READY) and can then be put into a sleep condition (SLEEP state), with very low power consumption. If no timeout is required, the STS1TX can be moved from READY to STANDBY state, which has the lowest possible current consumption while retaining FIFO, status and configuration registers. To manage the transitions towards and between these operating modes, the controller works as a state-machine, whose state switching is driven by SPI commands. See *Figure 4* for state diagram and transition time between states.

Figure 4. Diagram and transition



The STS1TX radio control has three stable states (READY, STANDBY, LOCK) which may be defined stable, and they are accessed by the specific commands (respectively READY, STANDBY, and LOCKTX), which can be left only if any other command is used. All other states are transient, which means that in a typical configuration, the controller remains in

those states, at most for any time-out timer duration. Also the READY and LOCK states behave as transients when they are not directly accessed with the specific commands (for example, when LOCK is temporarily used before reaching the TX state).

Table 18. States

STATE[6:0](1)	State/mode	Digital LDO	SPI	Xtal	RF Synth.	Wakeup timer	Response time to(2)
							TX
-	SHUTDOWN	OFF (register contents lost)	Off	Off	Off	Off	NA
0x40	STANDBY	ON (FIFO and register contents retained)	On	Off	Off	Off	125 µs
0x36	SLEEP		On	Off	Off	On	125 µs
0x03	READY (Default)		On	On	Off	Don't care	50 µs
0x0F	LOCK		On	On	On	Don't care	NA
0x5f	TX		On	On	On	Don't care	NA

1. All others values of STATE[6:0] are invalid and are an indication of an error condition due to bad registers configuration and/or hardware issue in the application board hosting STS1TX.
2. These values are crystal dependent. The values are referred to 52 MHz.

Note: Response time SHUTDOWN to READY is ~650 µs.

READY state is the default state after the power-on reset event. In the steady condition, the XO is settled and usable as the time reference for RCO calibration, for frequency synthesis, and as the system clock for the digital circuits.

The TX mode can be activated directly by the MCU using the TX command, or automatically if the state machine wakes up from SLEEP mode and some previous TX is pending. The values are intend to a VCO manual calibration.

In LOCK state the synthesizer is in a locking condition(a). If LOCK state is reached using specific command LOCKTX, the state machine remains in LOCK state and waits for the next command. This feature can be used by the MCU to perform preliminary calibrations, as the MCU can read the calibration word in the RCO_VCO_CALIBR_OUT register and store it in a non-volatile memory, and after that it requires a further tuning cycle.

When TX is activated by the TX command, the state machine goes into TX state and remains there until the current packet is fully transmitted or, in the case of direct mode TX, TXFIFO underflow condition is reached or the SABORT command is applied.

a. LOCK state is reached when one of the following events occurs first: lock detector assertion or locking timeout expiration.

After TX completion, the possible destinations are:

- TX, if the persistent-TX option is enabled in the PROTOCOL configuration registers
- PROTOCOL, if some protocol option (e.g. automatic re-transmission) is enabled
- READY, if TX is completed and no protocol option is in progress.

The SABORT command can always be used in TX state to break any deadlock condition and the subsequent destination depends on STS1TX programming according to the description above.

Commands are used in the STS1TX to change the operating mode, to enable/disable functions, and so on. A command is sent on the SPI interface and may be followed by any other SPI access without pulling CSn high.

The complete list of commands is reported in *Table 19*. Note that the command code is the second byte to be sent on the MOSI pin (the first byte must be 0x80).

Table 19. Commands list

Command code	Command name	Execution state	Description
0x60	TX	READY	Start to transmit
0x62	READY	STANDBY, SLEEP, LOCK	Go to READY
0x63	STANDBY	READY	Go to STANDBY
0x64	SLEEP	READY	Go to SLEEP
0x66	LOCKTX	READY	Go to LOCK state by using the TX configuration of the synthesizer
0x67	SABORT	TX	Exit from TX state and go to READY state
0x68	LDC_RELOAD	All	Reload the LDC timer with the value stored in the LDC_PRESCALER/COUNTER registers
0x69	SEQUENCE_UPDATE	All	Reload the packet sequence counter with the value stored in the PROTOCOL[2] register.
0x6A	AES Enc	All	Start the encryption routine
0x6B	AES Key	All	Start the procedure to compute the key for decryption
0x6C	AES Dec	All	Start decryption using the current key
0x6D	AES KeyDec	All	Compute the key and start decryption
0x70	SRES	All	Reset
0x72	FLUSHTXFIFO	All	Clean the TX FIFO

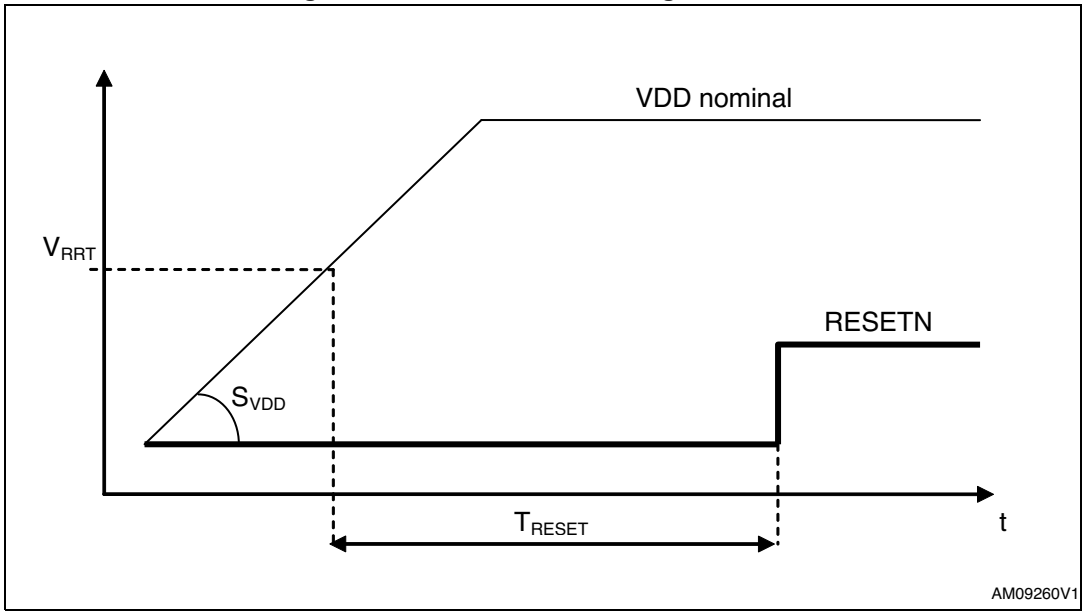
The commands are immediately valid after SPI transfer completion (i.e. no need for any CSn positive edge).

7.1 Reset sequence

The STS1TX includes an automatic power-on reset (POR) circuit which generates an internal RESETN active (low) level for a time T_{RESET} after the VDD reaches the reset

release threshold voltage V_{RRT} (provided that SDN is low), as shown below. The same reset pulse is generated after a step-down on the input pin SDN (provided that VDD>V_{RRT}).

Figure 5. Power-on reset timing and limits



The parameters V_{RRT} and T_{RESET} are fixed by design. At RESET, all the registers are initialized to their default values. Typical and extreme values are reported in the following table.

Table 20. POR parameters

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{RRT}	Reset startup threshold voltage		0.5		V
T_{RESET}	Reset pulse width	0.24	0.65	1.0	ms

Note: An SRES command is also available, which generates an internal RESET of the STS1TX.

7.2 Timer usage

Most of the timers are programmable via R/W registers. All timer registers are made up of two bytes: the first byte is a multiplier factor (prescaler); the second byte is a counter value.

Timer period= PRESCALER x COUNTER x Tclk

Note: If the counter register value (prescaler register value) is 0, the related timer never stops (infinite timeout), despite the value written in the prescaler register (counter register).

The available timers and their features are listed in the following table.