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STS3DPF60L

DUAL P-CHANNEL 60V - 0.10 Ω - 3A SO-8 STripFET™ MOSFET

Table 1: General Features

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STS3DPF60L	60 V	< 0.12 Ω	3 A

- TYPICAL $R_{DS}(on)$ = 0.10 Ω @ 10V
- STANDARD OUTLINE FOR EASY AUTOMATED SURFACE MOUNT ASSEMBLYY
- LOW THRESHOLD DRIVE

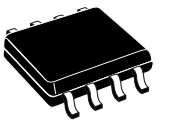
DESCRIPTION

This MOSFET is the latest development of STMicroelectronis unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

APPLICATIONS

- DC-DC CONVERTERS

Figure 1: Package



SO-8

Figure 2: Internal Schematic Diagram

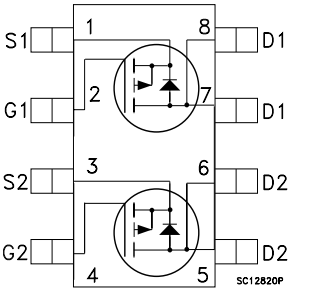


Table 2: Order Codes

PART NUMBER	MARKING	PACKAGE	PACKAGING
STS3DPF60L	S3DPF60L	SO-8	TAPE & REEL

Table 3: Absolute Maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	60	V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	60	V
V_{GS}	Gate- source Voltage	± 16	V
I_D	Drain Current (continuous) at T_C = 25°C Drain Current (continuous) at T_C = 100°C	3 1.9	A A
I_{DM}(•)	Drain Current (pulsed)	12	A
P_{tot}	Total Dissipation at T_C = 25°C	2	W
T_{stg}	Storage Temperature	-55 to 150	°C
T_j	Operating Junction Temperature		

(•) Pulse width limited by safe operating area.

Table 4: Thermal Data

Rthj-amb	(*)Thermal Resistance Junction-ambient	62.5	°C/W

(*) When Mounted on 1 inch^2 FR-4 board, 2 oz of Cu t ≤ 10 s

ELECTRICAL CHARACTERISTICS (T_{CASE} =25°C UNLESS OTHERWISE SPECIFIED)

Table 5: On/Off

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 250 µA, V_{GS} = 0	60			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating ,T_C= 125°C			1 10	µA µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ± 16 V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	1.5			V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10 V, I_D = 1.5 A V_{GS} = 4.5 V, I_D = 1.5 A		0.10 0.130	0.12 0.160	Ω Ω

ELECTRICAL CHARACTERISTICS (CONTINUED)

Table 6: Dynamic

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (*)	Forward Transconductance	V_{DS} = 10 V, I_D = 3 A		7.2		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V_{DS} = 25V f = 1 MHz V_{GS} = 0		630 121 49		pF pF pF
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on Delay Time Rise Time Turn-off Delay Time Fall Time	V_{DD} = 30 V , I_D = 1.5 A R_G = 4.7 Ω, V_{GS} = 4.5 V (see Figure 16)		124 54 39 14.5		ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V_{DD}= 48V, I_D= 3A V_{GS}=4.5V (see Figure 19)		11.6 4.5 4.7	15.7	nC nC nC

Table 7: Source Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (•)	Source-drain Current Source-drain Current (pulsed)				3 12	A A
V_{SD} (*)	Forward On Voltage	I_{SD} = 3 A, V_{GS} = 0			1.2	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 3 A, di/dt = 100A/µs V_{DD} = 30 V, T_j = 150°C (see Figure 17)		44 68.2 3.1		ns nC A

(*)Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
(•)Pulse width limited by safe operating area.

Figure 3: Safe Operating Area

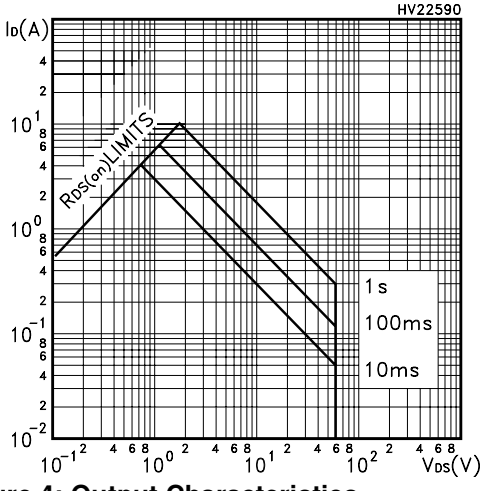


Figure 4: Output Characteristics

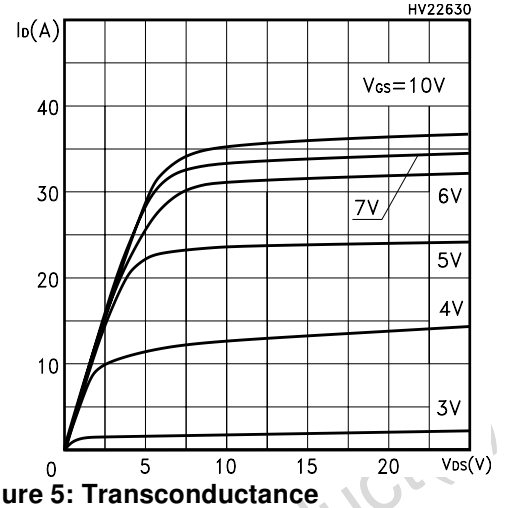


Figure 5: Transconductance

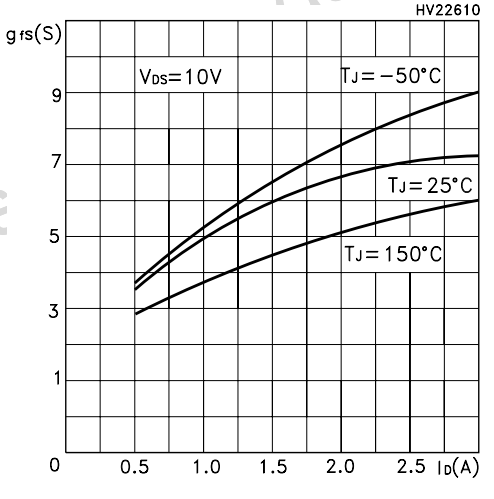


Figure 6: Thermal Impedance

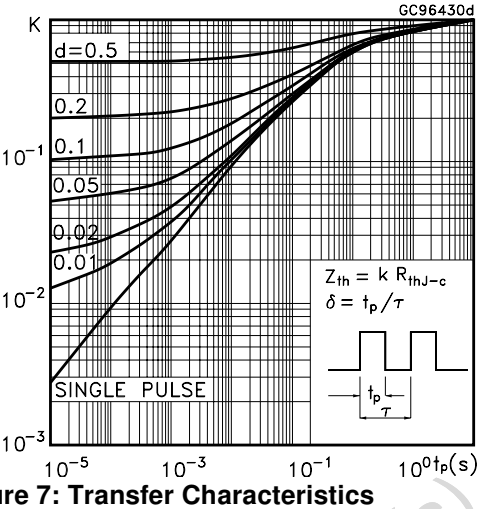


Figure 7: Transfer Characteristics

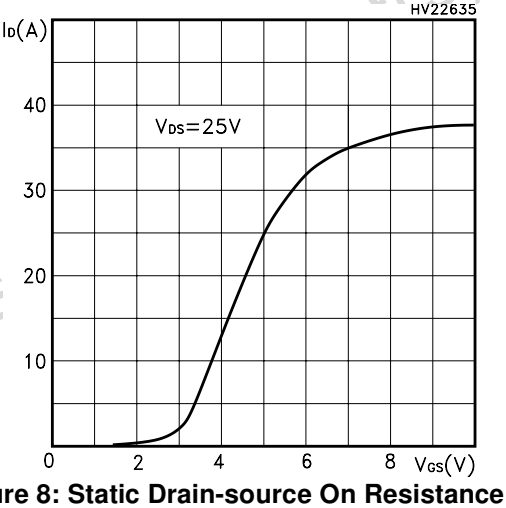


Figure 8: Static Drain-source On Resistance

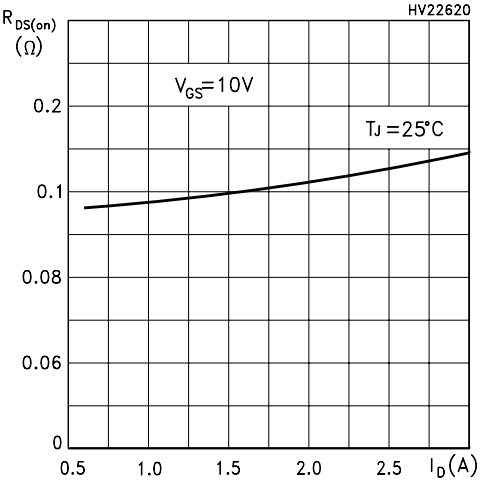


Figure 9: Gate Charge vs Gate-source Voltage

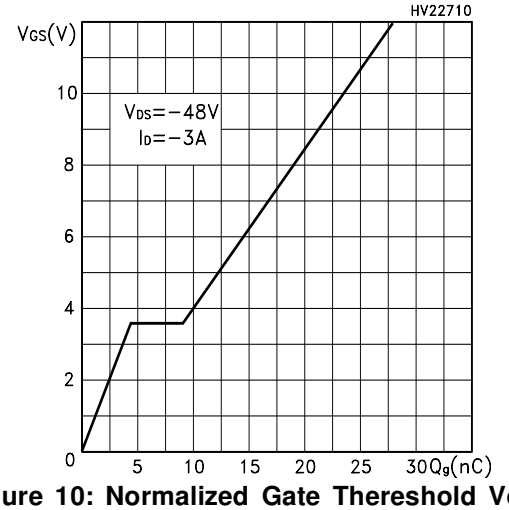


Figure 10: Normalized Gate Thereshold Voltage vs Temperature

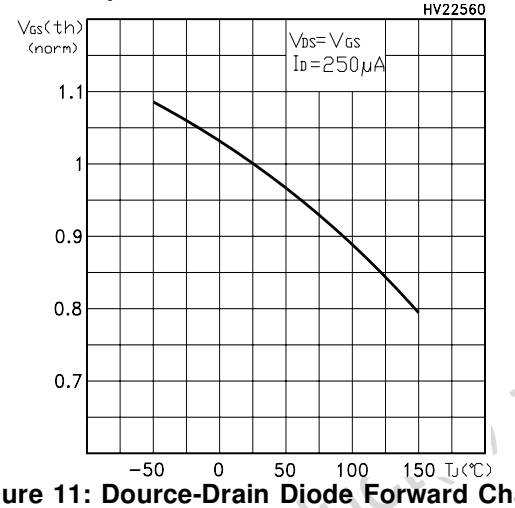


Figure 11: Dource-Drain Diode Forward Characteristics

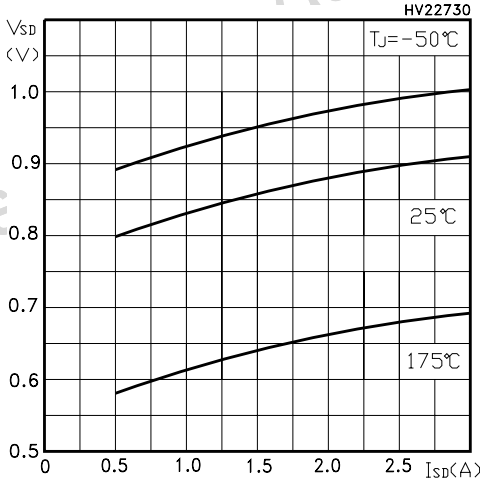


Figure 12: Capacitance Variations

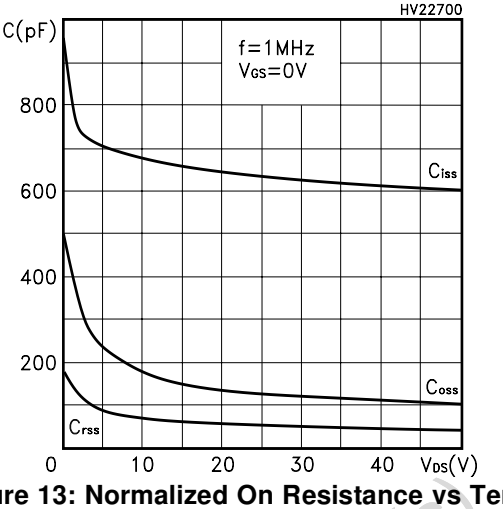


Figure 13: Normalized On Resistance vs Temperature

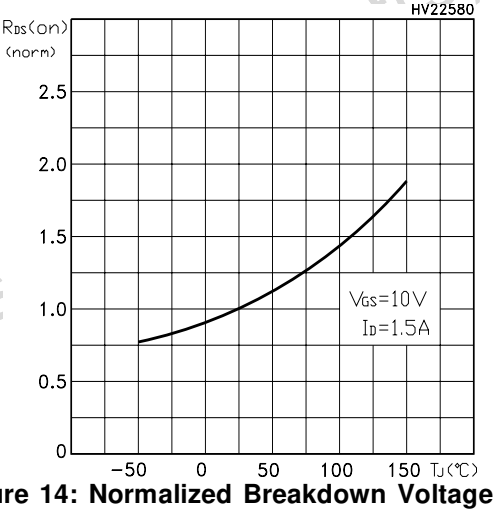


Figure 14: Normalized Breakdown Voltage vs Temperature

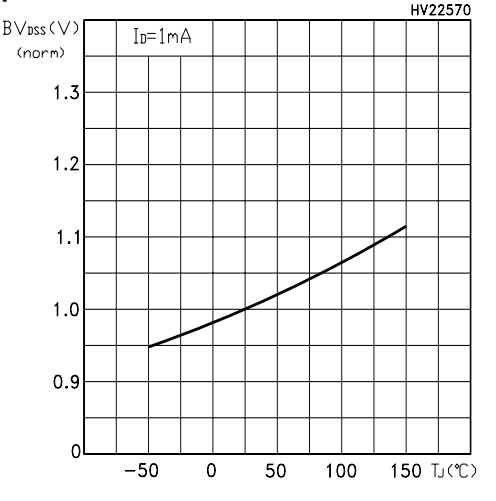


Figure 15: Unclamped Inductive Load Test Circuit

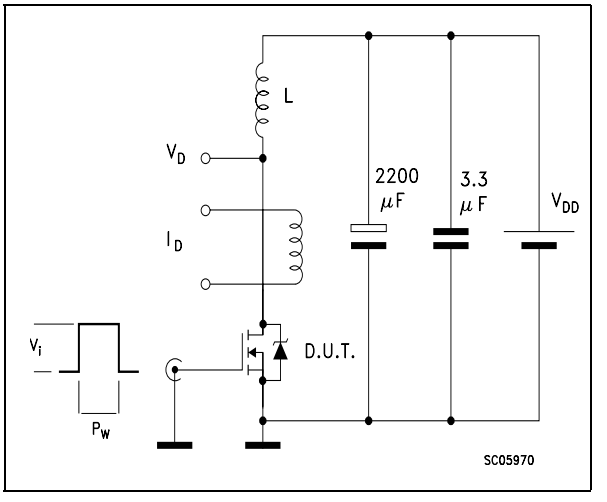


Figure 16: Switching Times Test Circuit For Resistive Load

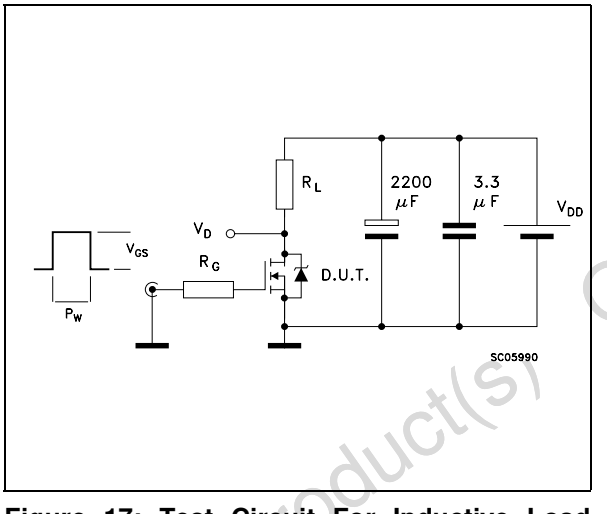


Figure 17: Test Circuit For Inductive Load Switching and Diode Recovery Times

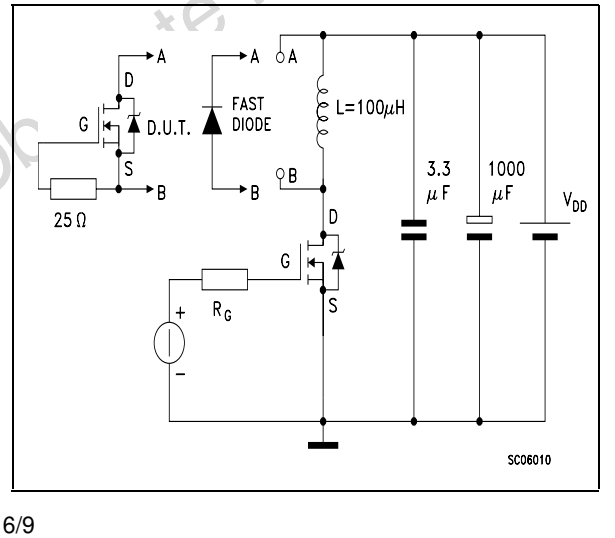


Figure 18: Unclamped Inductive Wafeform

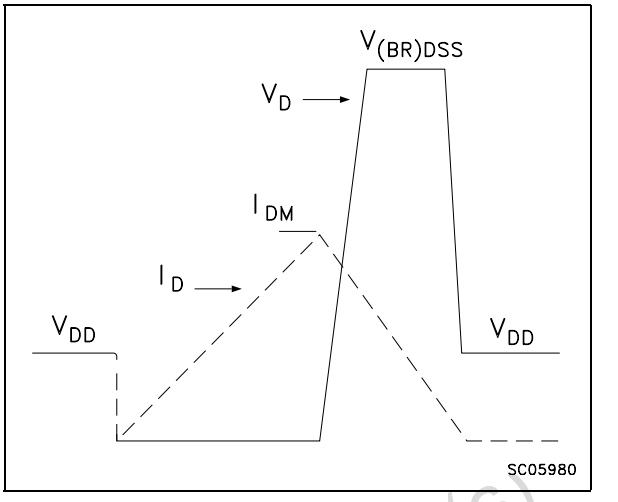
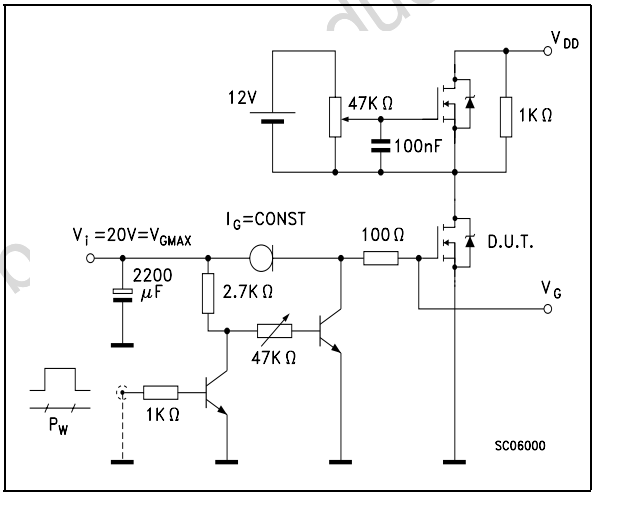


Figure 19: Gate Charge Test Circuit



SO-8 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					

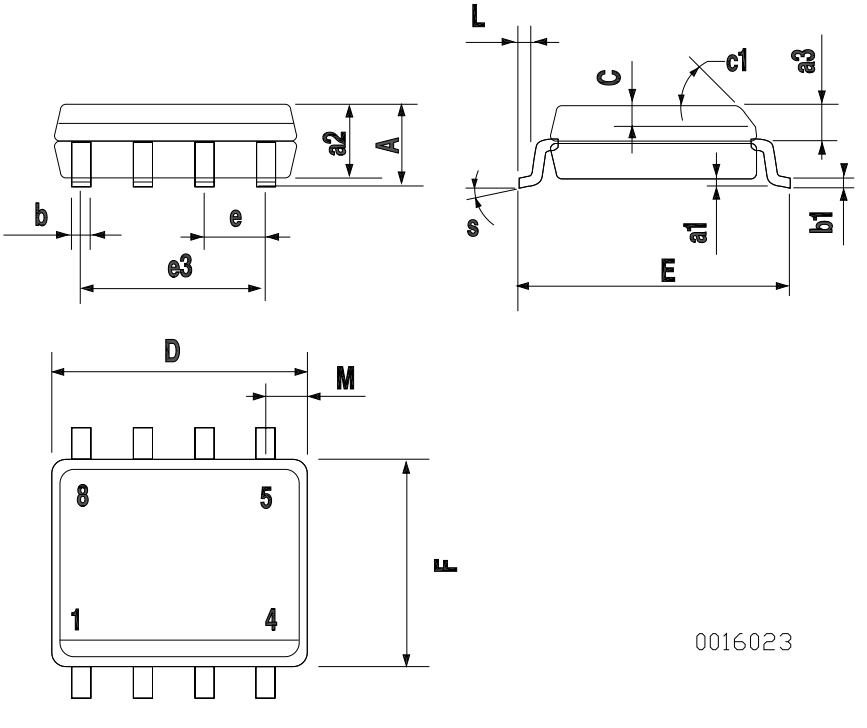


Table 8: Revision History

Date	Revision	Description of Changes
16-Sep-2004	1	New release.