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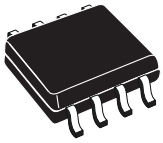
STS4C3F60L

N-channel 60V - 0.045 Ω - 4A SO-8
Complementary pair STripFET™ Power MOSFET

General features

Type	V_{DSS}	$R_{DS(on)}$	I_D
STS4C3F60L(N-channel)	60V	<0.056Ω	4A
STS4C3F60L(P-channel)	60V	<0.120Ω	3A

- Standard outline for easy automated surface mount assembly
- Low threshold drive

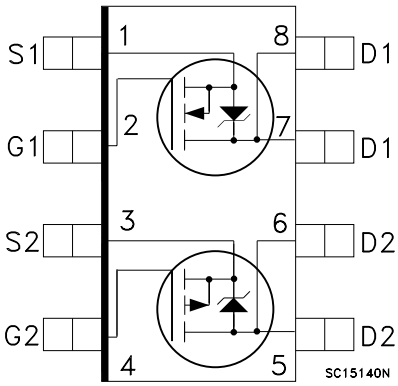


S0-8

Description

This Power MOSFET is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

Internal schematic diagram



Applications

- Switching application

Order codes

Part number	Marking	Package	Packaging
STS4C3F60L	S4C3F60L	SO-8	Tape & reel

Contents

1 Electrical ratings 3

2 Electrical characteristics 4

2.1 Electrical characteristics (curves) 6

3 Test circuit 10

4 Package mechanical data 11

5 Revision history 13

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		N-channel	P-channel	
V_{DS}	Drain-source voltage (v_{gs} = 0)	60		V
V_{GS}	Gate- source voltage	±16		V
I_D	Drain current (continuous) at T_C = 25°C	4	3	A
I_D	Drain current (continuous) at T_C = 100°C	2.5	1.9	A
I_{DM} (1)	Drain current (pulsed)	16	12	A
P_{TOT}	Total dissipation at T_C = 25°C	2		W
T_{stg} T_j	Storage temperature Max. operating junction temperature	-55 to 150		°C

1. Pulse width limited by safe operating area

Note: For the P-CHANNEL MOSFET actual polarity of voltages and current has to be reversed

Table 2. Thermal data

$R_{thj\text{-}a}$ (1)	Thermal resistance junction-ambient	62.5	°C/W

1. When mounted on 1 in^2 pad of 2 oz. copper, t ≤10 sec.

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown voltage	I_D = 250 µA, V_{GS} = 0	n-ch p-ch	60 60			V V
I_{DSS}	Zero gate voltage Drain current (V_{GS} = 0)	V_{DS} = Max rating V_{DS}=Max rating, T_C=125°C	n-ch p-ch			1 10	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±16V	n-ch p-ch			±100 ±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250µA	n-ch p-ch	1 1.5			V V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10V, I_D = 2A V_{GS} = 10V, I_D = 1.5A V_{GS} = 10V, I_D = 2A V_{GS} = 10V, I_D = 1.5A	n-ch p-ch n-ch p-ch		0.045 0.100 0.050 0.130	0.055 0.120 0.065 0.160	Ω Ω Ω Ω

Table 4. Dynamic

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} = 30 V, I_D= 2A V_{DS} = 10 V, I_D= 3A	n-ch p-ch		7 7.2		S S
C_{iss}	Input capacitance	V_{DS} = 25V, f = 1 MHz, V_{GS} = 0	n-ch p-ch		1030 630		pF pF
C_{oss}	Output capacitance		n-ch p-ch		140 121		pF pF
C_{rss}	Reverse transfer capacitance		n-ch p-ch		40 49		pF pF
Q_g	Total gate charge	**N-channel** V_{DD}=48V I_D4A V_{GS}=4.5V **P-channel** V_{DD} = 48V I_D = 3A V_{GS}= 4.5V (see Figure 26)	n-ch p-ch		15 11.6	20.4 15.7	nC nC
Q_{gs}	Gate-source charge		n-ch p-ch		4 4.5		nC nC
Q_{gd}	Gate-drain charge		n-ch p-ch		4 4.7		nC nC

1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5.

Table 5. Switching times

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	**N-channel** V_{DD} = 30 V, I_D = 2A R_G=4.7 Ω, V_{GS} = 4.5V **P-channel** V_{DD} = 30 V, I_D = 1.5 A R_G=4.7 Ω, V_{GS} = 4.5V (see Figure 25)	n-ch p-ch n-ch p-ch		15 124 28 54		ns ns ns ns
$t_{d(off)}$ t_f	Turn-off delay time Fall time	**N-channel** V_{DD} = 30 V, I_D = 2A R_G=4.7 Ω, V_{GS} = 4.5V **P-channel** V_{DD} = 30 V, I_D = 1.5 A R_G=4.7 Ω, V_{GS} = 4.5V (see Figure 25)	n-ch p-ch n-ch p-ch		45 39 10 14.5		ns ns ns ns

Table 6. Source drain diode

Symbol	Parameter	Test conditions		Min.	Typ.	Max	Unit
I_{SD}	Source-drain current		n-ch p-ch			4 3	A A
I_{SDM} (1)	Source-drain current (pulsed)		n-ch p-ch			16 12	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 4A, V_{GS} = 0 I_{SD} = 3A, V_{GS} = 0	n-ch p-ch			1.2 1.2	V V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	**N-channel** I_{SD} = 4A, di/dt = 100A/µs V_{DD}=20 V,T_j =150 °C **P-channel** I_{SD} = 3A, di/dt = 100A/µs V_{DD}=20 V, T_j =150 °C (see Figure 27)	n-ch p-ch n-ch p-ch n-ch p-ch		85 44 85 68.2 2 3.1		ns ns nC nC A A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe operating n-ch

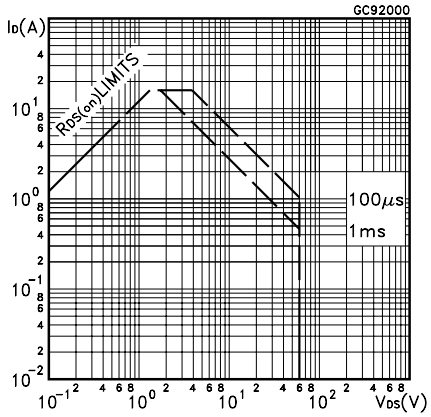


Figure 2. Thermal impedance for complementary pair

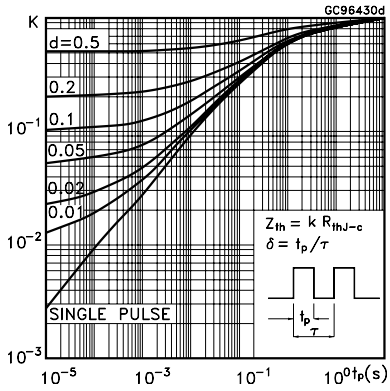


Figure 3. Output characteristics n-ch

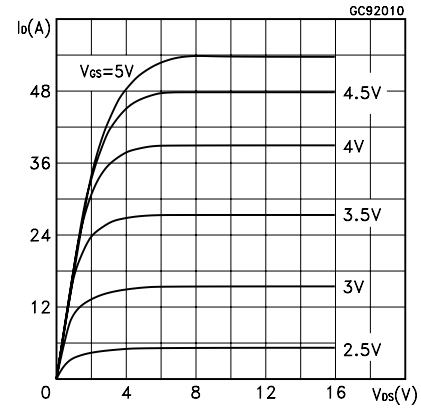


Figure 4. Transfer characteristics n-ch

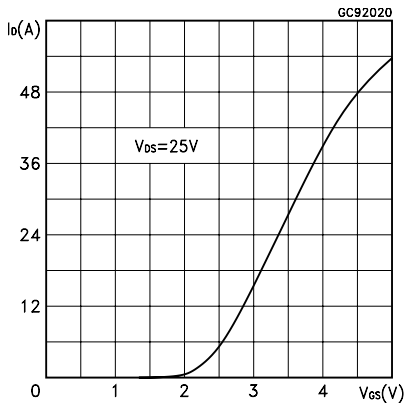


Figure 5. Transconductance n-ch

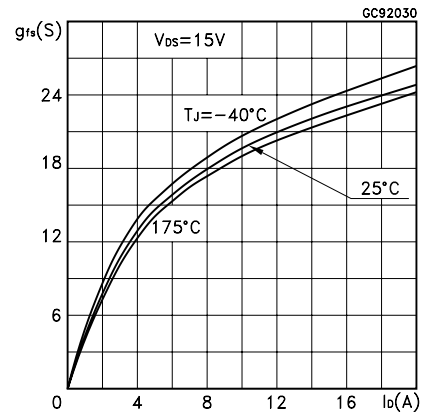


Figure 6. Static drain-source on resistance n-ch

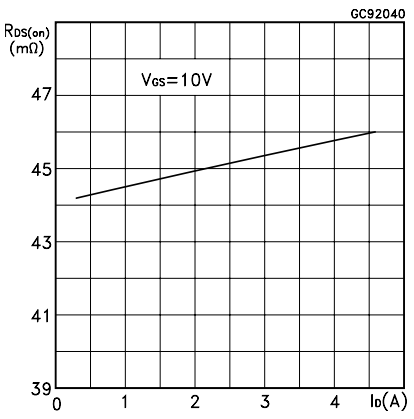


Figure 7. Gate charge vs. gate-source voltage n-ch

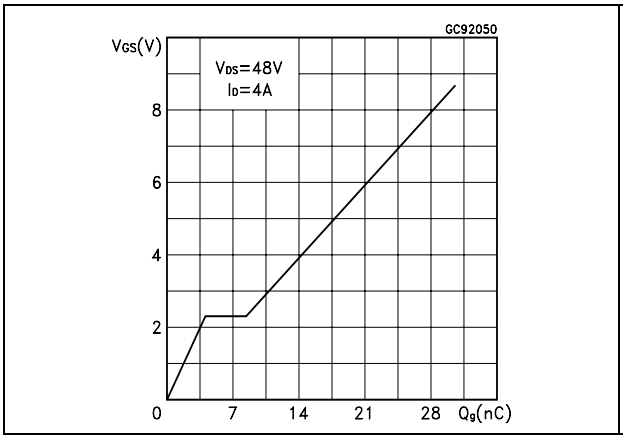


Figure 8. Capacitance variations n-ch

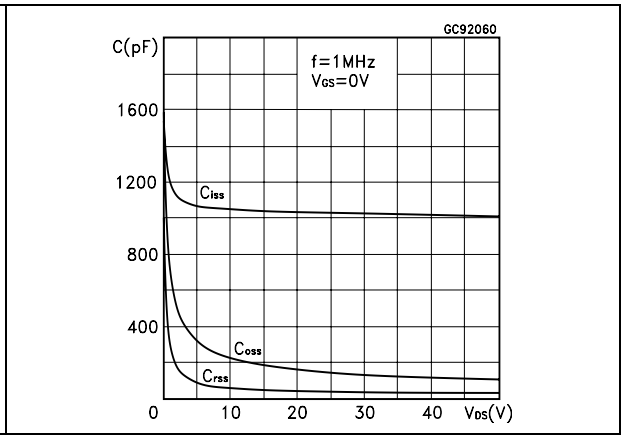


Figure 9. Normalized gate threshold voltage vs. temperature n-ch

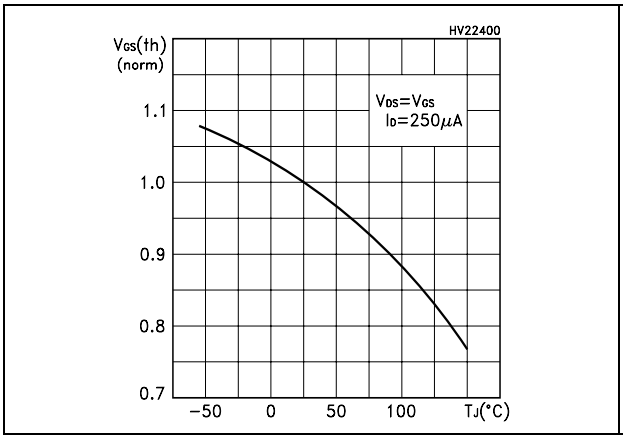


Figure 10. Normalized on resistance vs. temperature n-ch

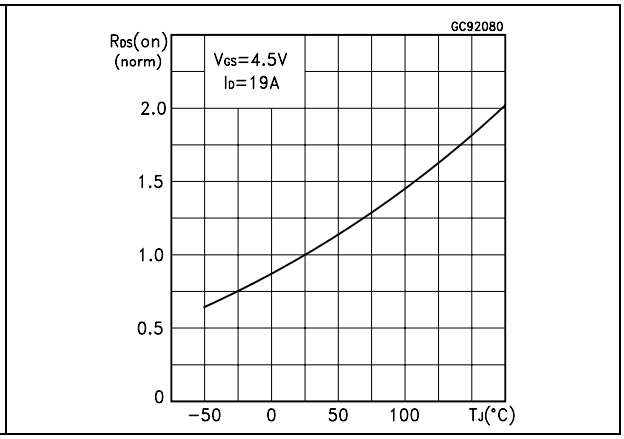


Figure 11. Source-drain diode forward characteristics n-ch

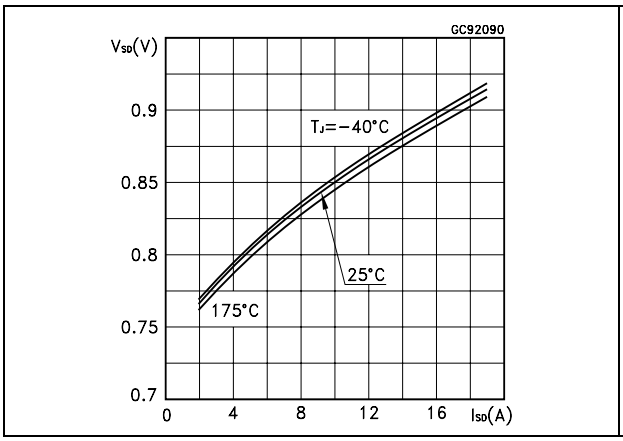


Figure 12. Normalized breakdown voltage vs. temperature n-ch

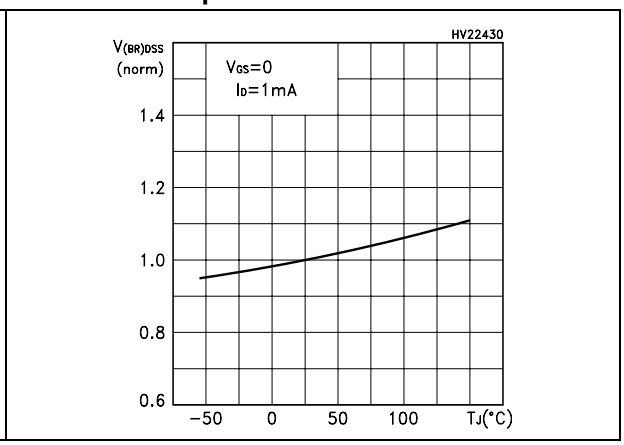


Figure 13. Safe operating p-ch

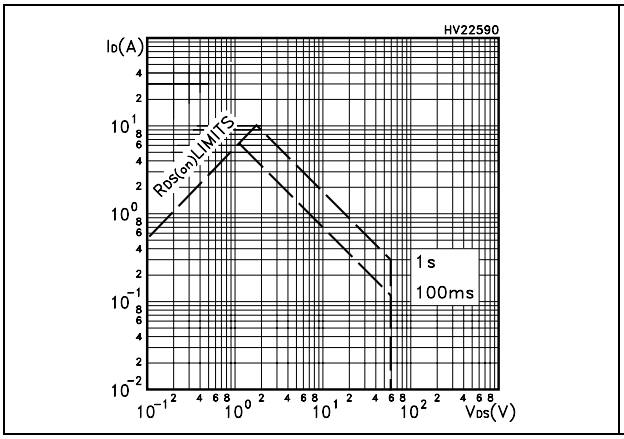


Figure 14. Thermal impedance p-ch

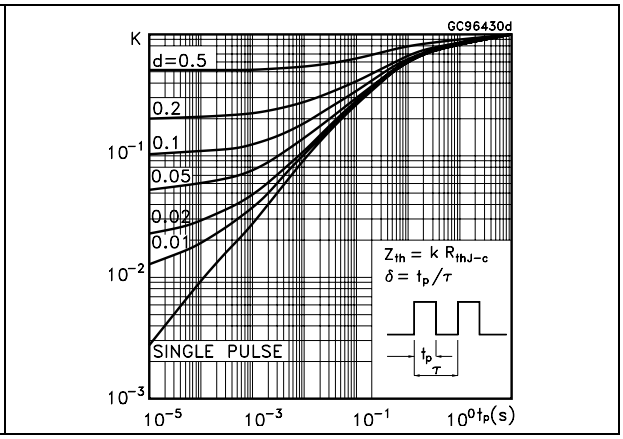


Figure 15. Output characteristics p-ch

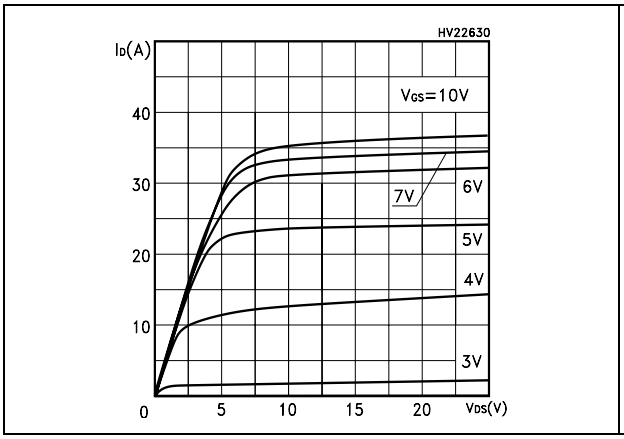


Figure 16. Transfer characteristics p-ch

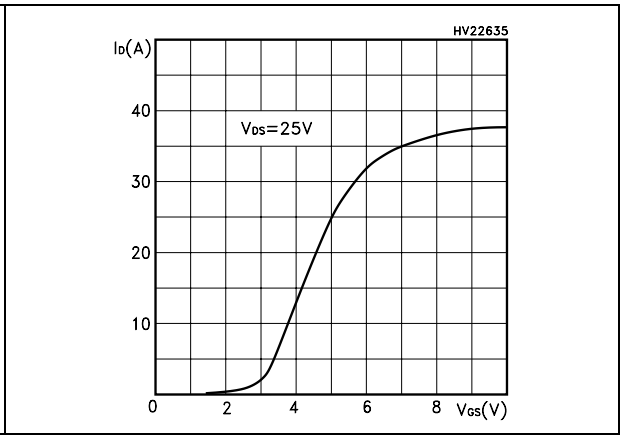


Figure 17. Transconductance p-ch

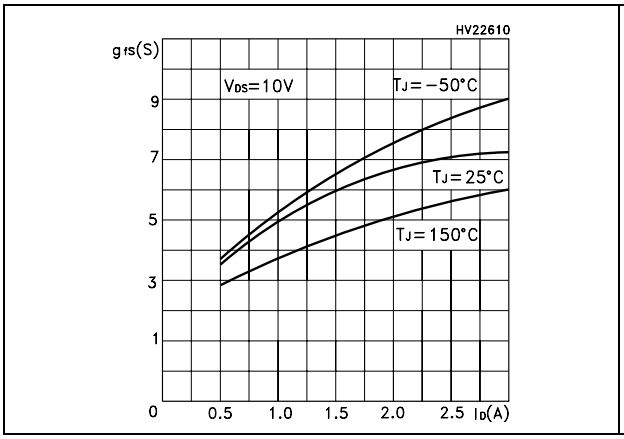


Figure 18. Static drain-source on resistance p-ch

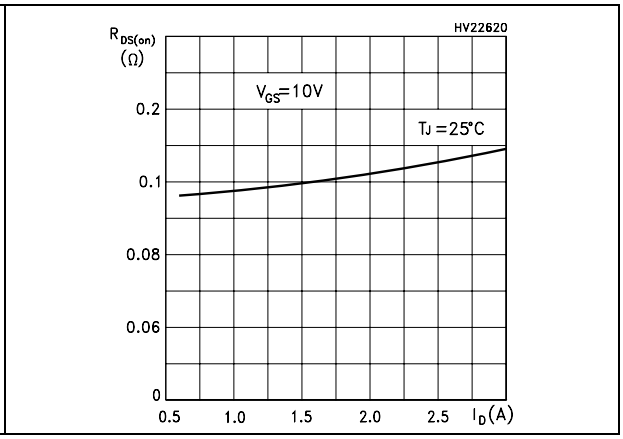


Figure 19. Gate charge vs. gate-source voltage p-ch

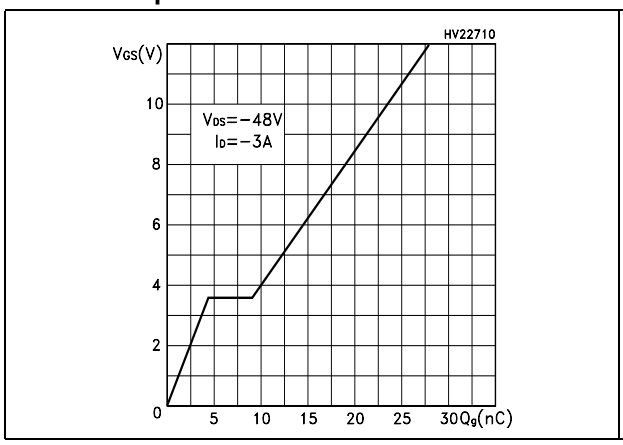


Figure 20. Capacitance variations p-ch

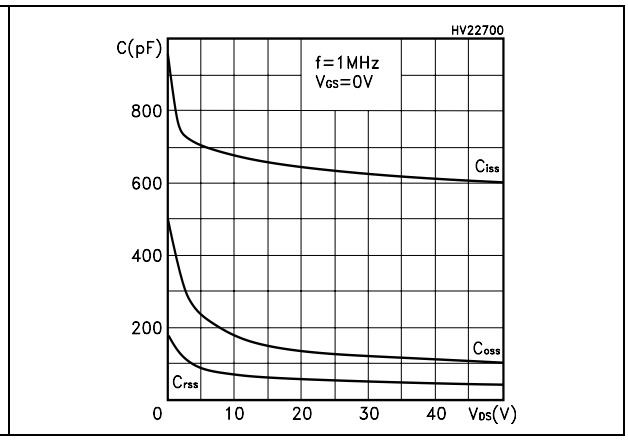


Figure 21. Normalized gate threshold voltage vs. temperature p-ch

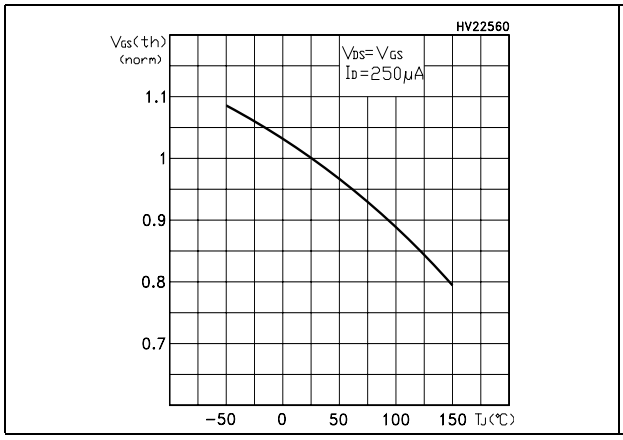


Figure 22. Normalized on resistance vs. temperature p-ch

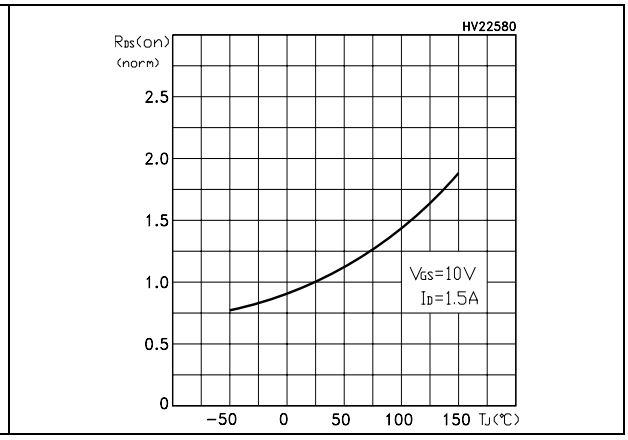


Figure 23. Source-drain diode forward characteristics p-ch

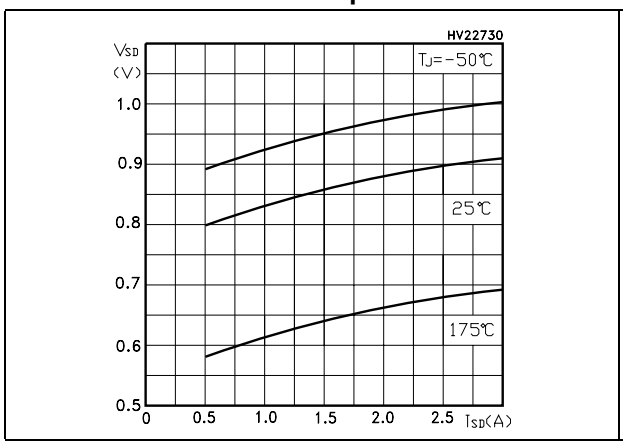
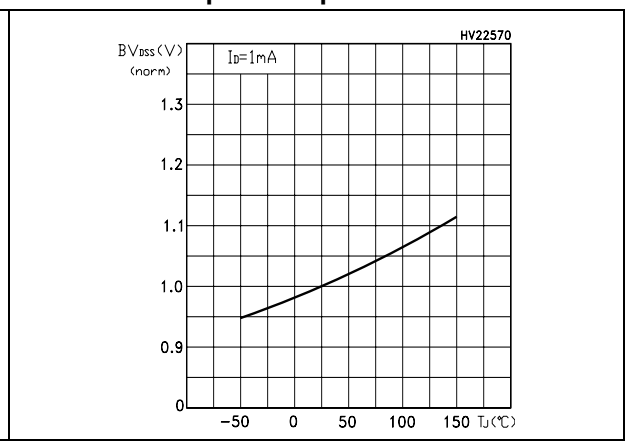


Figure 24. Normalized breakdown voltage vs. temperature p-ch



3 Test circuit

Figure 25. Switching times test circuit for resistive load

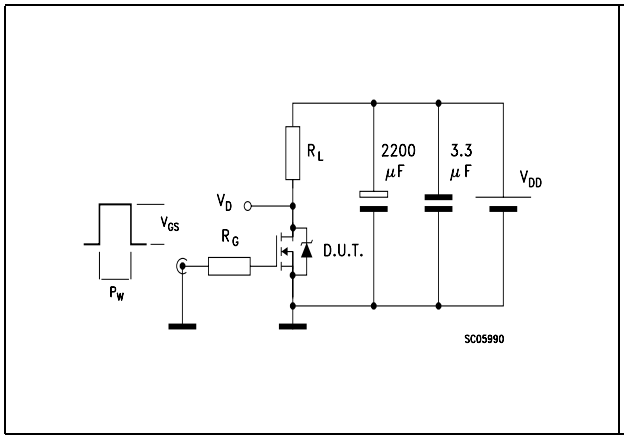


Figure 26. Gate charge test circuit

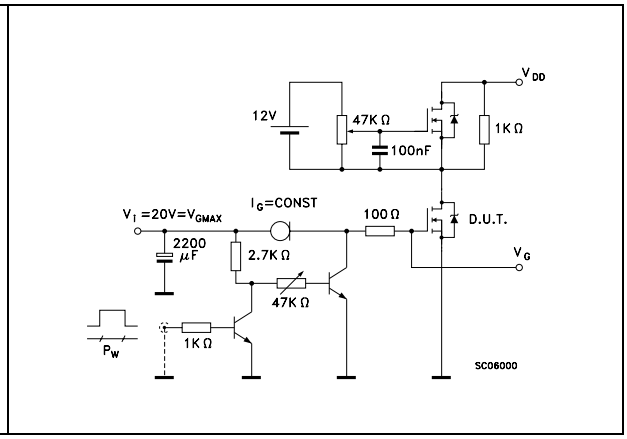


Figure 27. Test circuit for inductive load switching and diode recovery times

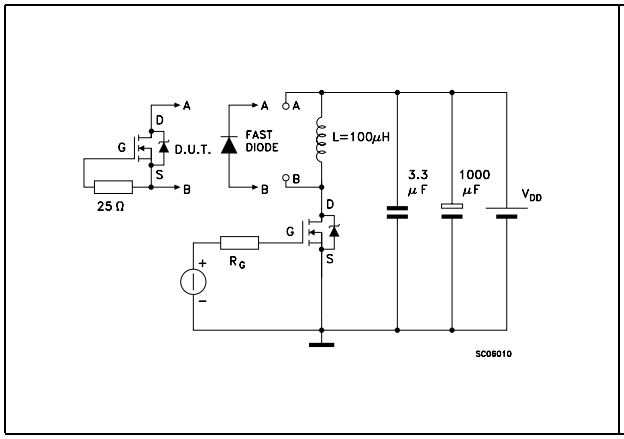


Figure 28. Unclamped Inductive load test circuit

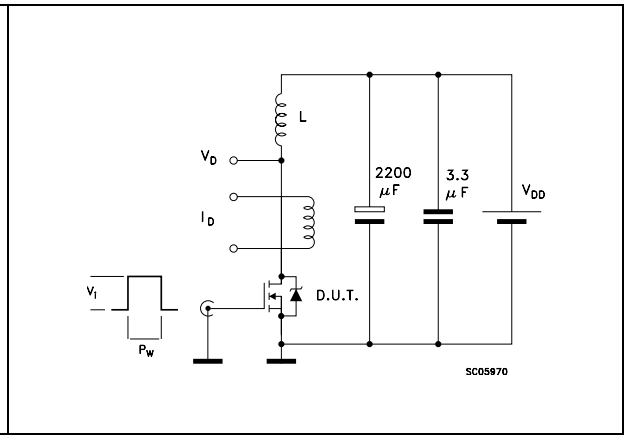


Figure 29. Unclamped inductive waveform

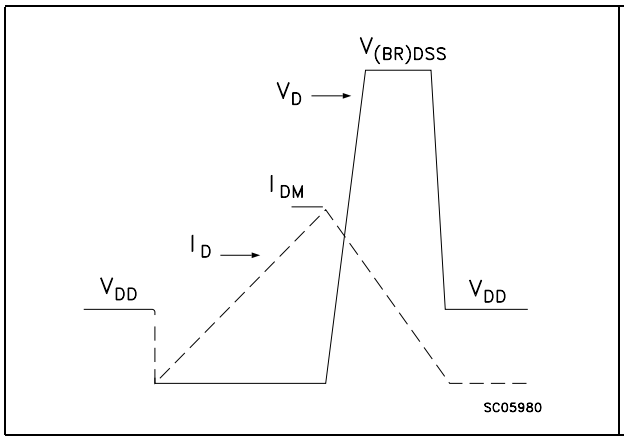
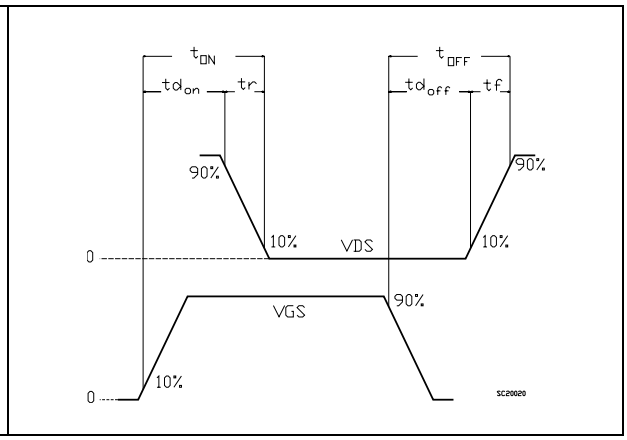


Figure 30. Switching time waveform

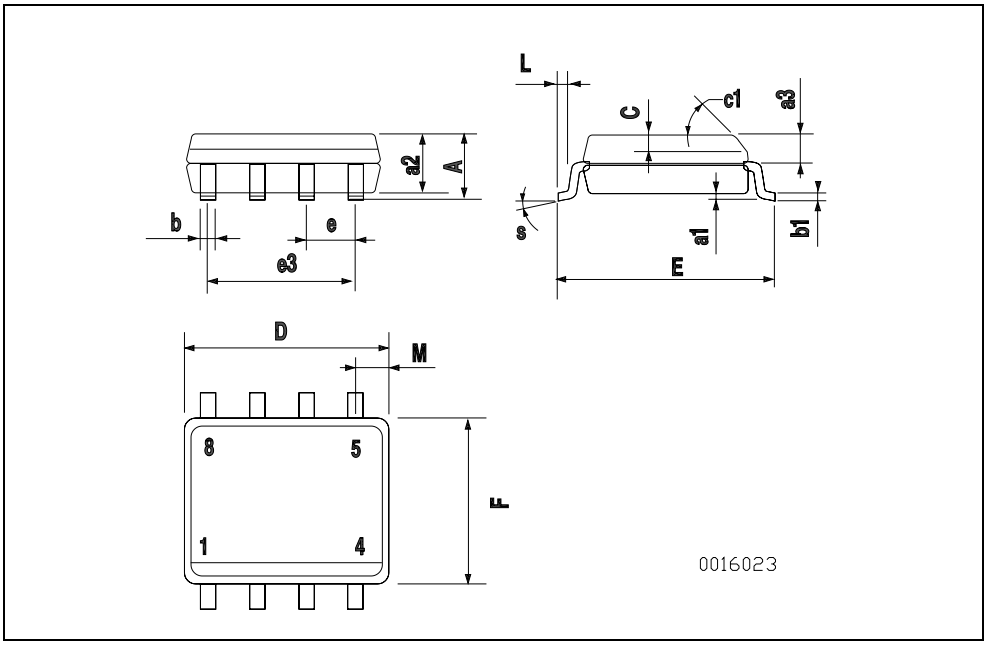


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at : *www.st.com*

SO-8 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					



5 Revision history

Table 7. Revision history

Date	Revision	Changes
28-Sep-2004	1	First release
13-Nov-2006	2	The document has been reformatted
26-Jan-2007	3	Typo mistake on *Table 1*.

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