



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

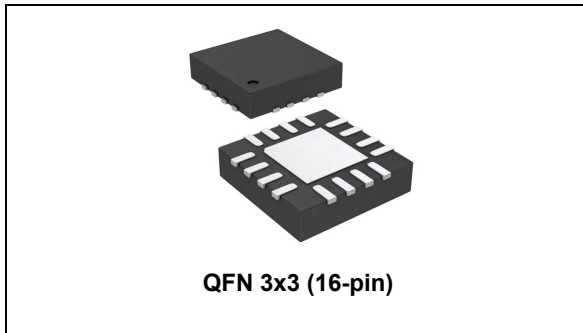


---

**Low voltage triple half-bridge motor driver for BLDC motors**

---

Datasheet - production data

**Description**

The STSPIN230 device integrates a triple half-bridge low  $R_{DS(ON)}$  power stage in a small QFN - 3 x 3 mm package.

The device is designed to operate in battery-powered scenarios and can be forced into a zero-consumption state, allowing a significant increase in battery life.

The device offers a complete set of protection including overcurrent, overtemperature and short-circuit protection.

**Features**

- Operating voltage from 1.8 to 10 V
- Maximum output current 1.3 A<sub>rms</sub>
- $R_{DS(ON)}$  HS + LS = 0.4  $\Omega$  typ.
- Full protection set
  - Non-dissipative overcurrent protection
  - Short-circuit protection
  - Thermal shutdown
  - Interlocking function
- Energy saving and long battery life with standby consumption less than 80 nA

**Applications**

- Battery-powered 3-phase brushless (BLDC) motors in applications such as:
  - Toys
  - Robotics
  - Portable medical equipment

# Contents

- 1      Block diagram ..... 5**
- 2      Electrical data ..... 6**
  - 2.1 Absolute maximum ratings ..... 6
  - 2.2 Recommended operating conditions ..... 6
  - 2.3 Thermal data ..... 6
  - 2.4 ESD protection ratings ..... 7
- 3      Electrical characteristics ..... 8**
- 4      Pin description ..... 10**
- 5      Typical applications ..... 12**
- 6      Functional description ..... 13**
  - 6.1 Standby and power-up ..... 13
  - 6.2 Motor driving ..... 13
  - 6.3 Overcurrent and short-circuit protection ..... 14
  - 6.4 Thermal shutdown ..... 16
- 7      Graphs ..... 17**
- 8      Package information ..... 19**
  - 8.1 VFQFPN 3x3x1.0 16L package information ..... 19
- 9      Ordering information ..... 21**
- 10     Revision history ..... 21**

## List of tables

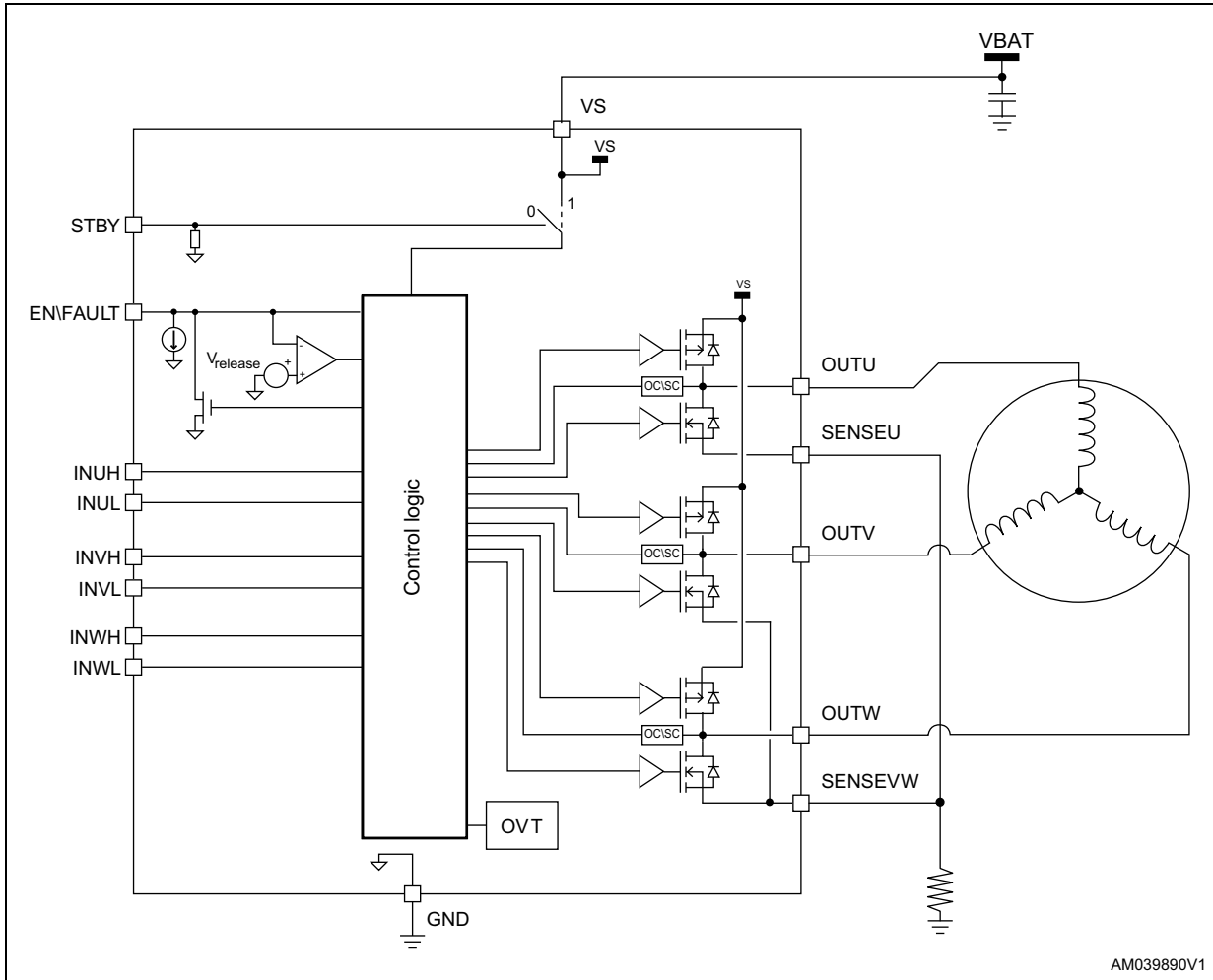
Table 1.	Absolute maximum ratings . . . . .	6
Table 2.	Recommended operating conditions . . . . .	6
Table 3.	Thermal data . . . . .	6
Table 4.	ESD protection ratings . . . . .	7
Table 5.	Electrical characteristics . . . . .	8
Table 6.	Pin description . . . . .	10
Table 7.	Typical application values . . . . .	12
Table 8.	INxH and INxL . . . . .	13
Table 9.	VFQFPN 3x3x1.0 16L package mechanical data . . . . .	20
Table 10.	Device summary . . . . .	21
Table 11.	Document revision history . . . . .	21

## List of figures

Figure 1.	Block diagram . . . . .	5
Figure 2.	Pin connection (top view) . . . . .	10
Figure 3.	Typical application schematic . . . . .	12
Figure 4.	Overcurrent and short-circuit protections management . . . . .	14
Figure 5.	Disable time versus $R_{EN}$ and $C_{EN}$ values ( $V_{DD} = 3.3\text{ V}$ ) . . . . .	15
Figure 6.	Disable time versus $R_{EN}$ and $C_{EN}$ values ( $V_{DD} = 1.8\text{ V}$ ) . . . . .	15
Figure 7.	Thermal shutdown management . . . . .	16
Figure 8.	Power stage resistance versus supply voltage . . . . .	17
Figure 9.	Power stage resistance versus temperature . . . . .	17
Figure 10.	Overcurrent threshold versus supply voltage . . . . .	18
Figure 11.	VFQFPN 3x3x1.0 16L package outline . . . . .	19
Figure 12.	VFQFPN 3x3x1.0 16L recommended footprint . . . . .	20

# 1 Block diagram

Figure 1. Block diagram



## 2 Electrical data

### 2.1 Absolute maximum ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Test condition	Value	Unit
$V_S$	Supply voltage		-0.3 to 11	V
$V_{IN}$	Logic input voltage		-0.3 to 5.5	V
$V_{OUT} - V_{SENSE}$	Output to sense voltage drop		up to 12	V
$V_S - V_{OUT}$	Supply to output voltage drop		up to 12	V
$V_{SENSE}$	Sense pins voltage		-1 to 1	V
$I_{OUT,RMS}$	Continuous power stage output current (each bridge)		1.3	$A_{RMS}$
$T_{j,OP}$	Operative junction temperature		-40 to 150	°C
$T_{j,STG}$	Storage junction temperature		-55 to 150	°C

### 2.2 Recommended operating conditions

Table 2. Recommended operating conditions

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_S$	Supply voltage		1.8		10	V
$V_{IN}$	Logic input voltage		0		5	V
$t_{INw}$	Logic inputs positive/negative pulse width		300			ns

### 2.3 Thermal data

Table 3. Thermal data

Symbol	Parameter	Conditions	Value	Unit
$R_{thJA}$	Junction to ambient thermal resistance	Natural convection, according to JESD51-2a <sup>(1)</sup>	57.1	°C/W
$R_{thJctop}$	Junction to case thermal resistance (top side)	Simulation with cold plate on package top	67.3	°C/W
$R_{thJcbot}$	Junction to case thermal resistance (bottom side)	Simulation with cold plate on exposed pad	9.1	°C/W
$R_{thJB}$	Junction to board thermal resistance	According to JESD51-8 <sup>(1)</sup>	23.3	°C/W
$\Psi_{JT}$	Junction to top characterization	According to JESD51-2a <sup>(1)</sup>	3.3	°C/W
$\Psi_{JB}$	Junction to board characterization	According to JESD51-2a <sup>(1)</sup>	22.6	°C/W

1. Simulated on a 21.2 x 21.2 mm board, 2s2p 1 Oz copper and four 300  $\mu$ m vias below exposed pad.

## 2.4 ESD protection ratings

**Table 4. ESD protection ratings**

Symbol	Parameter	Test condition	Class	Value	Unit
HBM	Human body model	Conforming to ANSI/ESDA/JEDEC JS-001-2014	2	2	kV
CDM	Charge device model	Conforming to ANSI/ESDA/JEDEC JS-002-2014	C2	750	V



### 3 Electrical characteristics

Testing conditions:  $V_S = 5\text{ V}$ ,  $T_j = 25\text{ °C}$  unless otherwise specified.

**Table 5. Electrical characteristics**

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
<b>Supply</b>						
$V_{Sth(ON)}$	$V_S$ turn-on voltage	$V_S$ rising from 0 V	1.45	1.65	1.79	V
$V_{Sth(OFF)}$	$V_S$ turn-off voltage	$V_S$ falling from 5 V	1.3	1.45	1.65	V
$V_{Sth(HYS)}$	$V_S$ hysteresis voltage			180		mV
$I_S$	$V_S$ supply current	No commutations, EN = 0		900	1300	$\mu\text{A}$
		No commutations, EN = 1		1500	1950	$\mu\text{A}$
$I_{S,STBY}$	$V_S$ standby current	STBY = 0 V		10	80	nA
$V_{STBYL}$	Standby low logic level input voltage				0.9	V
$V_{STBYH}$	Standby high logic level input voltage		1.48			V
<b>Power stage</b>						
$R_{DS(ON)HS+LS}$	Total on resistance HS + LS	$V_S = 10\text{ V}$ , $I_{OUT} = 1.3\text{ A}$		0.4	0.65	$\Omega$
		$V_S = 10\text{ V}$ , $I_{OUT} = 1.3\text{ A}$ , $T_j = 125\text{ °C}^{(1)}$		0.53	0.87	
		$V_S = 3\text{ V}$ , $I_{OUT} = 0.4\text{ A}$		0.53	0.8	
$I_{DSS}$	Leakage current	OUTx = $V_S$			1	$\mu\text{A}$
		OUTx = GND	- 1			
$V_{DF}$	Freewheeling diode forward voltage	$I_D = 1.3\text{ A}$		0.9		V
$t_{rise}$	Rise time	$V_S = 10\text{ V}$ ; unloaded outputs		10		ns
$t_{fall}$	Fall time	$V_S = 10\text{ V}$ ; unloaded outputs		10		ns
$t_{DT}$	Integrated dead time			50		ns
<b>Logic IOs</b>						
$V_{IH}$	High logic level input voltage		1.6			V
$V_{IL}$	Low logic level input voltage				0.6	V
$V_{RELEASE}$	FAULT open drain release voltage				0.4	V
$V_{OL}$	EN low logic level output voltage	$I_{EN} = 4\text{ mA}$			0.4	V
$R_{STBY}$	STBY pull-down resistance			36		k $\Omega$
$I_{PDEN}$	EN pull-down current			10.5		$\mu\text{A}$
$t_{End}$	EN input propagation delay	From EN falling edge to OUT high impedance		55		ns

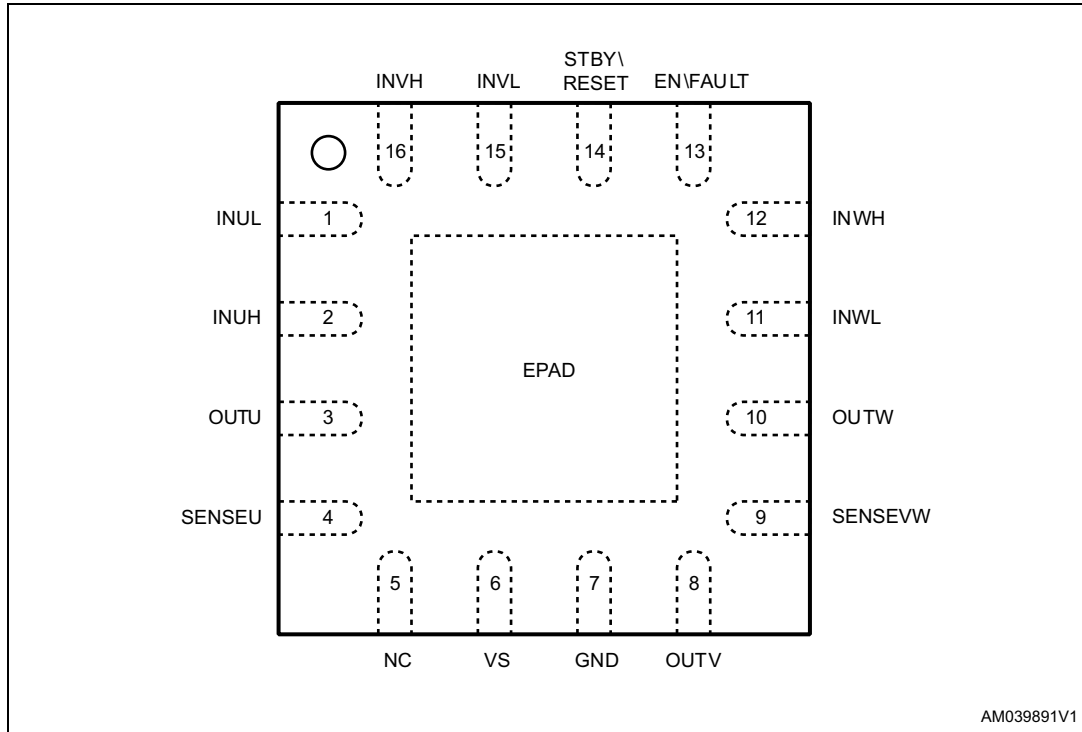
Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{IN,d(ON)}$	Turn-on propagation delay	From INxH rising edge to 10% of OUTx		125		ns
$t_{IN,d(OFF)}$	Turn-off propagation delay	From INxL rising edge to 90% of OUTx		140		ns
<b>Protections</b>						
$T_{jSD}$	Thermal shutdown threshold			160		°C
$T_{jSD,Hyst}$	Thermal shutdown hysteresis			40		°C
$I_{OC}$	Overcurrent threshold	See <a href="#">Figure 10 on page 18</a> .		2		A

1. Based on characterization data on a limited number of samples, not tested during production.

## 4 Pin description

Figure 2. Pin connection (top view)



AM039891V1

1. The exposed pad must be connected to ground.

Table 6. Pin description

No.	Name	Type	Function
1	INUL	Logic input	Output U driving input (low side)
2	INUH	Logic input	Output U driving input (high side)
3	OUTU	Power output	Power bridge output U
5	NC		
6	VS	Supply	Device supply voltage
7, EPAD	GND	Ground	Device ground
8	OUTV	Power output	Power bridge output V
10	OUTW	Power output	Power bridge output W
11	INWL	Logic input	Output W driving input (low side)
12	INWH	Logic input	Output W driving input (high side)
13	EN\FAULT	Logic input\ open drain output	Logic input 5 V compliant with open drain output. This is the power stage enable (when low, the power stage is turned off) and is forced low through the integrated open-drain MOSFET when a failure occurs.

Table 6. Pin description (continued)

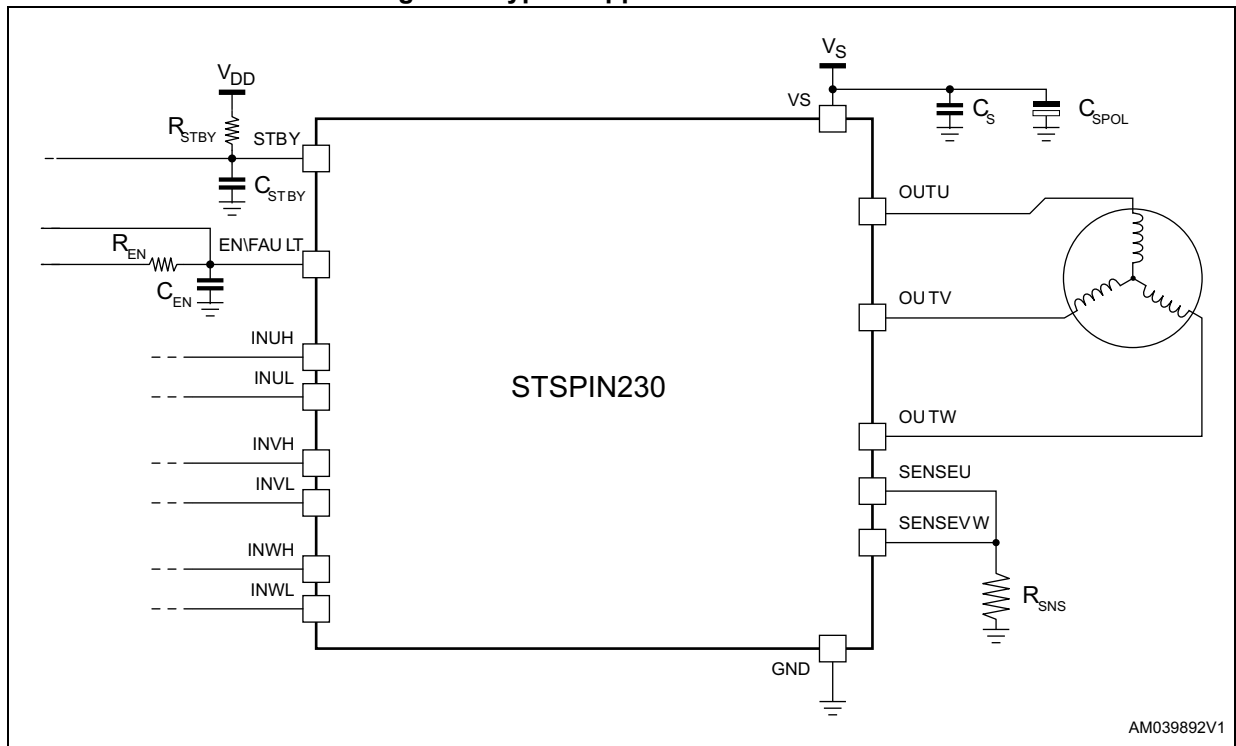
No.	Name	Type	Function
4	SENSEU	Power output	Sense output bridge U (must be connected to SENSEVW).
9	SENSEVW	Power output	Sense output bridge V and W (must be connected to SENSEU).
14	STBY\RESET	Logic input	Logic input 5 V compliant. When forced low, the device is forced into the low consumption mode.
15	INVL	Logic input	Output V driving input (low side).
16	INVH	Logic input	Output V driving input (high side).

# 5 Typical applications

Table 7. Typical application values

Name	Value
$C_S$	2.2 $\mu$ F / 16 V
$C_{SPOL}$	22 $\mu$ F / 16 V
$R_{SNS}$	330 m $\Omega$ / 1 W
$C_{EN}$	10 nF / 6.3 V
$R_{EN}$	18 k $\Omega$
$C_{STBY}$	1 nF / 6.3 V
$R_{STBY}$	18 k $\Omega$

Figure 3. Typical application schematic



AM039892V1

## 6 Functional description

The STSPIN230 device is a protected triple half-bridge motor driver.

### 6.1 Standby and power-up

The device provides a low consumption mode which is set forcing the STBY\RESET input below the  $V_{STBYL}$  threshold.

When the device is in standby status the power stage is disabled (outputs are in high impedance) and the supply to the integrated control circuitry is cut off. When the device leaves the standby status, all the control circuitry is reset to power-up condition.

### 6.2 Motor driving

The outputs of the three half-bridges are directly driven through the logic inputs as listed in [Table 8](#).

**Table 8. INxH and INxL**

ENFAULT	INxH	INxL	'x' half-bridge condition
0	X	X	High impedance
1	0	0	High impedance
1	0	1	Low side MOSFET ON
1	1	0	High side MOSFET ON
1	1	1	High impedance (interlocking)

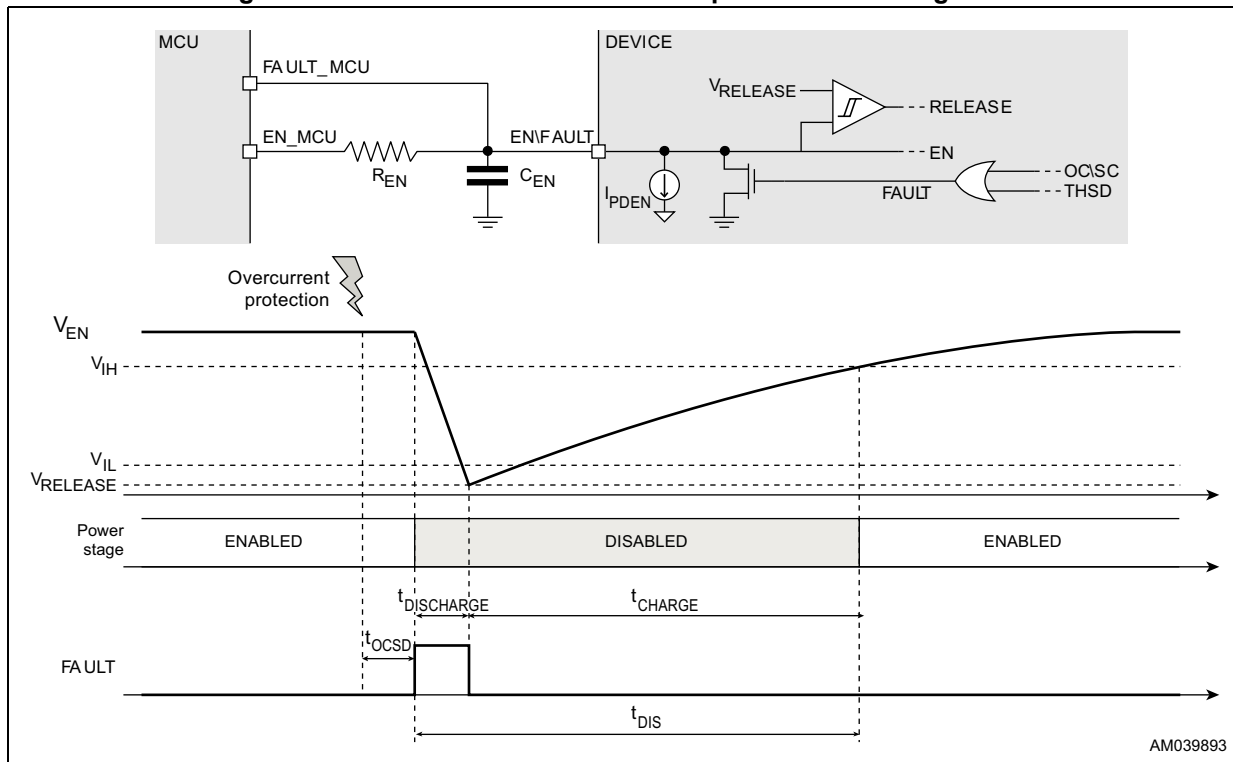
### 6.3 Overcurrent and short-circuit protection

The device embeds circuitry protecting each power output against the overload and short-circuit conditions (short to ground, short to VS and short between outputs).

When the overcurrent or the short-circuit protection is triggered the power stage is disabled and the EN\FAULT input is forced low through the integrated open-drain MOSFET discharging the external C<sub>EN</sub> capacitor (refer to [Figure 4](#)).

The power stage is kept disabled and the open-drain MOSFET is kept ON until the EN\FAULT input falls below the V<sub>RELEASE</sub> threshold, then the C<sub>EN</sub> capacitor is charged through the R<sub>EN</sub> resistor.

**Figure 4. Overcurrent and short-circuit protections management**



The total disable time after an overcurrent event can be set by properly sizing the external network connected to the EN\FAULT pin (refer to [Figure 4](#)):

**Equation 1**

$$t_{DIS} = t_{discharge} + t_{charge}$$

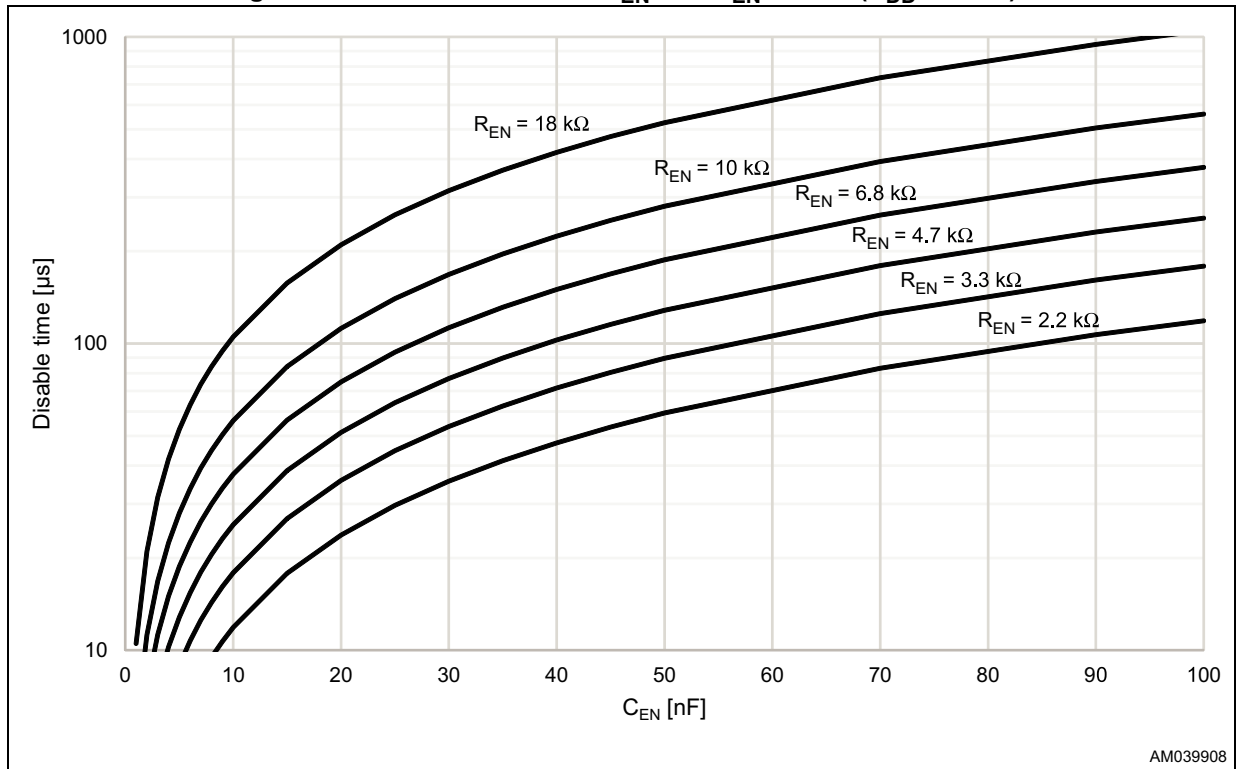
But t<sub>charge</sub> is normally much higher than t<sub>discharge</sub>, thus we can consider only the second one contribution:

**Equation 2**

$$t_{DIS} \cong R_{EN} \cdot C_{EN} \cdot \ln \frac{(V_{DD} - R_{EN} \cdot I_{PDEN}) - V_{RELEASE}}{(V_{DD} - R_{EN} \cdot I_{PDEN}) - V_{IH}}$$

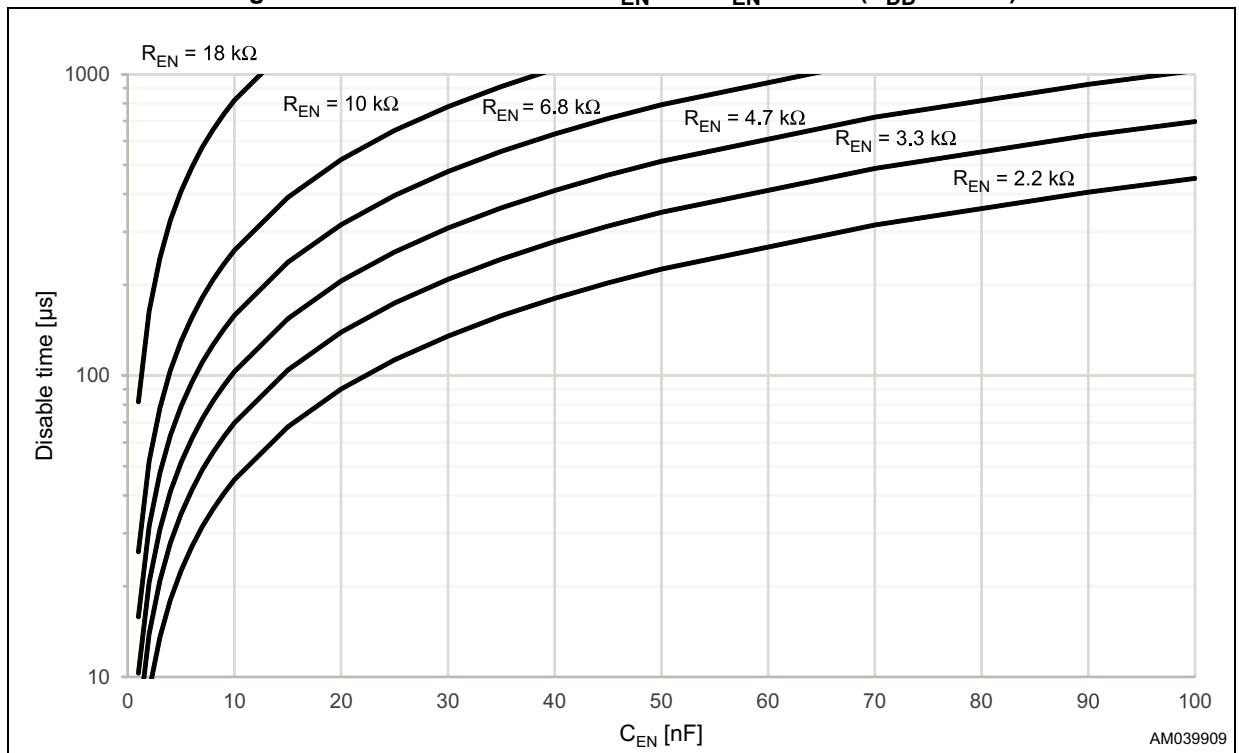
Where V<sub>DD</sub> is the pull-up voltage of the R<sub>EN</sub> resistor.

Figure 5. Disable time versus  $R_{EN}$  and  $C_{EN}$  values ( $V_{DD} = 3.3\text{ V}$ )



AM039908

Figure 6. Disable time versus  $R_{EN}$  and  $C_{EN}$  values ( $V_{DD} = 1.8\text{ V}$ )



AM039909



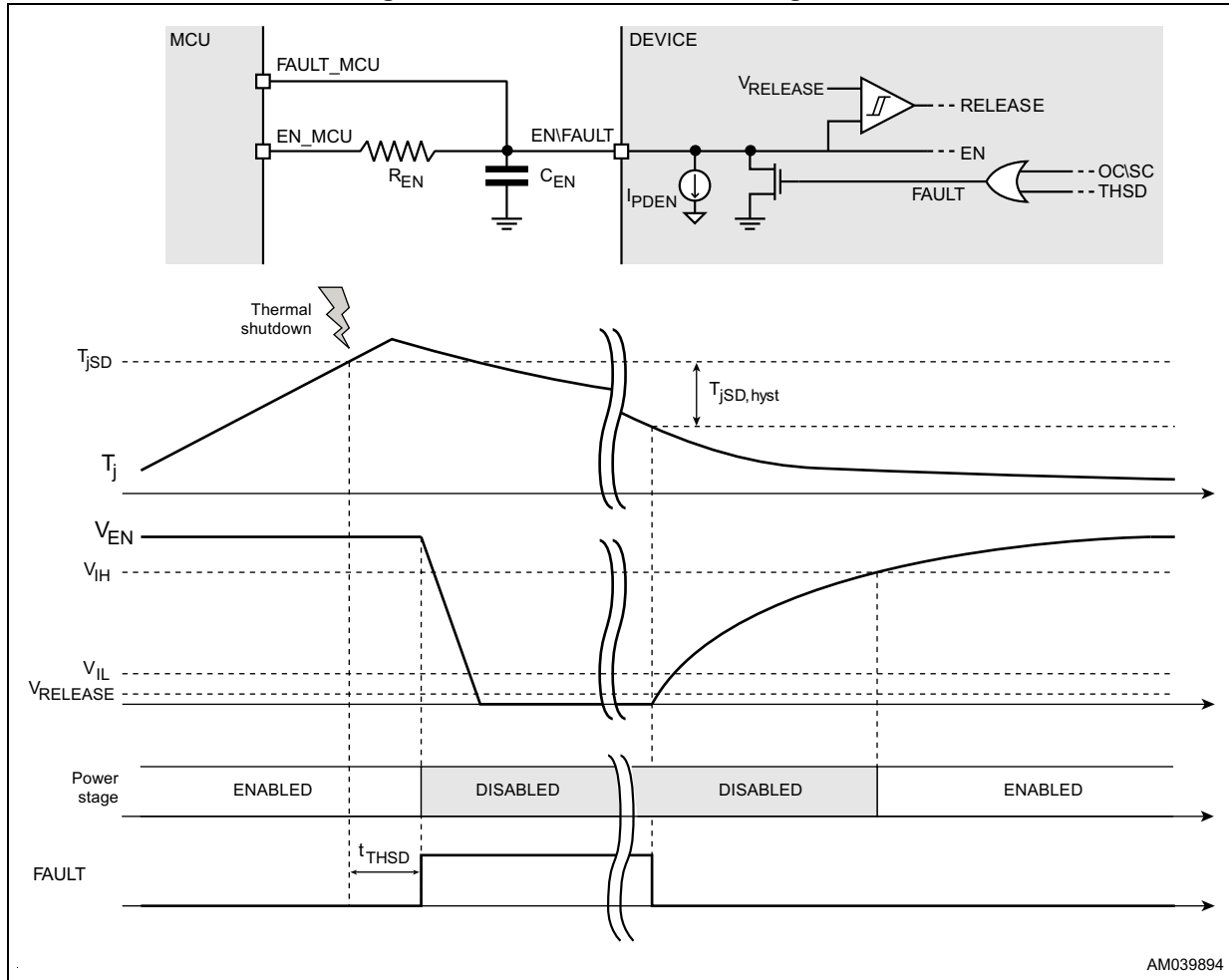
### 6.4 Thermal shutdown

The device embeds circuitry protecting it from the overtemperature condition.

When the thermal shutdown temperature is reached the power stage is disabled and the EN\FAULT input is forced low through the integrated open-drain MOSFET (refer to [Figure 7](#)).

The protection and the EN\FAULT output are released when the IC temperature returns below a safe operating value ( $T_{jSD} - T_{jSD,Hyst}$ ).

Figure 7. Thermal shutdown management



# 7 Graphs

Figure 8. Power stage resistance versus supply voltage

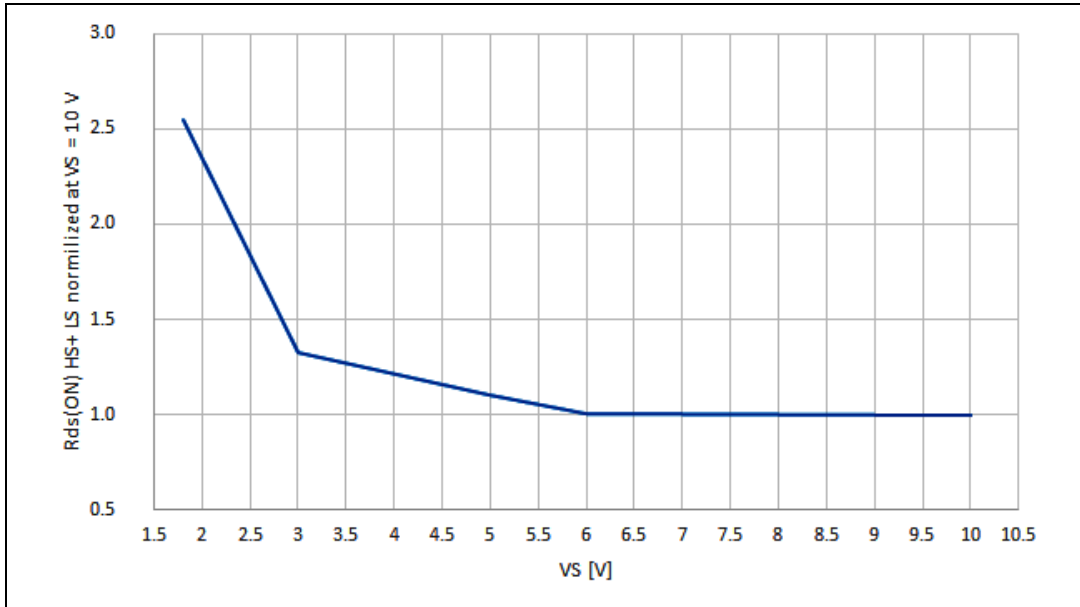
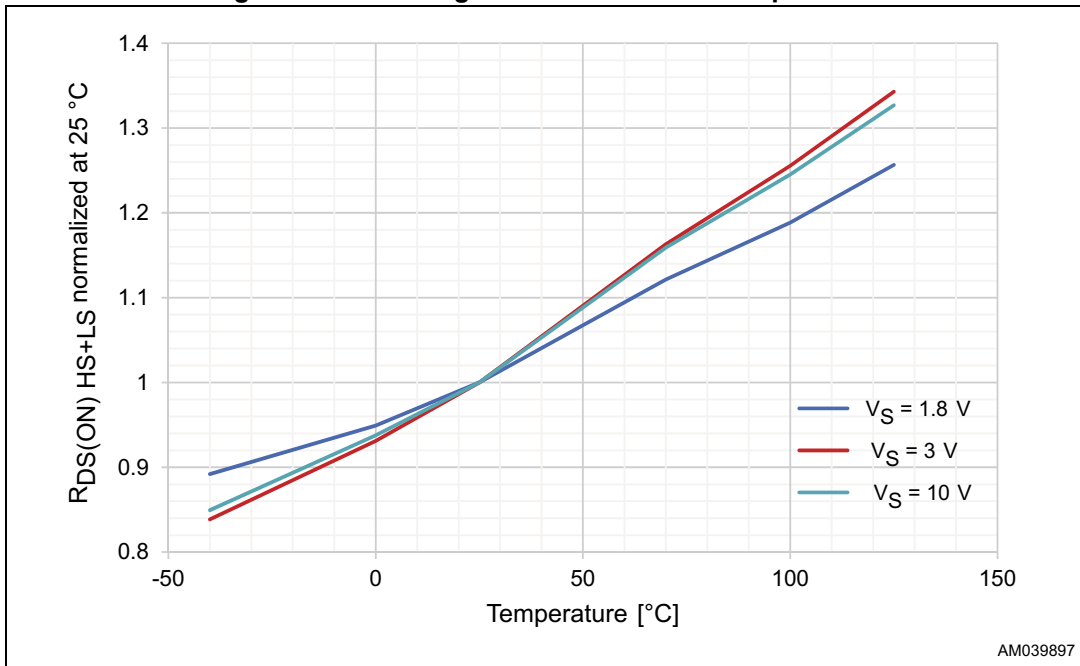
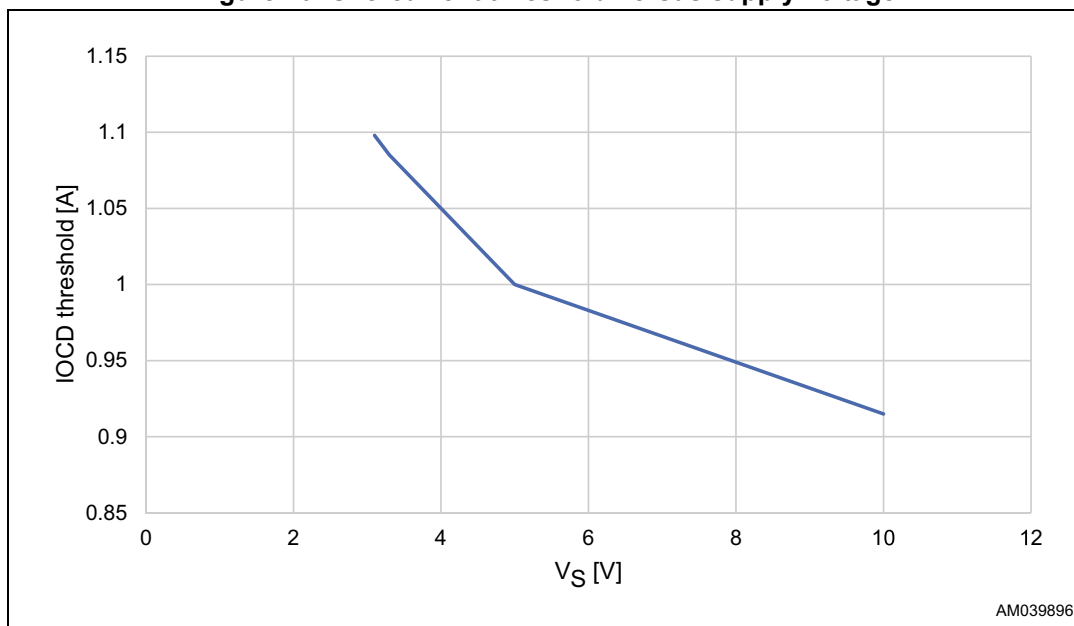


Figure 9. Power stage resistance versus temperature



AM039897

Figure 10. Overcurrent threshold versus supply voltage



## 8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 8.1 VFQFPN 3x3x1.0 16L package information

Figure 11. VFQFPN 3x3x1.0 16L package outline

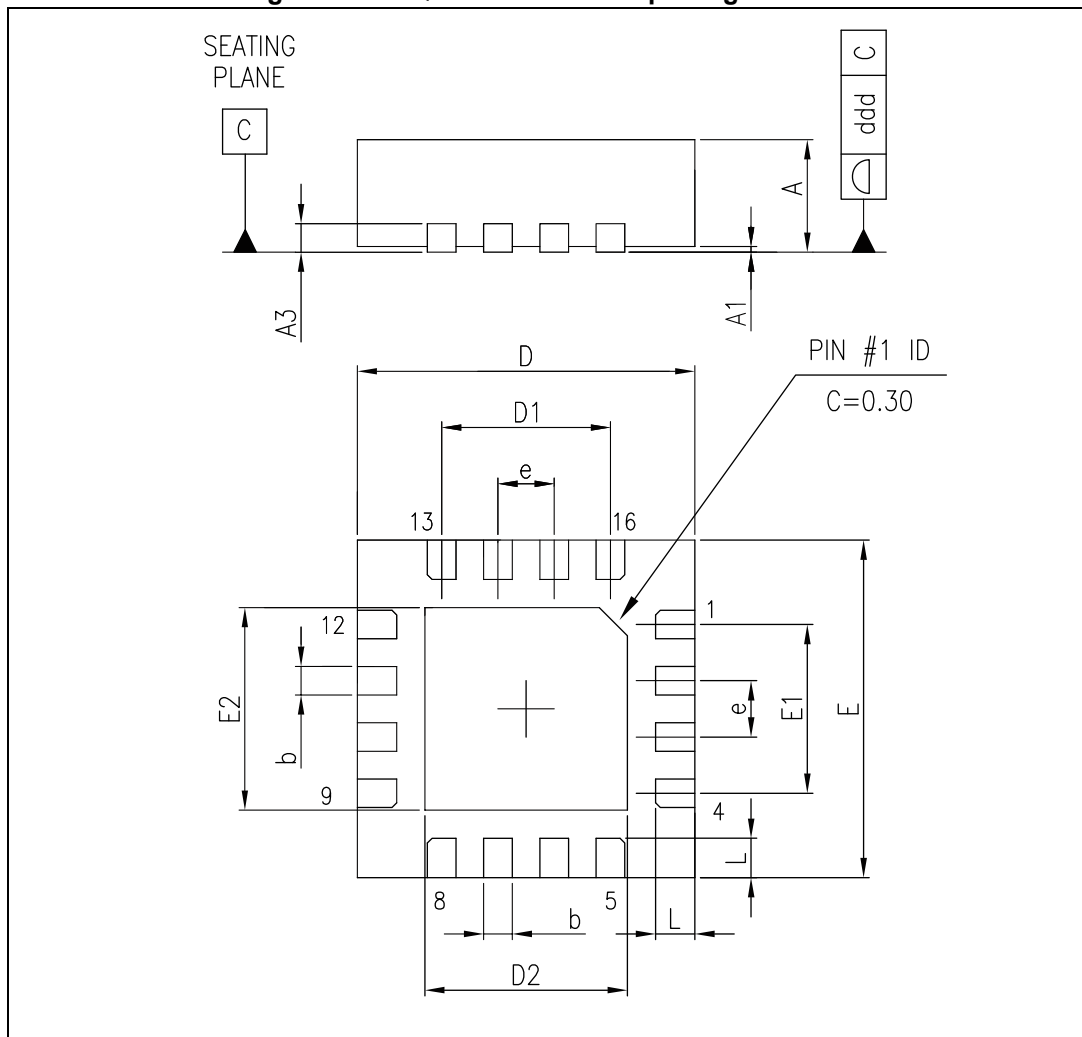
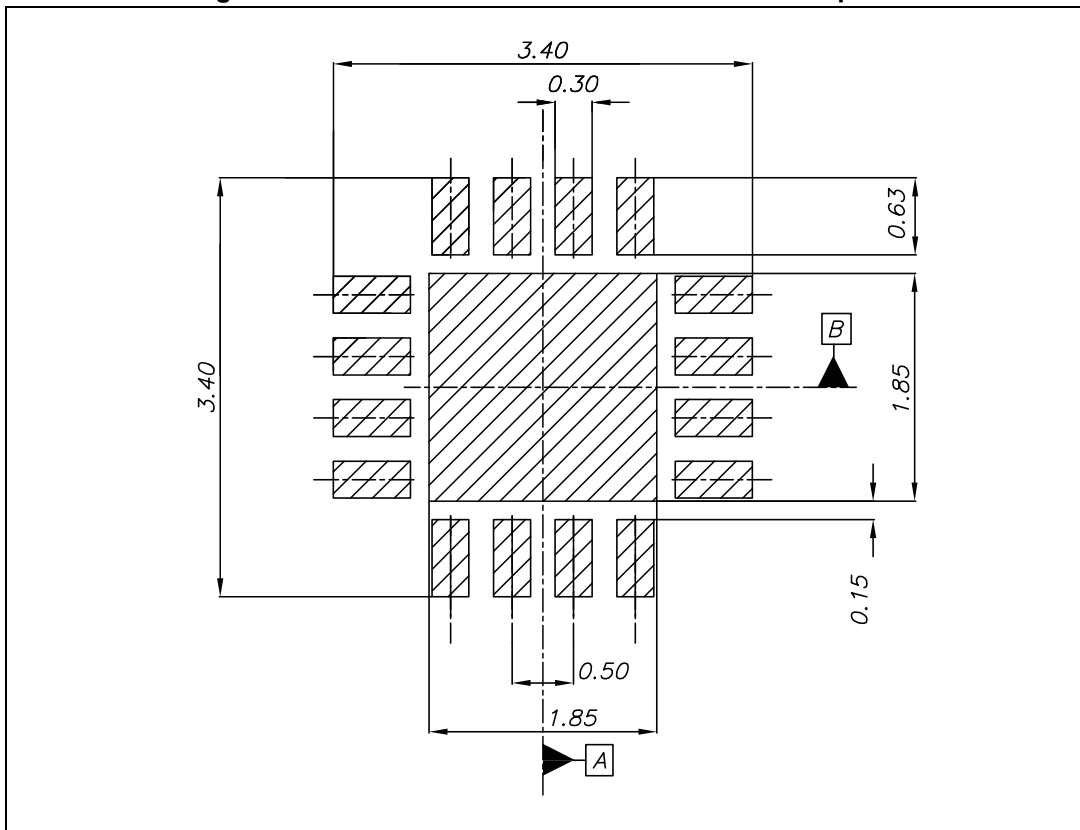


Table 9. VFQFPN 3x3x1.0 16L package mechanical data

Symbol	Dimensions (mm)			NOTES
	Min.	Typ.	Max.	
A	0.80	0.90	1.00	(1)
A1		0.02		
A3		0.20		
b	0.18	0.25	0.30	
D	2.85	3.00	3.15	
D2	1.70	1.80	1.90	
E	2.85	3.00	3.15	
E2	1.70	1.80	1.90	
e		0.50		
L	0.45	0.50	0.55	

- VFQFPN stands for "Thermally Enhanced Very thin Fine pitch Quad Packages No lead".  
 Very thin:  $0.80 < A \leq 1.00$  mm / fine pitch:  $e < 1.00$  mm.  
 The pin #1 identifier must be present on the top surface of the package by using an indentation mark or an other feature of the package body.

Figure 12. VFQFPN 3x3x1.0 16L recommended footprint



## 9 Ordering information

Table 10. Device summary

Order code	Package	Packaging
STSPIN230	VFQFPN 3x3x1.0 16L	Tape and reel

## 10 Revision history

Table 11. Document revision history

Date	Revision	Changes
06-May-2016	1	Initial release.
30-Jun-2016	2	Updated document status to <i>Datasheet - production data</i> on page 1. Updated <i>Table 1 on page 6</i> (changed Max. value of $V_S$ from 12 to 11).
19-Oct-2016	3	Updated main title <i>on page 1</i> (added "for BLDC motors"). Updated <i>Section : Features on page 1</i> (added "Interlocking function"). Updated <i>Figure 1 on page 5</i> , <i>Figure 3 on page 12</i> , and <i>Figure 8 on page 17</i> (replaced by new figures). Updated <i>Table 3 on page 6</i> (replaced by new table). Updated <i>Figure 2 on page 10</i> (replaced "SENSE" by "SENSEU" and "SENSEVW"). Updated <i>Table 6 on page 10</i> (updated pin 4 and 9). Minor modifications throughout document.
04-Nov-2016	4	Updated <i>Table 2 on page 6</i> (added $t_{INW}$ symbol).

**IMPORTANT NOTICE – PLEASE READ CAREFULLY**

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2016 STMicroelectronics – All rights reserved