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STSPIN32F0A

Advanced BLDC controller with embedded STM32 MCU

Datasheet - production data

Features

- Extended operating voltage from 6.7 to 45 V
- Three-phase gate drivers
  - 600 mA sink/source
  - Integrated bootstrap diodes
  - Cross-conduction prevention
- 32-bit ARM® Cortex®-M0 core:
  - Up to 48 MHz clock frequency
  - 4-kByte SRAM with HW parity
  - 32-kByte Flash memory with option bytes used for write/readout protection
  - Availability FW bootloader
- 3.3. V DC/DC buck converter regulator with overcurrent, short-circuit, and thermal protection
- 12 V LDO linear regulator with thermal protection
- 16 general-purpose I/O ports (GPIO)
- 5 general-purpose timers
- 12-bit ADC converter (up to 9 channels)
- I^2C, USART and SPI interfaces
- 3 rail-to-rail operation amplifiers for signal conditioning
- Comparator for overcurrent protection with programmable threshold
- Standby mode for low power consumption
- UVLO protection on each power supply:
  - V_M, V_{DD}, V_{REG} and V_{BOOTx}
- On-chip debug support via SWD
- Extended temperature range: -40 to +125 °C

Applications

- Smart manufacturing equipment
- Power tools, FANs and pumps
- Home appliances: vacuum cleaners, hand/hair dryers, air purifiers and coffee machines
- High-tech applications such as: drones, gimbals, educational/home robots

Contents

List of tables

List of figures

1 Description

The STSPIN32F0A is a System-In-Package providing an integrated solution suitable for driving three-phase BLDC motors using different driving modes.

It embeds a triple half-bridge gate driver able to drive power MOSFETs with a current capability of 600 mA (sink and source). The high- and low-side switches of same half-bridge cannot be simultaneously driven high thanks to an integrated interlocking function.

An internal DC/DC buck converter provides the 3.3 V voltage suitable to supply both the MCU and external components. An internal LDO linear regulator provides the supply voltage for gate drivers.

The integrated operational amplifiers are available for the signal conditioning, e.g. the current sensing across the shunt resistors.

A comparator with a programmable threshold is integrated to perform the overcurrent protection.

The integrated MCU (STM32F031C6 with extended temperature range, suffix 7 version) allows performing field-oriented control, the 6-step sensorless and other advanced driving algorithms. It has the write-protection and read-protection feature for the embedded Flash memory to protect against unwanted writing and/or reading. It is possible to download the firmware on-the-field through the serial interface thanks to the embedded bootloader.

The STSPIN32F0A device also features overtemperature and undervoltage lockout protections and can be put in the standby mode to reduce the power consumption. The device provides 16 general-purpose I/O ports (GPIO) with the 5 V tolerant capability, one 12-bit analog-to-digital converter with up to 9 channels performing conversions in a single-shot or scan modes, 5 synchronizable general-purpose timers and supports an easy to use debugging serial interface (SWD).

2 Block diagrams

Figure 1: STSPIN32F0A System-In-Package block diagram

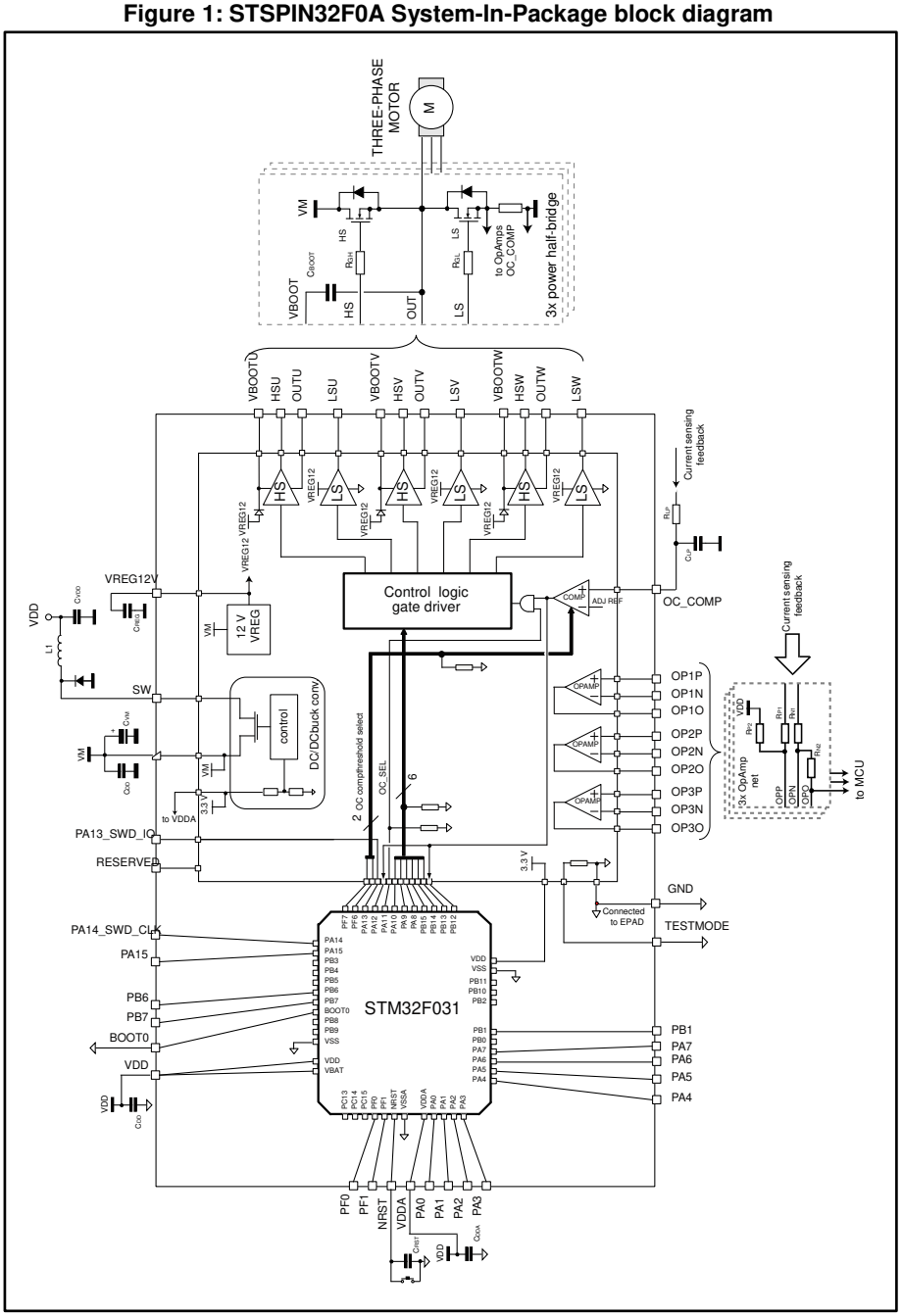
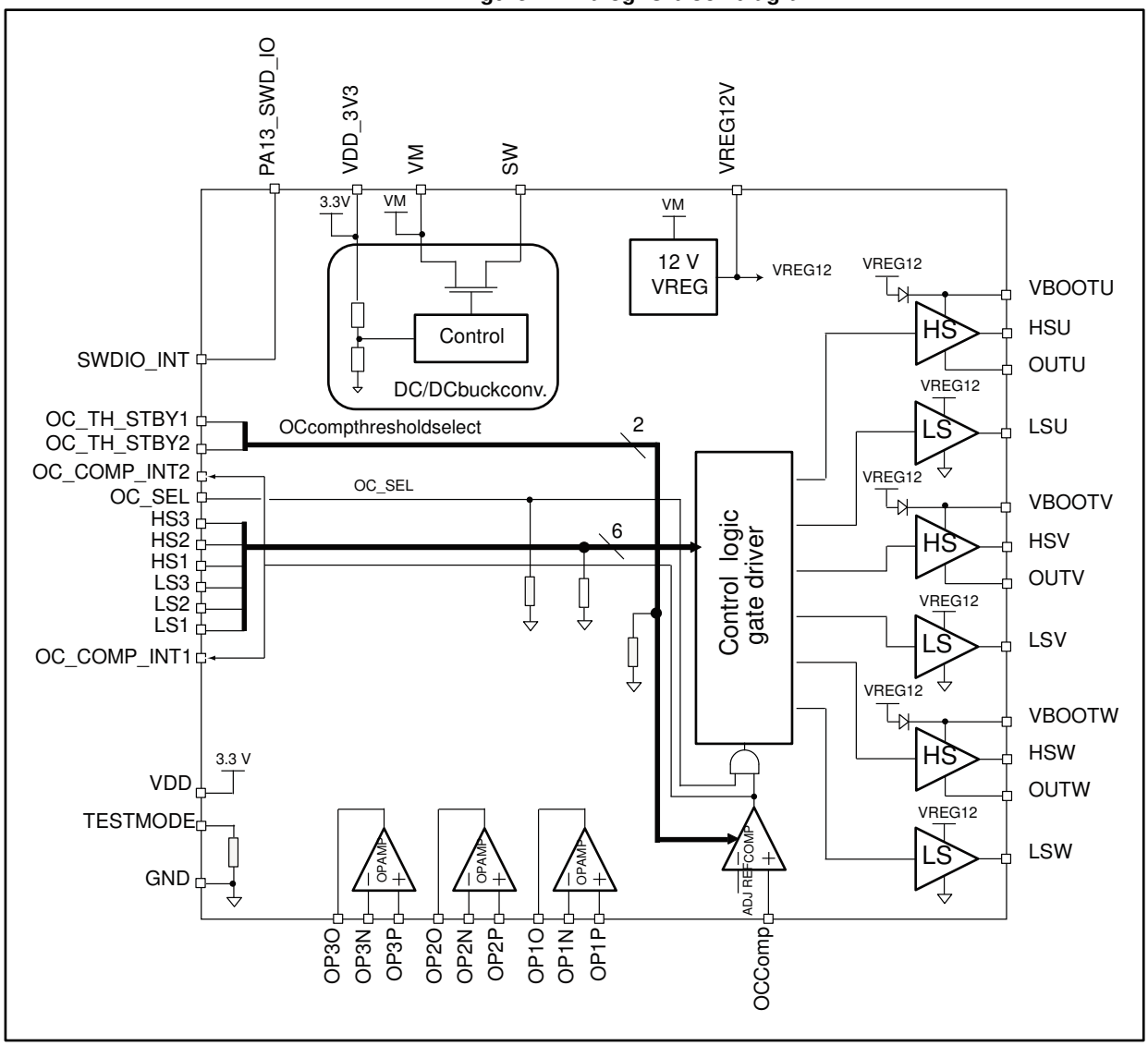


Figure 2: Analog IC block diagram



3 Electrical data

3.1 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 1: "Absolute maximum ratings"* may cause permanent damage to the device. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 1: Absolute maximum ratings

Symbol	Parameter	Test condition	Value	Unit
V_M	Power supply voltage	-	-0.3 to 48	V
V_{REG12}	Linear regulator output and gate driver supply voltage	VREG12 shorted to VM	15	V
V_{OPP}	Op amp positive input voltage	-	-0.2 to V_{DD} + 0.2	V
V_{OPN}	Op amp negative input voltage	-	-0.2 to V_{DD} + 0.2	V
V_{CP}	Comparator input voltage	-	-2 to 2	V
V_{HS}	High-side gate output voltage	-	V_{OUT} - 0.3 to V_{BOOT} + 0.3	V
V_{LS}	Low-side gate output voltage	-	-0.3 to V_{REG12} + 0.3	V
V_{BOOT}	Bootstrap voltage	-	Max. (V_{OUT} - 0.3 or -0.3) to min. ('V_{OUT} + V_{REG12} + 0.3' or 60)	V
V_{OUT}	Output voltage (OUTU, OUTV, OUTW)	-	-2 to V_M + 2	V
dV_{OUT}/dt	Output slew rate	-	± 10	V/ns
V_{IO}	MCU logic input voltage(1)	TTa type (1)	-0.3 to 4	V
		(1) FT, FTf type	-0.3 to V_{DD} + 4 (2)	
		BOOT0	0 to 9.0	
I_{IO}	MCU I/O output current	(1)	-25 to 25	mA
ΣI_{IO}	MCU I/O total output current	(1), (3)	-80 to 80	mA
V_{DD}	MCU digital supply voltage	(1)	-0.3 to 4	V
V_{DDA}	MCU analog supply voltage	(1)	-0.3 to 4	V
T_{stg}	Storage temperature	-	-55 to 150	°C
T_j	Operating junction temperature	-	-40 to 150	°C

Notes:

(1)See Table 15 Voltage characteristics in the STM32F031C6 datasheet (suffix 7 version).

(2)Valid only if the internal pull-up/pull-down resistors are disabled. If internal the pull-up or pull-down resistor is enabled, the maximum limit is 4 V.

(3)If the MCU supply voltage is provided by an integrated DC/DC regulator, the application current consumption is limited at $I_{DDA,max}$ value (see *Table 5: "Electrical characteristics"*).

3.2 ESD protections

Table 2: ESD protection ratings

Symbol	Parameter	Test condition	Class	Value	Unit
HBM	Human body model	Conforming to ANSI/ESDA/JEDEC JS-001-2014	H2	2	kV
CDM	Charge device model	Conforming to ANSI/ESDA/JEDEC JS-002-2014	C2	750	V

3.3 Recommended operating conditions

Table 3: Recommended operating conditions

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_M	Power supply voltage	-	6.7 (1)	-	45	V
dV_M/dt	Power supply voltage slope	V_M = 45 V	-	-	0.75	V/µs
V_{DDA}	DC/DC regulator output voltage	-	-	3.3	-	V
L_{SW}	Output inductance	-	-	22	-	µH
C_{DDA}	Output capacitance	-	47	-	-	µF
ESR_{DDA}	Output capacitor ESR	-	-	-	200	mΩ
V_{REG12}	Linear regulator output and gate driver supply voltage	13 < V_M < 45 V	-	12	-	V
		Shorted to VM	6.7(1)	-	15	
C_{REG}	Load capacitance	-	1	10	-	µF
ESR_{REG}	ESR load capacitance	-	-	-	1.2	Ω
V_{BO}	Floating supply voltage (2)	-	-	V_{REG12} - 1	15	V
V_{CP}	Comparator input voltage	-	0	-	1	V
T_j	Operating junction temperature	Analog IC	-40	-	125	°C
		MCU (3)	-40	-	125	°C

Notes:

(1) UVLO threshold V_{MOn_max}.

(2) $V_{BO} = V_{BOOT} - V_{OUT}$.

(3) See the STM32F031C6 datasheet (suffix 7 version).

3.4 Thermal data

Thermal values are calculated by simulation with the following boundary conditions: 2s2p board as per the std. JEDEC (JESD51-7) in natural convection, board dimensions: 114.3 x 76.2 x 1.6 mm, ambient temperature: 25 °C.

Table 4: Thermal data

Symbol	Parameter	Value	Unit
$R_{th\ (JA)}$	Thermal resistance junction to ambient	45.6	°C/W

4 Electrical characteristics

Testing conditions: V_M = 15 V; V_{DD} = 3.3 V, unless otherwise specified.

Typical values are tested at T_j = 25 °C, minimum and maximum values are guaranteed by thermal characterization in the temperature range of -40 to 125 °C, unless otherwise specified.

Table 5: Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Power supply and standby mode						
I_M	V_M current consumption	V_M = 45 V; V_{DD} = 3.5 V externally supplied	-	2	2.6	mA
		Standby PF7 = '0' PF6 = '0 V_M = 45 V; V_{DD} = 3.5 V externally supplied	-	880	1100	µA
V_{MOn}	V_M UVLO turn-on threshold	V_M rising from 0 V	6.0	6.3	6.6	V
V_{MOff}	V_M UVLO turn-off threshold	V_M falling from 8 V	5.8	7.1	6.4	V
V_{MHys}	V_M UVLO threshold hysteresis	-	-	0.2	-	V
I_{DD}	V_{DD} current consumption	V_{DD} = 3.5 V externally supplied (1)	-	2.5	5	mA
		Standby PF7 = '0' PF6 = '0' V_{DD} = 3.5 V externally supplied(1)	-	2.5	5	
I_{DDA}	V_{DDA} current consumption	V_{DD} = 3.5 V externally supplied(1)	-	400	550	µA
		Standby PF7 = '0' PF6 = '0' V_{DD} = 3.5 V externally supplied(1)	-	80	125	
V_{DDOn}	V_{DD} UVLO turn-on threshold	V_{DD} rising from 0 V	2.5	2.65	2.8	V
V_{DDOff}	V_{DD} UVLO turn-off threshold	V_{DD} falling from 3.3 V	2.2	2.35	2.5	V
V_{DDHys}	V_{DD} UVLO threshold hysteresis	-	-	0.3	-	V
I_{REG12}	V_{REG} current consumption	V_{REG} = 13 V externally supplied, V_M = 45 V; no commutation	-	800	1200	µA
		Standby PF7 = '0' PF6 = '0' V_{REG} = 13 V externally supplied	-	800	1200	
$V_{REG12On}$	V_{REG12} UVLO turn-on threshold	V_{REG12} rising from 0 V	6.0	6.3	6.6	V
$V_{REG12Off}$	V_{REG12} UVLO turn-off threshold	V_{REG12} falling from 8 V	5.8	6.1	6.4	V
$V_{REG12Hys}$	V_{REG12} UVLO threshold hysteresis	-	-	0.25	-	V
I_{BOOT}	V_{BO} current consumption	HS on V_{BO} = 13 V	-	200	290	µA
V_{BOOn}	V_{BO} UVLO turn-on threshold	V_{BO} rising from 0 V	5.5	5.8	6.1	V
V_{BOOff}	V_{BO}UVLO turn-off threshold	V_{BO} falling from 8 V	5.3	5.6	5.9	V

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{BOHys}	V_{BO} UVLO threshold hysteresis	-	-	0.15	-	V
t_{sleep}	Standby set time	-	-	-	1	µs
DC/DC switching regulator						
V_{PWR_OK}	Power good voltage	-	5.6	6	6.4	V
V_{DDA}	Average output voltage	(2)	3.09	3.3	3.5	V
I_{DDA}	Output current	DC; MCU current consumption included	-	-	70	mA
f_{SW}	Maximum SW switching frequency	Open loop, V_{DDA} floating I_{SW} = 100 mA	-	200	330	kHz
$R_{SWDS(ON)}$	Switch ON resistance	I_{SW} = 200 mA	-	1.4	-	Ω
η	Efficiency	V_M = 8 V; I_{DDA} = $I_{DDA,max}$ (2)	-	80	-	%
$I_{SW,peak}$	Peak current threshold	-	-	320	-	mA
I_{OVC}	Latched overcurrent threshold	-	-	1	-	A
t_{SS}	Soft-start time	-	2.5	5	7.5	ms
Linear regulator						
V_{REG12}	Linear regulator output and gate driver supply voltage	V_M = 13 ÷ 45 V (3) I_O = 10 mA	11.4	12	12.6	V
$V_{REG12,drop}$	Drop voltage	V_M = 8 ÷ 11 V, I_O = 10 mA	-	200	400	mV
$I_{REG12,lim}$	Linear regulator current limit	V_M = 13 V	20	-	40	mA
Gate drivers						
I_{SI} I_{SO}	Maximum sink/source current capabilities	T_J = 25 °C	400	600	-	mA
		Full temperature range	350	-	-	mA
R_{PDin}	Input lines pull-down resistor	-	30	60	95	kΩ
t_{on} t_{off}	Input-to-output propagation delay (4)	-	-	20	40	ns
MT	Delay matching, HS and LS turn-on/off (5)	-	-	10	20	ns
R_{DS_diode}	Bootstrap diode ON resistance	-	-	120	240	Ω
Operational amplifiers						
V_{icm}	Input common mode voltage range	-	-0.1	-	V_{DD} + 0.1	V
V_{OPio}	Input offset voltage	V_{out} = 1.65; T_j = 25 °C	-	1	6	mV
		V_{out} = 1.65; full temp. range	-	-	7	mV
I_{OPio}	Input offset current	V_{out} = 1.65 (6)	-	-	100	pA
I_{OPib}	Input bias current	(6)	-	-	100	pA
CMRR	Common mode rejection ratio	0 to 3.3 V; V_{out} = 1.65 V	70	90	-	dB

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
A_{OL}	Open loop gain	R_L = 10 kΩ; V_{out} = 1.65	-	90	-	dB
V_{DD} - V_{OH}	High level output voltage	R_L = 10 kΩ (7)	-	15	40	mV
V_{OL}	Low level output voltage	R_L = 10 kΩ(7)	-	15	40	mV
I_{OUT}	Sink output current	V_{out} = 3.3 V; T_j = 25 °C	18	-	-	mA
		V_{out} = 3.3 V; full temp. range	16	-	-	
	Source output current	V_{out} = 0 V; T_j = 25 °C	18	-	-	mA
		V_{out} = 0 V; full temp. range	16	-	-	
GBP	Gain bandwidth product	R_L = 2 kΩ; C_L = 100 pF V_{out} = 1.65	10	18	-	MHz
Gain	Minimum gain for stability	Phase margin = 45° 0.2 V < V_{out} < V_{DD} - 0.2	-	4	-	V/V
SR	Slew rate	R_L = 2 kΩ; C_L = 100 pF V_{in} 1 to 2 V step	-	10	-	V/µs
OC comparator						
OC_{th}	Overcurrent threshold	PF6 = '0' PF7 = '1'	90	-	120	mV
		PF6 = '1' PF7 =' 0'	235	255	275	mV
		PF6 = '1' PF7 = '1'	465	505	545	mV
t_{CPD}	Comparator propagation delay	OC_{th} = 0.5 V; OC_Comp: voltage step from 0 to 1 V	-	80	120	ns
$t_{OCdeglitch}$	Comparator input deglitch filter time	(8)	35	50	-	ns
$t_{OCrelease}$	Minimum overcurrent latch release pulse width	(8)	-	-	20	ns
Thermal protection						
T_{SD}	Thermal shut-down temperature	-	130	140	150	°C
T_{hys}	Thermal shut-down hysteresis	-	20	30	40	°C

Notes:

(1)The current consumption depends on the firmware loaded in the microcontroller.

(2)Using the 47 µF capacitor (APXG250ARA470MF61G), 22 µH inductor (MLF1608C220KTA00), and diode 1N4448TR.

(3)With 11 < V_M < 13 V the linear output voltage can be VREG12 or 'VM-VREG12,drop' depending on the linear regulator is already turned-on or not.

(4)*Figure 3: "Gate drivers timing"*.

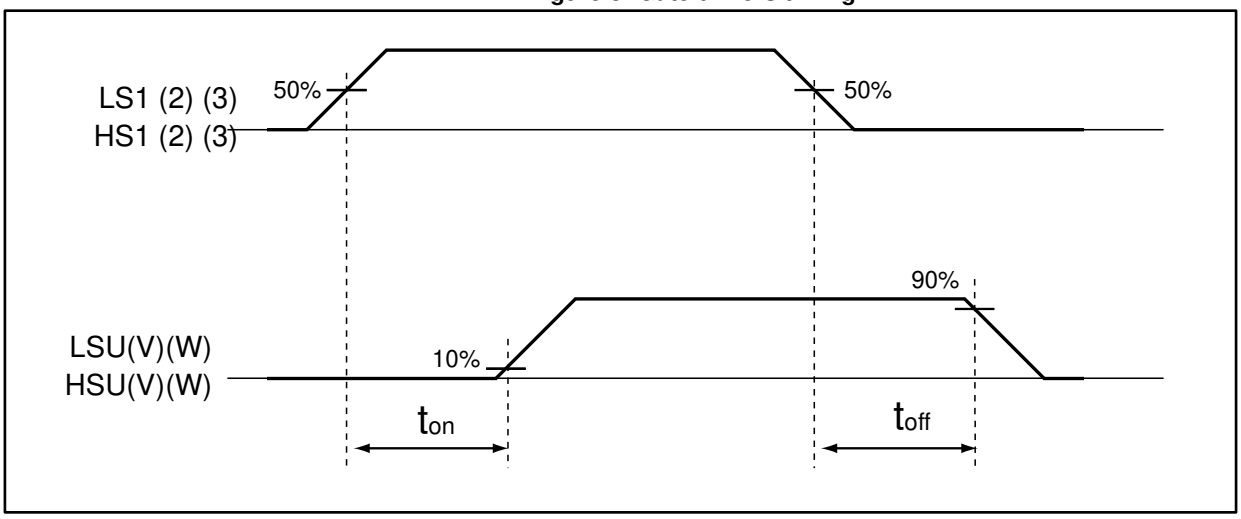
(5) MT = max. ($|t_{on(LVG)} - t_{off(LVG)}|$, $|t_{on(HVG)} - t_{off(HVG)}|$, $|t_{off(LVG)} - t_{on(HVG)}|$, $|t_{off(HVG)} - t_{on(LVG)}|$).

(6)Guaranteed by design.

(7)Guaranteed by I_{OUT} test.

(8) See *Figure 16: "Driver logic overcurrent management signals"*.

Figure 3: Gate drivers timing



5 Pin description

Figure 4: STSPIN32F0A SiP pin connection (top view)

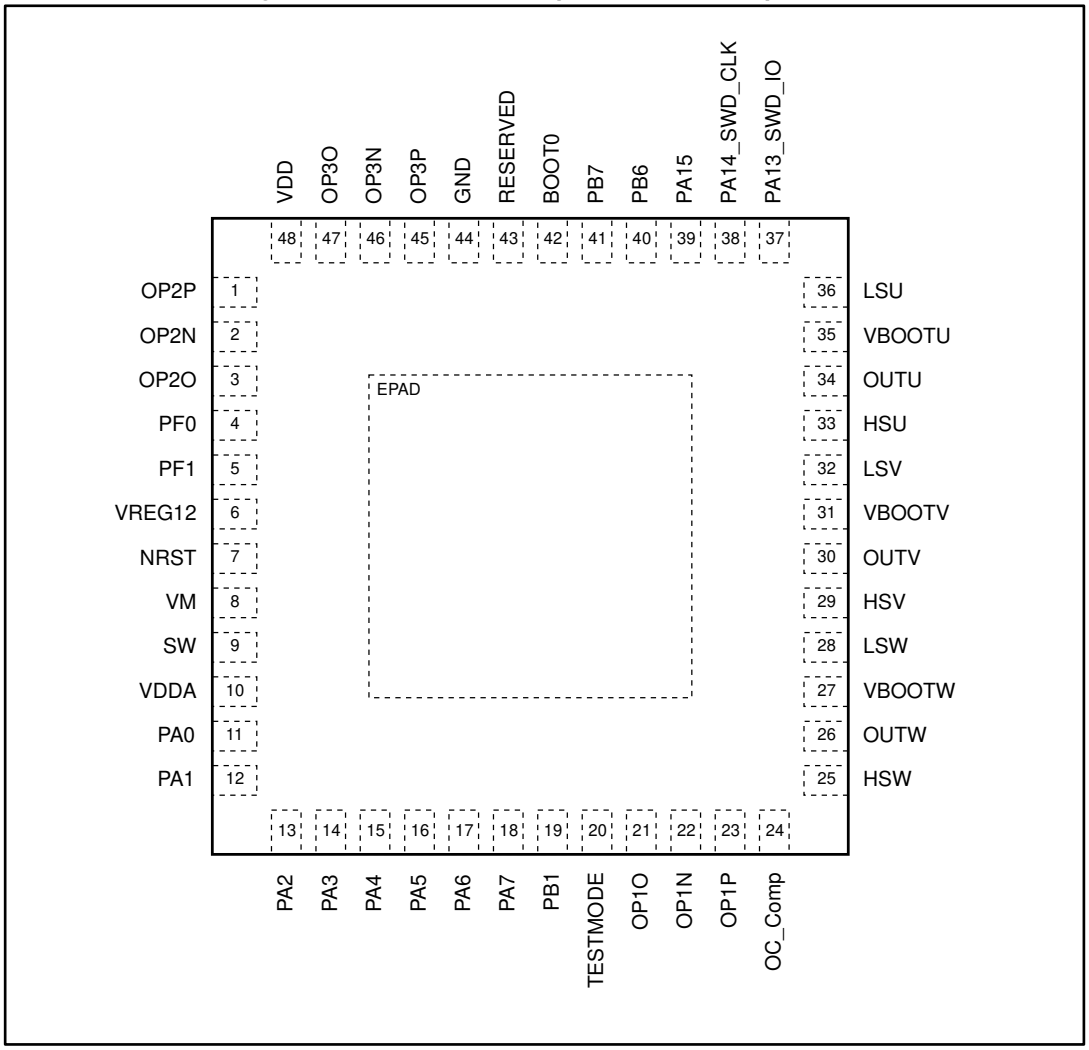


Table 6: STSPIN32F0A SiP pin description

No.	Name	Type	Function
1	OP2P	Analog in	Op amp 2 non-inverting input
2	OP2N	Analog in	Op amp 2 inverting input
3	OP2O	Analog out	Op amp 2 output
4	PF0	GPIO	MCU PF0
5	PF1	GPIO	MCU PF1
6	VREG12	Power	12 V linear regulator output
7	NRST	GPIO	MCU reset pin
8	VM	Power	Power supply voltage (bus voltage)
9	SW	Analog out	3.3 V DC/DC buck regulator switching node

No.	Name	Type	Function
10	VDDA	Power	MCU analog power supply voltage
11	PA0	GPIO	MCU PA0
12	PA1	GPIO	MCU PA1
13	PA2	GPIO	MCU PA2
14	PA3	GPIO	MCU PA3
15	PA4	GPIO	MCU PA4
16	PA5	GPIO	MCU PA5
17	PA6	GPIO	MCU PA6
18	PA7	GPIO	MCU PA7
19	PB1	GPIO	MCU PB1
20	TESTMODE	Digital In	Test mode input
21	OP1O	Analog out	Op amp 1 output
22	OP1N	Analog in	Op amp 1 inverting input
23	OP1P	Analog in	Op amp 1 non-inverting input
24	OC_COMP	Analog in	Overcurrent comparator input
25	HSW	Analog out	W phase high-side driver output
26	OUTW	Power	W phase high-side (floating) common voltage
27	VBOOTW	Power	W phase bootstrap supply voltage
28	LSW	Analog out	W phase low-side driver output
29	HSV	Analog out	V phase high-side driver output
30	OUTV	Power	V phase high-side (floating) common voltage
31	VBOOTV	Power	V phase bootstrap supply voltage
32	LSV	Analog out	V phase low-side driver output
33	HSU	Analog out	U phase high-side driver output
34	OUTU	Power	U phase high-side (floating) common voltage
35	VBOOTU	Power	U phase bootstrap supply voltage
36	LSU	Analog out	U phase low-side driver output
37	PA13_SWD_IO	GPIO	MCU PA13/SWDIO (system debug data via analog IC)
38	PA14_SWD_CLK	GPIO	MCU PA14/SWDCLK (system debug clock)
39	PA15	GPIO	MCU PA15
40	PB6	GPIO	MCU PB6
41	PB7	GPIO	MCU PB7
42	BOOT0	Digital in	MCU BOOT0
43	RESERVED	-	Reserved for test mode (can be left floating in application)
44	GND	Power	Ground
45	OP3P	Analog in	Op amp 3 non-inverting input
46	OP3N	Analog in	Op amp 3 inverting input

No.	Name	Type	Function
47	OP3O	Analog out	Op amp 3 output
48	VDD	Power	MCU digital power supply
	EPAD	Power	Internally connected to ground

Table 7: STSPIN32F0A MCU pad mapping

MCU pad	Type	Analog IC pad	Alternate and additional functions
PF0	I/O - FT	-	OSC_IN
PF1	I/O - FT	-	OSC_OUT
NRST	I/O - RST	-	Device reset input / internal reset output (active low)
VDDA	S	VDD_3V3	Analog power supply voltage
PA0	I/O - TTa	-	TIM2_CH1_ETR, USART1_CTS ADC_IN0, RTC_TAMP2, WKUP1
PA1	I/O - TTa	-	TIM2_CH2, EVENTOUT, USART1_RTS ADC_IN1
PA2	I/O - TTa	-	TIM2_CH3, USART1_TX ADC_IN2
PA3	I/O - TTa	-	TIM2_CH4, USART1_RX ADC_IN3
PA4	I/O - TTa	-	SPI1_NSS, I2S1_WS, TIM14_CH1, USART1_CK ADC_IN4
PA5	I/O - TTa	-	SPI1_SCK, I2S1_CK, TIM2_CH1_ETR ADC_IN5
PA6	I/O - TTa	-	SPI1_MISO, I2S1_MCK, TIM3_CH1, TIM1_BKIN, TIM16_CH1, EVENTOUT ADC_IN6
PB1	I/O - TTa	-	TIM3_CH4, TIM14_CH1, TIM1_CH3N ADC_IN9
PA7	I/O - TTa	-	SPI1_MOSI, I2S1_SD, TIM3_CH2, TIM14_CH1, TIM1_CH1N, TIM17_CH1, EVENTOUT ADC_IN7
PB12	I/O - FT	OC_COMP_INT	TIM1_BKIN (1)
PB13	I/O - FT	LS1	TIM1_CH1N(1)
PB14	I/O - FT	LS2	TIM1_CH2N(1)
PB15	I/O - FT	LS3	TIM1_CH3N(1)
PA8	I/O - FT	HS1	TIM1_CH1(1)

MCU pad	Type	Analog IC pad	Alternate and additional functions
PA9	I/O - FTf	HS2	TIM1_CH2(1)
PA10	I/O - FTf	HS3	TIM1_CH3
PA11	I/O - FT	OC_SEL	Push-pull output(1)
PA12	I/O - FT	OC_COMP_INT2	TIM1_ETR(1)
PA13_SWD_IO	I/O - FT	SWDIO_INT	IR_OUT, SWDIO
PF6	I/O - FTf	OC_TH_STBY2	Push-pull output(1)
PF7	I/O - FTf	OC_TH_STBY1	Push-pull output(1)
PA14_SWD_CLK	I/O - FT	-	USART1_TX, SWCLK
PA15	I/O - FT	-	SPI1_NSS, I2S1_WS, TIM2_CH_ETR, EVENTOUT, USART1_RX
PB6	I/O - FTf	-	I2C1_SCL, USART1_TX, TIM16_CH1N
PB7	I/O - FTf	-	I2C1_SDA, USART1_RX, TIM17_CH1N
VBAT, VDD	S	VDD	Backup and digital power supply
VSS, VSSA	S	-	Ground
BOOT0	I	-	Boot memory selection
PC13, PC14, PC15, PB0, PB2, PB10, PB11, PA15, PB3, PB4, PB5, PB8, PB9	-	-	Not connected

Notes:

(1)The analog IC is designed to support these GPIOs configuration only. Different configuration could cause device malfunctioning. The GPIO input configuration without pull-up or pull-down is always allowed.

Each unused GPIO inside the SiP should be configured in the OUTPUT mode low level after the startup by software.

Table 8: STSPIN32F0A analog IC pad description

Pinout name	Pad name	Type	Function
PA13_SWD_IO	SYS_SWDIO	Digital I/O	System debug data (connected to the output through the analog IC)
VDDA	VDD_3V3	Power	3.3 V DC/DC buck regulator voltage output
VM	VM	Power	Power supply voltage (bus voltage)
SW	SW	Analog out	3.3 V DC/DC buck regulator switching node
VREG12	VREG12	Power	12 V linear regulator output
VBOOTU	VBOOTU	Power	U phase bootstrap supply voltage

Pinout name	Pad name	Type	Function
HSU	HSU	Analog out	U phase high-side driver output
OUTU	OUTU	Power	U phase high-side (floating) common voltage
LSU	LSU	Analog out	U phase low-side driver output
VBOOTV	VBOOTV	Power	V phase bootstrap supply voltage
HSV	HSV	Analog out	V phase high-side driver output
OUTV	OUTV	Power	V phase high-side (floating) common voltage
LSV	LSV	Analog out	V phase low-side driver output
VBOOTW	VBOOTW	Power	W phase bootstrap supply voltage
HSW	HSW	Analog out	W phase high-side driver output
OUTW	OUTW	Power	W phase high-side (floating) common voltage
LSW	LSW	Analog out	W phase low-side driver output
OC_Comp	OC_COMP	Analog in	Overcurrent comparator input
OP1P	OP1P	Analog out	Op amp 1 output
OP1N	OP1N	Analog in	Op amp 1 inverting input
OP1O	OP1O	Analog in	Op amp 1 non-inverting input
OP2P	OP2P	Analog out	Op amp 2 output
OP2N	OP2N	Analog in	Op amp 2 inverting input
OP2O	OP2O	Analog in	Op amp 2 non-inverting input
OP3P	OP3P	Analog out	Op amp 3 output
OP3N	OP3N	Analog in	Op amp 3 inverting input
OP3O	OP3O	Analog in	Op amp 3 non-inverting input
RESERVED	RESERVED	Analog in	Reserved for test mode
GND	GND	Power	Ground
TESTMODE	TESTMODE	Digital in	Test mode input
-	VDD	Power	MCU digital power supply
-	OC_COMP_INT	Digital out	OC comparator output
-	HS1	Digital in	High-side input driver U
-	HS2	Digital in	High-side input driver V
-	HS3	Digital in	High-side input driver W
-	LS1	Digital in	Low-side input driver U
-	LS2	Digital in	Low-side input driver V

Pinout name	Pad name	Type	Function
-	LS3	Digital in	Low-side input driver W
-	OC_SEL	Digital in	OC protection selection
-	OC_COMP_INT2	Digital out	OC comparator output
-	SWD_IO_INT	Digital in	System debug data (connected to the output through the analog IC)
-	OC_TH_STBY1	Digital in	Overcurrent threshold selection and standby input 1
-	OC_TH_STBY2	Digital in	Overcurrent threshold selection and standby input 2

6 Device description

The STSPIN32F0A is a System-In-Package providing an integrated solution suitable for driving the three-phase BLDC motors. The device will be developed in the BCD8s (0.18 µm) technology.

6.1 UVLO and thermal protections

Table 9: "UVLO and OT protection management" summarizes the UVLO and OT protection management.

Table 9: UVLO and OT protection management

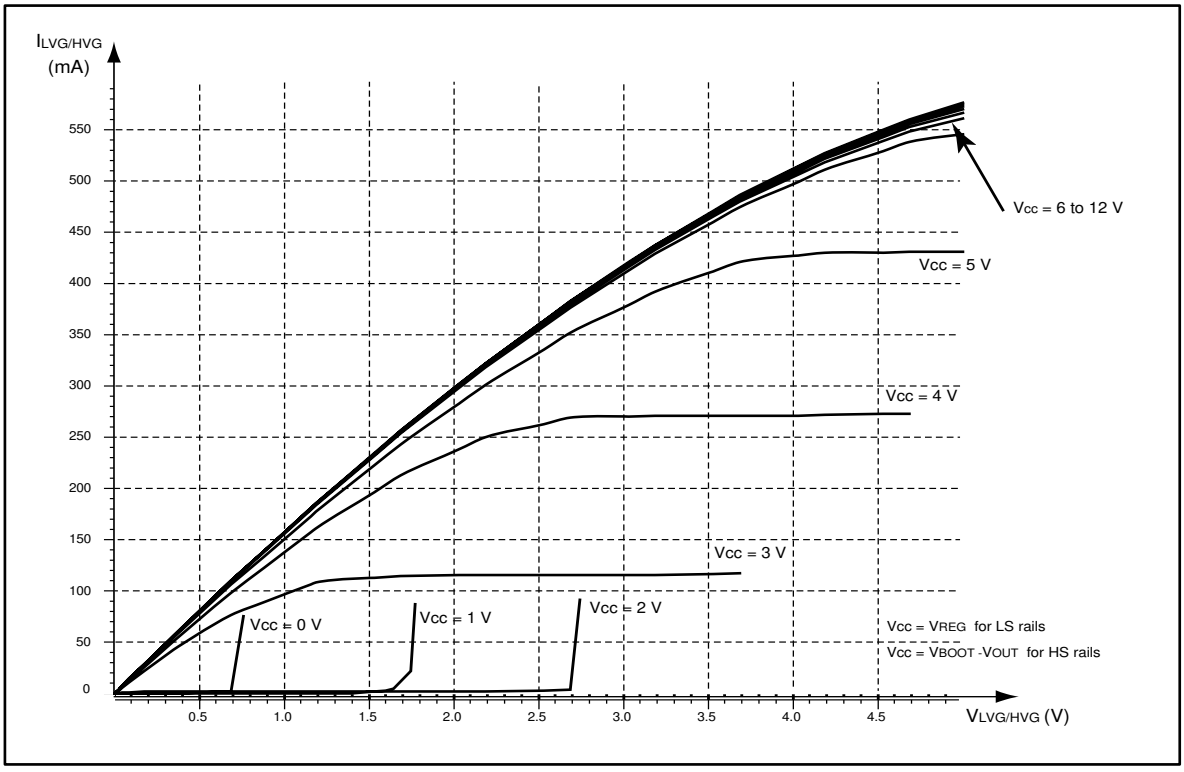
Block	V_M UVLO	V_{DD} UVLO	V_{REG12} UVLO	V_{BOOT} UVLO	Lin. Reg OT	DC/DC Reg OT
DC/DC regulator	-	-	-	-	-	OFF
Linear regulator	OFF	OFF	-	-	OFF	-
Op amps and OC comp	OFF	OFF	-	-	-	-
HSU, HSV, HSW output	LOW	LOW	LOW (1)	LOW(1), (2)	-	-
LSU, LSV, LSW output	LOW	LOW	LOW(1)	-	-	-

Notes:

(1)The N-channel of the gate driver is turned ON with all the available supply voltage, refer to *Figure 5: "Gate drivers' outputs characteristics in UVLO conditions"*.

(2)Only the high-side gate driver in which the UVLO condition is detected (e.g. UVLO on VBOOTU causes the HSU turning off).

Figure 5: Gate drivers' outputs characteristics in UVLO conditions



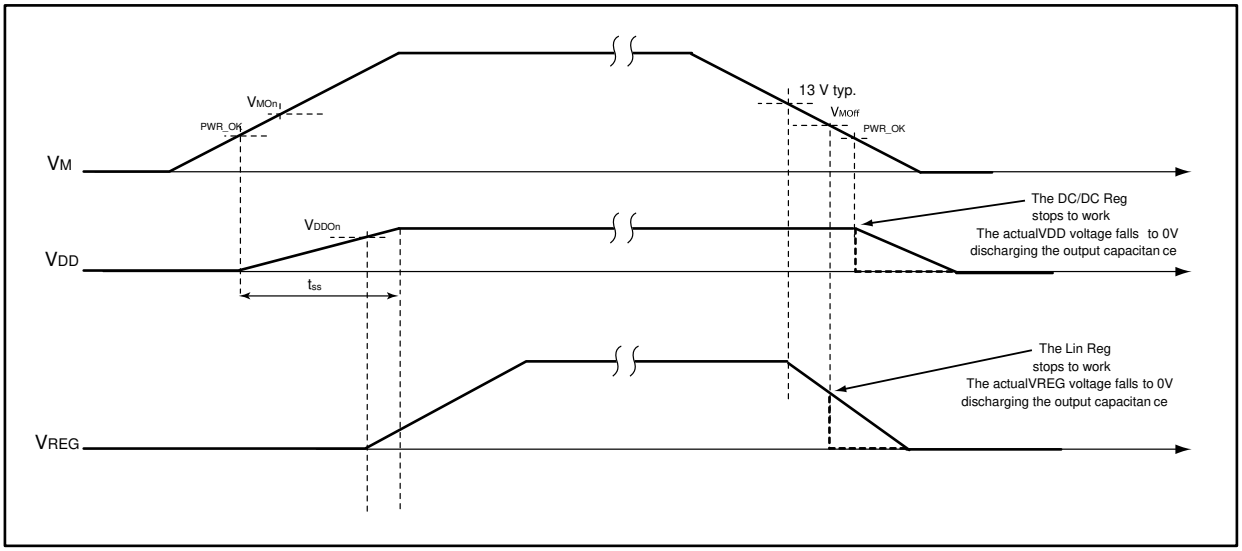
6.1.1 UVLO on supply voltages

The STSPIN32F0A device provides UVLO protections on all power supplies.

The device enters into the undervoltage condition when the power supply voltage falls below the off threshold voltage and expires when the motor supply voltage goes over the on threshold voltage.

Table 9: "UVLO and OT protection management" shows the UVLO protection management: which blocks are switched off after an UVLO event.

Figure 6: Power-up and power-down sequence



6.1.2 Thermal protection

The device embeds an overtemperature shut-down protection. The thermal sensors are placed next to the DC/DC and linear regulator blocks.

When the OT protection is triggered the correspondent block is switched off, the thermal shut-down condition only expires when the temperature goes below the "T_{SD} - T_{hys}" temperature (auto-restart).

Table 9: "UVLO and OT protection management" shows the thermal protection management which blocks are switched off after an overtemperature event.

6.2 DC/DC buck regulator

The internal DC/DC buck converter provides the 3.3 V supply voltage suitable to supply the MCU and other external devices.

The regulator operates in the discontinuous current mode (DCM).

A soft-start function with fixed start-up time is implemented to minimize the inrush current at the start-up, refer to *Figure 8: "Soft-start timing"*.

An overcurrent and short-circuit protection is provided.

If the failure event occurs on the SW pin and the I_{OVC} threshold is reached the regulator is latched off. To restart the DC/DC regulator a power-down and power-up cycle of device supply voltage (V_M) is mandatory.

If the failure event occurs on the regulator output (VDDA pin) and the voltage goes below the UVLO threshold (V_{DDOff}), the regulator restarts with a new soft-start sequence until the OC condition is removed. In this case the current in the coil is limited by $I_{SW.peak}$.

The DC/DC regulator embeds a thermal protection as described in *Section 6.1.2: "Thermal protection"*.

Figure 7: DC/DC buck regulator topology

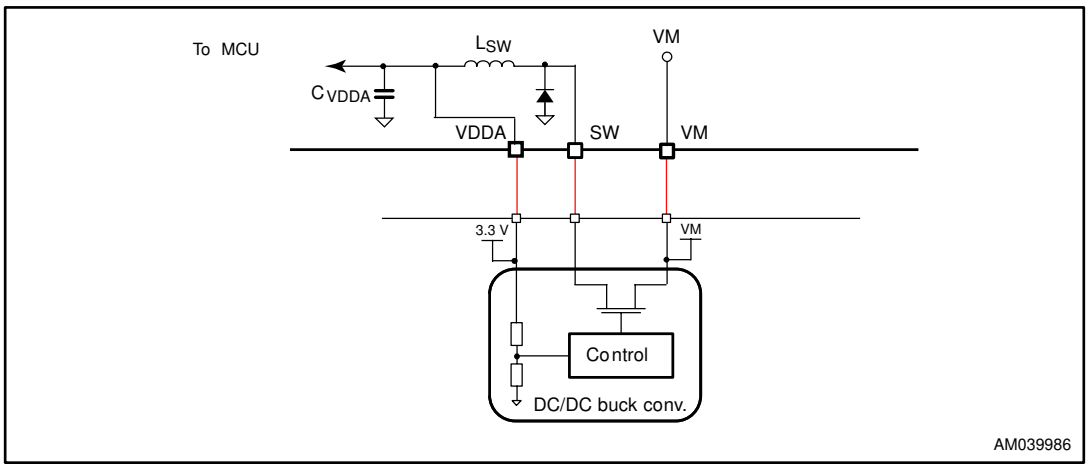
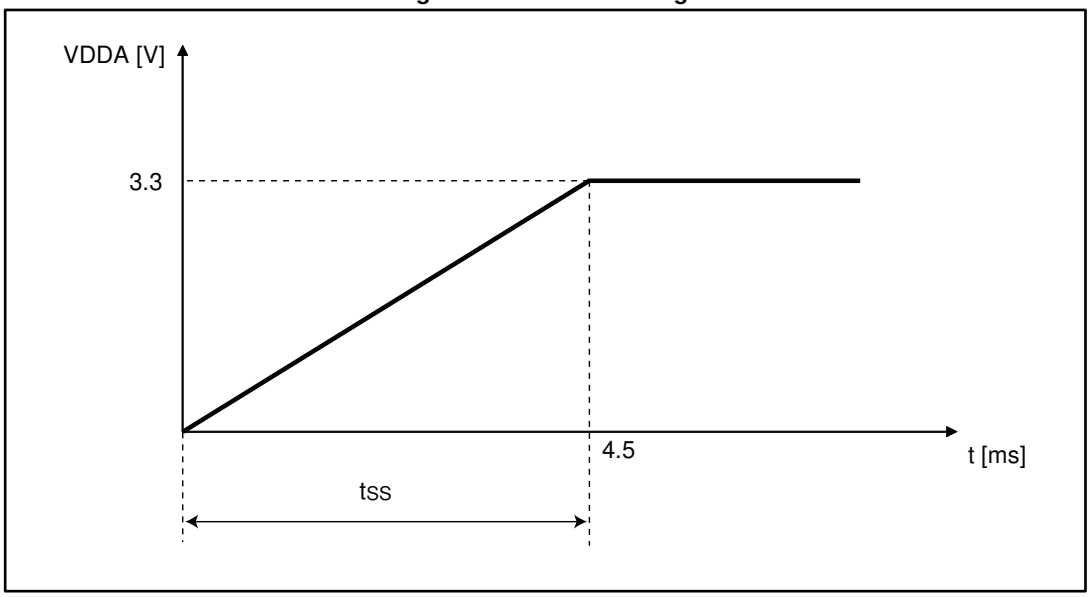


Figure 8: Soft-start timing



6.2.1 External optional 3.3 V supply voltage

It is possible provide externally the 3.3 V supply voltage directly on the VDDA pin. In this case, there are two possible configurations:

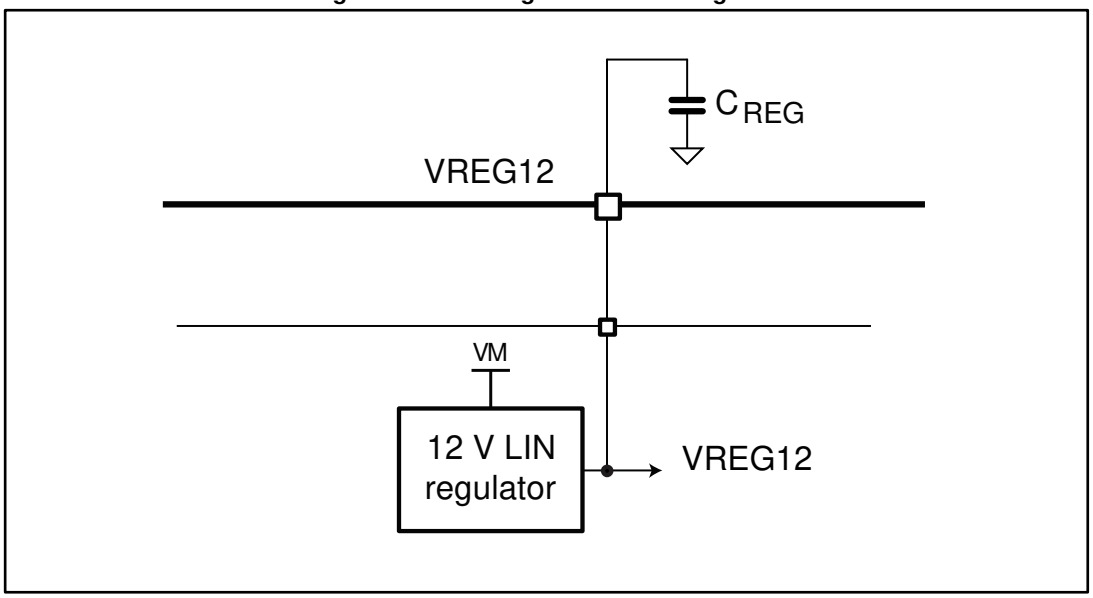
1. The SW pin floating or shorted to VM: in this case the internal power switch of the DC/DC converter continues to switch on/off according to the internal clock
2. The SW pin shorted to GND or VDD: in this case the internal power switch detects a short-circuit and it is latched off.

It is not allowed to apply VDD voltage externally in case of VM < VDD.

6.3 Linear regulator

The internal 12 V linear regulator is a LDO regulator providing the supply voltage for the gate drivers section. An external capacitor connected to the VREG12 pin is required.

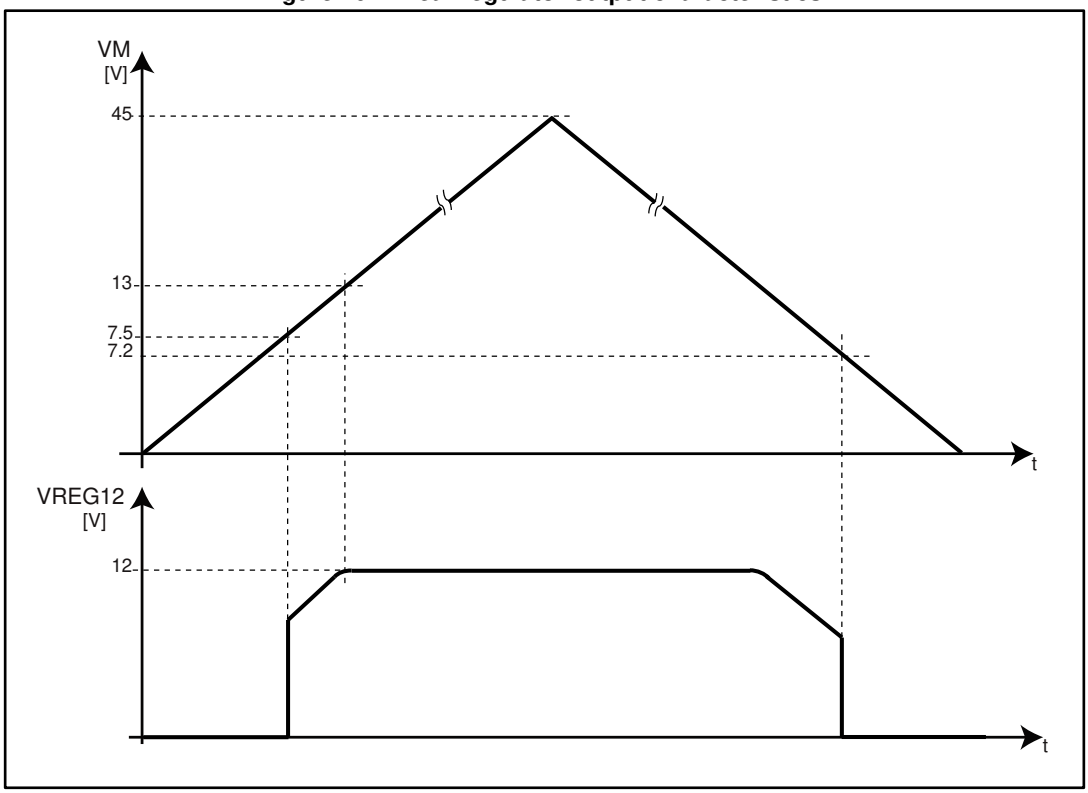
Figure 9: Linear regulator block diagram



When the VM voltage is below to 12 V, the VM pin and the linear regulator output can be shorted together providing the gate driver supply externally.

The linear regulator embeds a thermal protection as described in *Section 6.1.2: "Thermal protection"*.

Figure 10: Linear regulator output characteristics



The linear regulator is designed to supply the internal circuitry only and must not be used to supply external components.

6.4 Standby mode

The device is forced into the standby mode to reduce power consumption forcing both the OC_TH_STBY1 and OC_TH_STBY2 analog IC inputs low (see *Table 12: "OC threshold values"*).

When the standby mode is set the analog IC is put into the low consumption mode after a t_{sleep} time, in particular:

- The linear regulator is switched off
- All the output drivers are forced low (external power switches turned off)
- Op amps and comparators disabled
- The DC/DC regulator remains operative.

When the device exits from the standby mode a set time is necessary to recover a proper value of the 12 V internal regulator. This set time is strictly dependent by the capacitor connected on the VREG12 pin and can be calculated with *Equation 1*.