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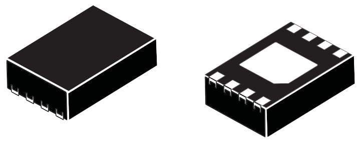
STTS2002

2.3 V memory module temperature sensor with a 2 Kb SPD EEPROM

Features

- 2.3 V memory module temperature sensor with integrated 2 Kb SPD EEPROM
- Forward compatible with JEDEC TSE 2002a2 and backward compatible with STTS424E02
- Operating temperature range:
  - –40 °C to +125 °C
- Single supply voltage: 2.3 V to 3.6 V
- 2 mm x 3 mm TDFN8, height: 0.80 mm (max)
  - JEDEC MO-229, WCED-3 compliant
- RoHS compliant, halogen-free



TDFN8
2 mm x 3 mm
(max height 0.80 mm)

Temperature sensor

- Temperature sensor resolution: programmable (9-12 bits) 0.25 °C (typ)/LSB - (10-bit) default
- Temperature sensor accuracy (max):
  - ± 1 °C from +75 °C to +95 °C
  - ± 2 °C from +40 °C to +125 °C
  - ± 3 °C from –40 °C to +125 °C
- ADC conversion time: 125 ms (max) at default resolution (10-bit)
- Typical operating supply current: 160 µA (EEPROM standby)
- Temperature hysteresis selectable set points from: 0, 1.5, 3, 6.0 °C
- Supports SMBus timeout 25 ms - 35 ms

2 Kb SPD EEPROM

- Functionality identical to ST's M34E02 SPD EEPROM
- Permanent and reversible software data protection for the lower 128 bytes
- Byte and page write (up to 16 bytes)
- Self-time WRITE cycle (5 ms, max)
- Automatic address incrementing

Two-wire bus

- Two-wire SMBus/I^{2}C - compatible serial interface
- Supports up to 400 kHz transfer rate
- Does not initiate clock stretching

Contents

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1 Description

The STTS2002 is targeted for DIMM modules in mobile personal computing platforms (laptops), servers and other industrial applications. The thermal sensor (TS) in the STTS2002 is compliant with the JEDEC specification TSE2002a2, which defines memory module thermal sensors requirements for mobile platforms. The 2 Kb serial presence detect (SPD) I^2C-compatible electrically erasable programmable memory (EEPROM) in the STTS2002 is organized as 256 x8 bits and is functionally identical to the industry standard M34E02.

The TS-SPD EEPROM combination provides space as well as cost savings for mobile and server platform dual inline memory modules (DIMM) manufacturers, as it is packaged in the compact 2 mm x 3 mm 8-lead TDFN package with a thinner maximum height of 0.80 mm. The DN package is compliant to JEDEC MO-229, variation WCED-3.

The digital temperature sensor has a programmable 9-12 bit analog-to-digital converter (ADC) which monitors and digitizes the temperature to a resolution of up to 0.0625 °C. The default resolution is 0.25 °C/LSB (10-bit). The typical accuracies over these temperature ranges are:

±2 °C over the full temperature measurement range of –40 °C to 125 °C

±1 °C in the +40 °C to +125 °C active temperature range, and

±0.5 °C in the +75 °C to +95 °C monitor temperature range

The temperature sensor in the STTS2002 is specified for operating at supply voltages from 2.3 V to 3.6 V. Operating at 3.3 V, the typical supply current is 160 µA (includes SMBus communication current).

The on-board sigma delta ADC converts the measured temperature to a digital value that is calibrated in °C. For Fahrenheit applications, a lookup table or conversion routine is required. The STTS2002 is factory-calibrated and requires no external components to measure temperature.

The digital temperature sensor component has user-programmable registers that provide the capabilities for DIMM temperature-sensing applications. The open drain event output pin is active when the monitoring temperature exceeds a programmable limit, or it falls above or below an alarm window. The user has the option to set the event output as a critical temperature output. This pin can be configured to operate in either a comparator mode for thermostat operation or in interrupt mode.

The 2 Kb serial EEPROM memory in the STTS2002 has the ability to permanently lock the data in its first half (upper) 128 bytes (locations 00h to 7Fh). This feature has been designed specifically for use in DRAM DIMMs with SPD. All of the information concerning the DRAM module configuration (e.g. access speed, size, and organization) can be kept write protected in the first half of the memory. The second half (lower) 128 bytes of the memory can be write protected using two different software write protection mechanisms.

By sending the device a specific sequence, the first 128 bytes of the memory become write protected: permanently or resettable. In the STTS2002 the write protection of the memory array is dependent on whether the software protection has been set.

2 Serial communications

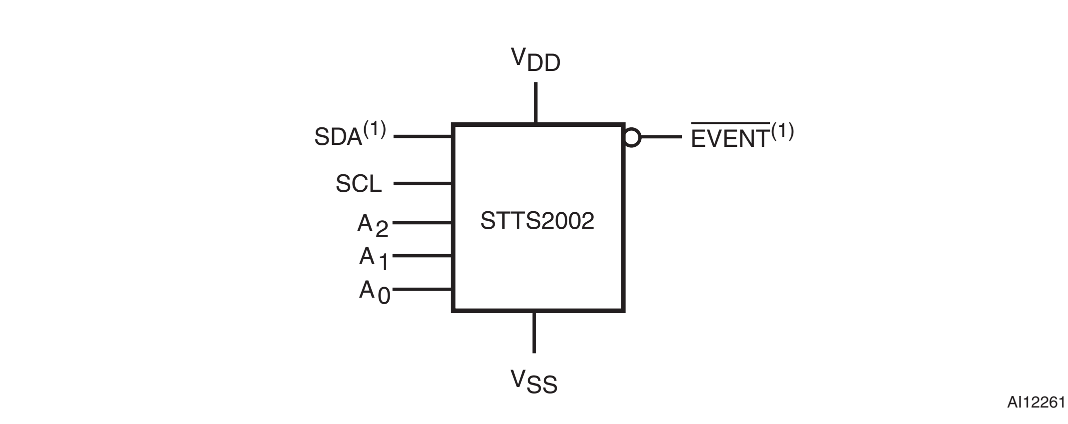
The STTS2002 has a simple 2-wire SMBus/I^2C-compatible digital serial interface which allows the user to access both the 2 Kb serial EEPROM and the data in the temperature register at any time. It communicates via the serial interface with a master controller which operates at speeds of up to 400 kHz. It also gives the user easy access to all of the STTS2002 registers in order to customize device operation.

2.1 Device type identifier (DTI) code

The JEDEC temperature sensor and EEPROM each have their own unique I^2C address, which ensures that there are no compatibility or data translation issues. This is due to the fact that each of the devices have their own 4-bit DTI code, while the remaining three bits are configurable. This enables the EEPROM and thermal sensors to provide their own individual data via their unique addresses and still not interfere with each other's operation in any way. The DTI codes are:

- '0011' for the TS, and
- '1010' for addressing the EEPROM memory array, and
- ‘0110’ to access the software write protection settings of the EEPROM.

Figure 1. Logic diagram



1. SDA and $\overline{EVENT}$ are open drain.

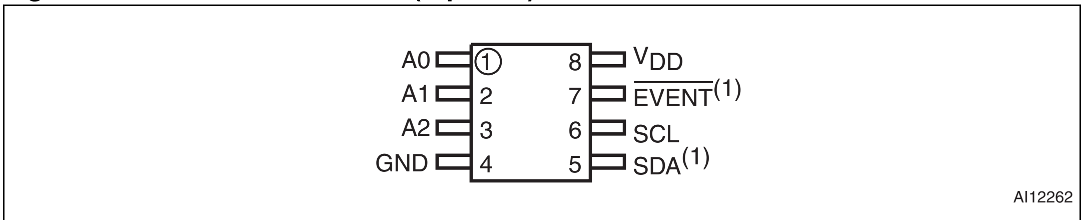
Table 1. Signal names

Pin	Symbol	Description	Direction
1	A0	Serial bus address selection pin. Can be tied to V_{SS} or V_{DD}.	Input
2	A1	Serial bus address selection pin. Can be tied to V_{SS} or V_{DD}.	Input
3	A2	Serial bus address selection pin. Can be tied to V_{SS} or V_{DD}.	Input
4	V_{SS}	Supply ground	
5	SDA(1)	Serial data	Input/output
6	SCL	Serial clock	Input
7	$\overline{EVENT}$(1)	Event output pin. Open drain and active-low.	Output
8	V_{DD}	Supply power (2.3 V to 3.6 V)	

1. SDA and $\overline{EVENT}$ are open drain.

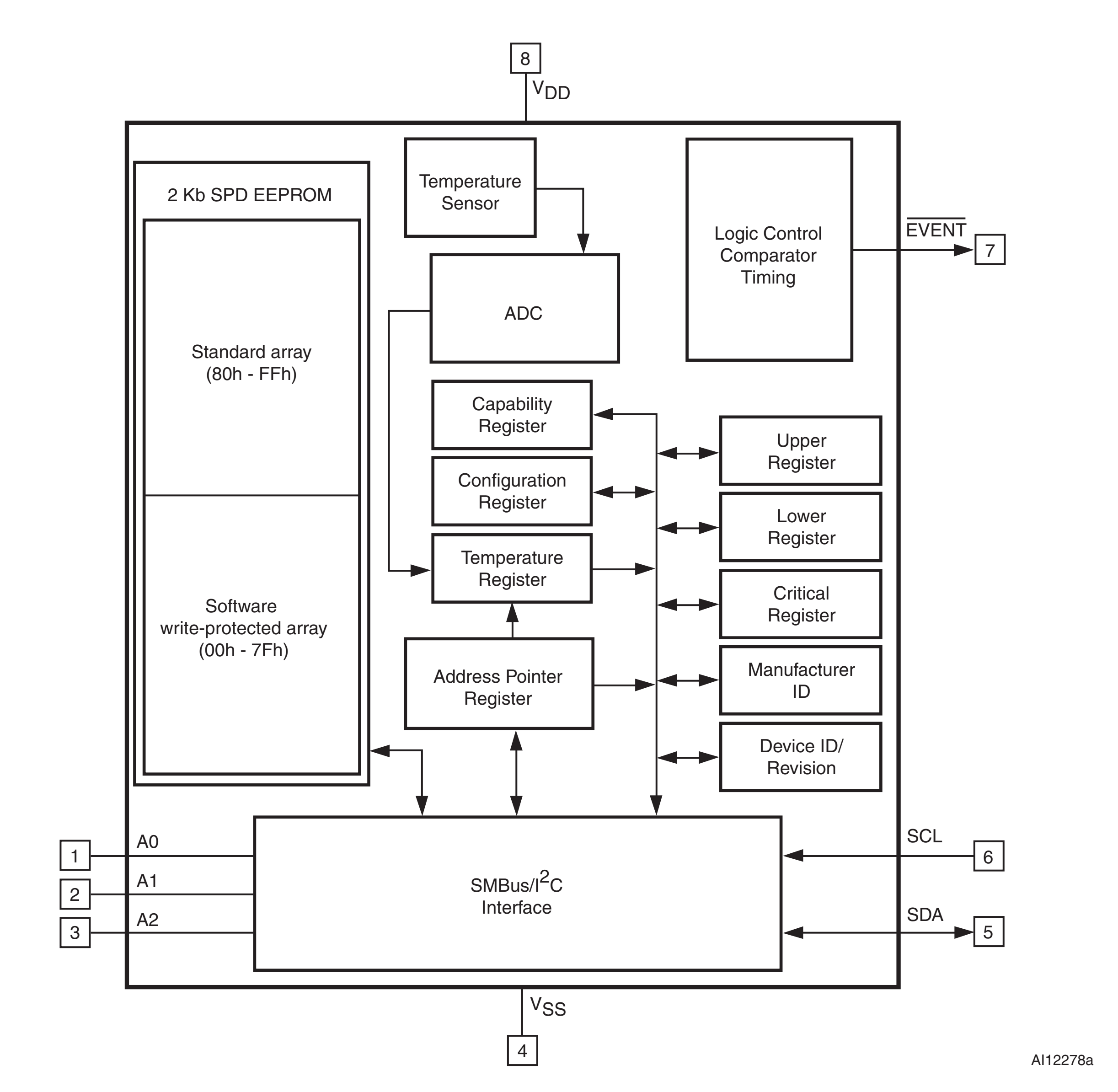
Note: See Section 2.2: Pin descriptions on page 10 for details.

Figure 2. TDFN8 connections (top view)



1. SDA and $\overline{EVENT}$ are open drain.

Figure 3. Block diagram



2.2 Pin descriptions

2.2.1 A0, A1, A2

A2, A1, and A0 are selectable address pins for the 3 LSBs of the I^2C interface address. They can be set to V_{DD} or GND to provide 8 unique address selections. These pins are internally connected to the E2, E1, E0 (chip selects) of EEPROM.

2.2.2 V_{SS} (ground)

This is the reference for the power supply. It must be connected to system ground.

2.2.3 SDA (open drain)

This is the serial data input/output pin.

2.2.4 SCL

This is the serial clock input pin.

2.2.5 $\overline{\text{EVENT}}$ (open drain)

This output pin is open drain and active-low.

2.2.6 V_{DD} (power)

This is the supply voltage pin, and ranges from 2.3 V to 3.6 V.

3 Temperature sensor operation

The temperature sensor continuously monitors the ambient temperature and updates the temperature data register. Temperature data is latched internally by the device and may be read by software from the bus host at any time.

The SMBus/I^2C slave address selection pins allow up to 8 such devices to co-exist on the same bus. This means that up to 8 memory modules can be supported, given that each module has one such slave device address slot.

After initial power-on, the configuration registers are set to the default values. The software can write to the configuration register to set bits per the bit definitions in *Section 3.1: SMBus/I^2C communications*.

For details of operation and usage of 2 Kb SPD EEPROM, refer to *Section 5: SPD EEPROM operation*.

3.1 SMBus/I^2C communications

The registers in this device are selected by the pointer register. At power-up, the pointer register is set to “00”, which is the capability register location. The pointer register latches the last location it was set to. Each data register falls into one of three types of user accessibility:

1. Read-only
2. Write-only, and
3. WRITE/READ same address

A WRITE to this device will always include the address byte and the pointer byte. A WRITE to any register other than the pointer register, requires two data bytes.

Reading this device is achieved in one of two ways:

- If the location latched in the pointer register is correct (most of the time it is expected that the pointer register will point to one of the read temperature registers because that will be the data most frequently read), then the READ can simply consist of an address byte, followed by retrieval of the two data bytes.
- If the pointer register needs to be set, then an address byte, pointer byte, repeat start, and another address byte will accomplish a READ.

The data byte transfers the MSB first. At the end of a READ, this device can accept either an acknowledge (ACK) or no acknowledge (No ACK) status from the master. The No ACK status is typically used as a signal for the slave that the master has read its last byte. This device subsequently takes up to 125 ms to measure the temperature for the default temperature resolution.

Note: STTS2002 does not initiate clock stretching which is an optional I^2C bus feature.

Figure 4. SMBus/I²C write to pointer register

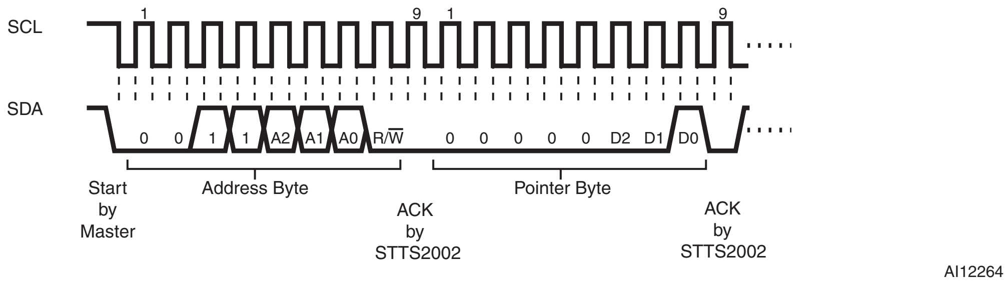


Figure 5. SMBus/I²C write to pointer register, followed by a read data word

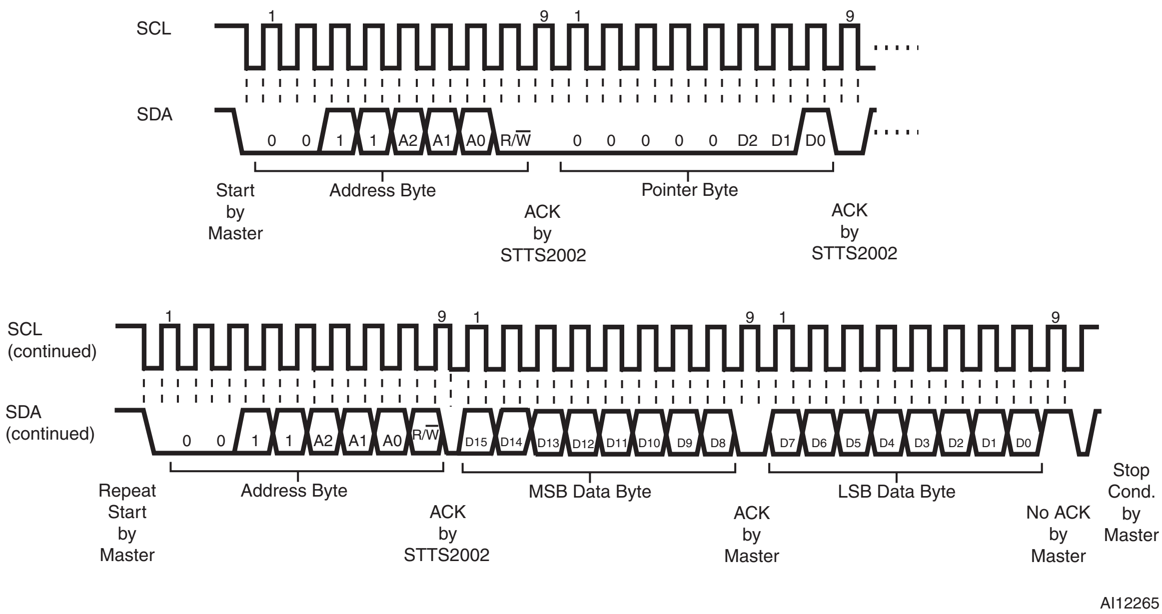
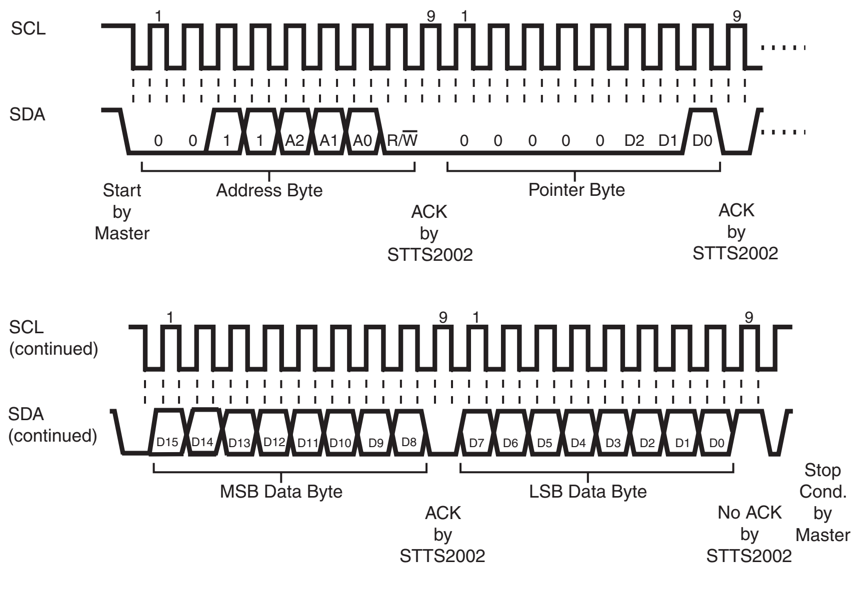


Figure 6. SMBus/I^{2}C write to pointer register, followed by a write data word



3.2 SMBus/I^{2}C slave sub-address decoding

The physical address for the TS is different than that used by the EEPROM. The TS physical address is binary 0 0 1 1 A2 A1 A0 RW, where A2, A1, and A0 are the three slave sub-address pins, and the LSB “RW” is the READ/WRITE flag.

The EEPROM physical address is binary 1 0 1 0 A2 A1 A0 RW for the memory array and is 0 1 1 0 A2 A1 A0 RW for permanently set write protection mode.

3.3 SMBus/I²C AC timing consideration

In order for this device to be both SMBus- and I²C-compatible, it complies to a subset of each specification. The requirements which enable this device to co-exist with devices on either an SMBus or an I²C bus include:

- The SMBus minimum clock frequency is required.
- The SMBus timeout is maximum 35 ms (temperature sensor only).

Figure 7. SMBus/I²C timing diagram

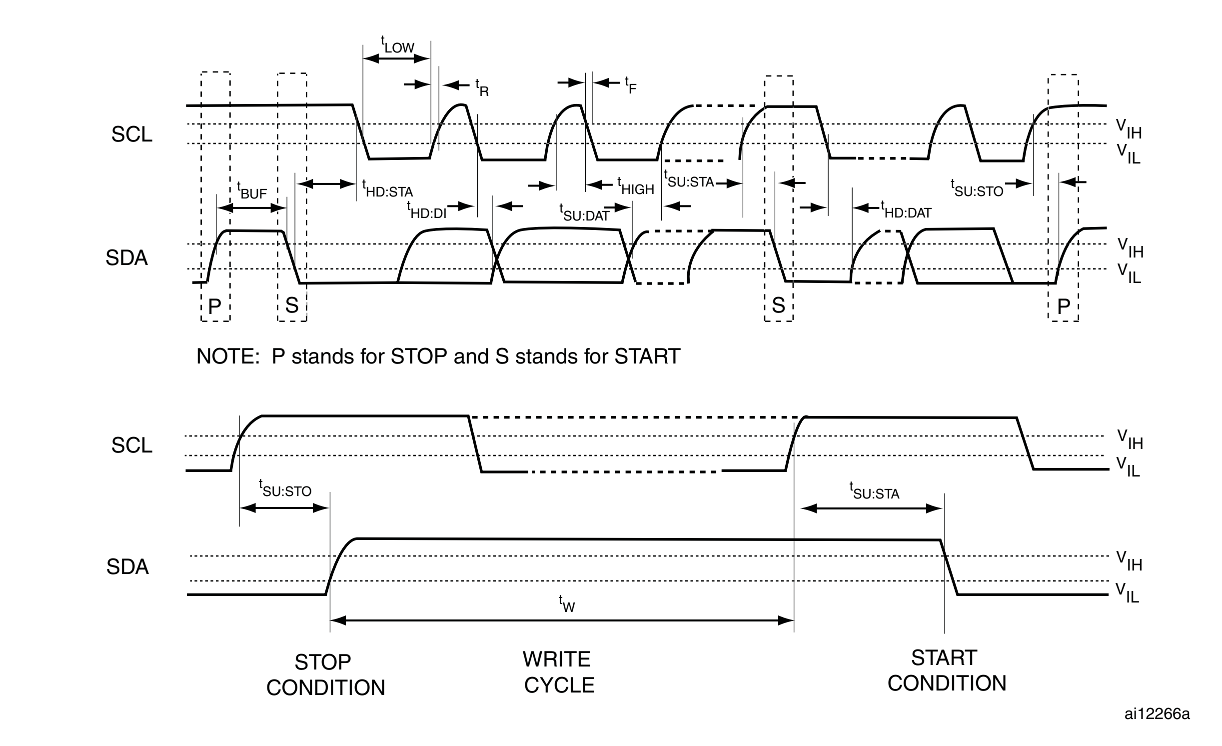


Table 2. AC characteristics of STTS2002 for SMBus and I^2C compatibility timings

Symbol	Parameter	Min	Max	Units
f_{SCL}	SMBUS/I^2C clock frequency	10	400	kHz
t_{HIGH}	Clock high period	600	–	ns
t_{LOW}(1)	Clock low period	1300	–	ns
t_R(2)	Clock/data rise time	–	300	ns
t_F(2)	Clock/data fall time	20	300	ns
$t_{SU:DAT}$	Data in setup time	100	–	ns
$t_{HD:DI}$	Data in hold time	0	–	ns
$t_{HD:DAT}$	Data out hold time	200	900	ns
$t_{SU:STA}$(3)	Repeated start condition setup time	600	–	ns
$t_{HD:STA}$	Hold time after (repeated) start condition. After this period, the first clock cycle is generated.	600	–	ns
$t_{SU:STO}$	Stop condition setup time	600	–	ns
t_{BUF}	Bus free time between stop (P) and start (S) conditions	1300	–	ns
t_W(4)	WRITE time for EEPROM	–	10	ms
$t_{timeout}$(5)	Bus timeout (temperature sensor only)	25	35	ms

1. STTS2002 will not initiate clock stretching which is an I^2C bus optional feature.
2. Guaranteed by design and characterization, not necessarily tested.
3. For a restart condition, or following a WRITE cycle.
4. This parameter reflects maximum WRITE time for EEPROM.
5. Bus timeout value supported depends on setting of TMOUT bit 6 in capability register.

4 Temperature sensor registers

The temperature sensor component is comprised of various user-programmable registers. These registers are required to write their corresponding addresses to the pointer register. They can be accessed by writing to their respective addresses (see *Table 3*). Pointer register bits 7 - 4 must always be written to '0' (see *Table 4*). This must be maintained, as not setting these bits to '0' may keep the device from performing to specifications.

The main registers include:

- *Capability register (read-only)*
- *Configuration register (read/write)*
- *Temperature register (read-only)*
- *Temperature trip point registers (read/write)*, including
  - Alarm temperature upper boundary,
  - Alarm temperature lower boundary, and
  - Critical temperature.
- *Manufacturer ID register (read-only)*
- *Device ID and device revision ID register (read-only)*
- *Temperature resolution register (TRES) (read/write)*

See *Table 5 on page 17* for pointer register selection bit details.

Table 3. Temperature sensor registers summary

Address (hex)	Register name		Power-on default
Not applicable	Address pointer		Undefined
00	Capability	B-grade	0x006F
01	Configuration		0x0000
02	Alarm temperature upper boundary trip		0x0000
03	Alarm temperature lower boundary trip		0x0000
04	Critical temperature trip		0x0000
05	Temperature		Undefined
06	Manufacturer's ID		0x104A
07	Device ID/revision		0x0300
08	Temperature resolution register		0x0001

Note: Registers beyond the specified (00-08) are reserved for STMicroelectronics internal use only, for device test modes in product manufacturing. The registers must NOT be accessed by the user (customer) in the system application or the device may not perform according to specifications.

Table 4. Pointer register format

MSB							LSB
Bit7	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
0	0	0	0	P3	P2	P1	P0
				Pointer/register select bits			

Table 5. Pointer register select bits (type, width, and default values)

P3	P2	P1	P0	Name	Register description		Width (bits)	Type (R/$\overline{W}$)	Default state (POR)
0	0	0	0	CAPA	Thermal sensor capabilities	B-grade only	16	R	00 6F
0	0	0	1	CONF	Configuration		16	R/$\overline{W}$	00 00
0	0	1	0	UPPER	Alarm temperature upper boundary		16	R/$\overline{W}$	00 00
0	0	1	1	LOWER	Alarm temperature lower boundary		16	R/$\overline{W}$	00 00
0	1	0	0	CRITICAL	Critical temperature		16	R/$\overline{W}$	00 00
0	1	0	1	TEMP	Temperature		16	R	00 00
0	1	1	0	MANU	Manufacturer ID		16	R	10 4A
0	1	1	1	ID	Device ID/revision		16	R	03 00
1	0	0	0	TRES	Temperature resolution register		8	R/$\overline{W}$	01

4.1 Capability register (read-only)

This 16-bit register is read-only, and provides the TS capabilities which comply with the minimum JEDEC TSE2002a2 specifications (see *Table 6* and *Table 7 on page 18*). The STTS2002 resolution is programmable via writing to pointer 08 register. The power-on default value is 0.25 °C/LSB (10-bit).

Table 6. Capability register format

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
Bit7	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
EVSD	TMOUT	V_{HV}	TRES1	TRES0	Wider range	Higher precision	Alarm and critical trips

Table 7. Capability register bit definitions

Bit	Definition
0	Basic capability – 0 = Alarm and critical trips turned OFF. **– 1 = Alarm and critical trips turned ON.**
1	Accuracy – 0 = Accuracy ±2 °C over the active range and ±3 °C over the monitoring range (C-grade). – **1 = High accuracy ±1 °C over the active range and ±2 °C over the monitoring range (B-grade) (default)**.
2	Range width – 0 = Values lower than 0 °C will be clamped and represented as binary value '0'. **– 1 = Temperatures below 0 °C can be read and the Sign bit will be set accordingly.**
4:3	Temperature resolution – 00 = 9 bit, 0.5 °C/LSB **– 01 = 10 bit, 0.25 °C/LSB - default resolution** – 10 = 11 bit, 0.125 °C/LSB – 11 = 12 bit, 0.0625 °C/LSB
5	(V_{HV}) high voltage support for A0 (pin 1) **– 1 = STTS2002 supports a voltage up to 10 volts on the A0 pin - (default)**
6	TMOUT - bus timeout support (for temperature sensor only) – 0 = $t_{timeout}$ is supported in the range of 10 to 60 ms – 1 = **Default for STTS2002-SMBus compatible 25 ms - 35 ms** Note: Timeout is not required for EEPROM component
7	EVSD - $\overline{\text{EVENT}}$ behavior upon shutdown **– 0 = Default for STTS2002. The $\overline{\text{EVENT}}$ output freezes in its current state when entering shutdown. Upon entering shutdown, the $\overline{\text{EVENT}}$ output remains in the previous state until the next thermal data conversion or possibly sooner if $\overline{\text{EVENT}}$ is programmed for comparator mode.** – 1 = $\overline{\text{EVENT}}$ output is deasserted (not driven) when entering shutdown and remains deasserted upon exit from shutdown until the next thermal sample is taken or possibly sooner if $\overline{\text{EVENT}}$ is programmed for comparator mode.
15:8	Reserved **These values must be set to '0'.**

4.2 Configuration register (read/write)

The 16-bit configuration register stores various configuration modes that are used to set up the sensor registers and configure according to application and JEDEC requirements (see *Table 8 on page 19* and *Table 9 on page 20*).

4.2.1 Event thresholds

All event thresholds use hysteresis as programmed in register address 0x01 (bits 10 through 9) to be set when they de-assert.

4.2.2 Interrupt mode

The interrupt mode allows an event to occur where software may write a '1' to the clear event bit (bit 5) to de-assert the event Interrupt output until the next trigger condition occurs.

4.2.3 Comparator mode

Comparator mode enables the device to be used as a thermostat. READs and WRITEs on the device registers will not affect the event output in comparator mode. The event signal will remain asserted until temperature drops outside the range or is re-programmed to make the current temperature “out of range”.

4.2.4 Shutdown mode

The STTS2002 features a shutdown mode which disables all power-consuming activities (e.g. temperature sampling operations), and leaves the serial interface active. This is selected by setting shutdown bit (bit 8) to '1'. In this mode, the devices consume the minimum current (I_{SHDN}), as shown in *Table 30 on page 41*.

Note: Bit 8 cannot be set to '1' while bits 6 and 7 (the lock bits) are set to '1'.

The device may be enabled for continuous operation by clearing bit 8 to '0'. In shutdown mode, all registers may be read or written to. Power recycling will also clear this bit and return the device to continuous mode as well.

Table 8. Configuration register format

Bit15	**Bit14**	**Bit13**	**Bit12**	**Bit11**	**Bit10**	**Bit9**	**Bit8**
RFU	RFU	RFU	RFU	RFU	Hysteresis	Hysteresis	Shutdown mode
Bit7	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
Critical lock bit	Alarm lock bit	Clear event	Event output status	Event output control	Critical event only	Event polarity	Event mode

Table 9. Configuration register bit definitions

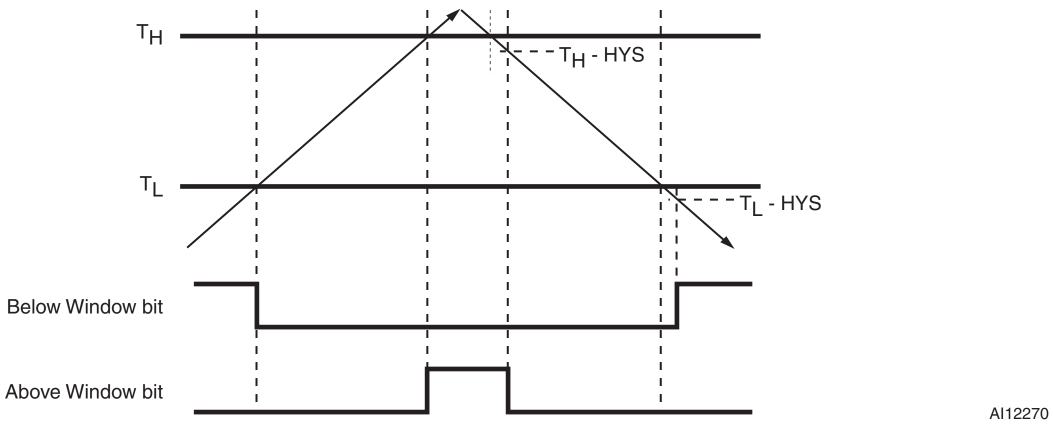
Bit	Definition
0	Event mode **– 0 = Comparator output mode (this is the default).** – 1 = Interrupt mode; when either of the lock bits (bit6 or bit7) is set, this bit cannot be altered until it is unlocked.
1	Event polarity(1) The event polarity bit controls the active state of the EVENT pin. The EVENT pin is driven to this state when it is asserted. **– 0 = Active-low (this is the default). Requires a pull-up resistor to set the inactive state of the open-drain output. The power to the pull-up resistor should not be greater than V_{DD} + 0.2 V. Active state is logical "0".** – 1 = Active-high. The active state of the pin is then logical "1".
2	Critical event only **– 0 = Event output on alarm or critical temperature event (this is the default).** – 1 = Event only if the temperature is above the value in the critical temperature register ($T_A > T_{CRIT}$); when the alarm window lock bit (bit6) is set, this bit cannot be altered until it is unlocked.
3	Event output control **– 0 = Event output disabled (this is the default).** – 1 = Event output enabled; when either of the lock bits (bit6 or bit7) is set, this bit cannot be altered until it is unlocked.
4	Event status (read-only)(2) **– 0 = Event output condition is not being asserted by this device.** – 1 = Event output condition is being asserted by this device via the alarm window or critical trip event.
5	Clear event (write-only)(3) **– 0 = No effect.** – 1 = Clears the active event in interrupt mode. The pin is released and will not assert until a new interrupt condition occurs.
6	Alarm window lock bit **– 0 = Alarm trips are not locked and can be altered (this is the default).** – 1 = Alarm trip register settings cannot be altered. This bit is initially cleared. When set, this bit returns a logic '1' and remains locked until cleared by an internal power-on reset. These bits can be written to with a single WRITE, and do not require double WRITEs.
7	Critical trip lock bit **– 0 = Critical trip is not locked and can be altered (this is the default).** – 1 = Critical trip register settings cannot be altered. This bit is initially cleared. When set, this bit returns a logic '1' and remains locked until cleared by an internal power-on reset. These bits can be written to with a single WRITE, and do not require double WRITEs.
8	Shutdown mode **– 0 = TS is enabled, continuous conversion (this is the default).** – 1 = Shutdown TS when the shutdown, device, and A/D converter are disabled in order to save power. No event conditions will be asserted; when either of the lock bits (bit6 or bit7) is set, then this bit cannot be altered until it is unlocked. It can be cleared at any time.

Table 9. Configuration register bit definitions (continued)

Bit	Definition
10:9	Hysteresis enable (see *Figure 8* and *Table 10*) **– 00 = Hysteresis is disabled (default)** – 01 = Hysteresis is enabled at 1.5 °C – 10 = Hysteresis is enabled at 3 °C – 11 = Hysteresis is enabled at 6 °C Hysteresis applies to all limits when the temperature is dropping below the threshold so that once the temperature is above a given threshold, it must drop below the threshold minus the hysteresis in order to be flagged as an interrupt event. Note that hysteresis is also applied to the EVENT pin functionality. When either of the lock bits is set, these bits cannot be altered.
15:11	**Reserved for future use. These bits will always read ‘0’ and writing to them will have no effect. For future compatibility, all RFU bits must be programmed as ‘0’.**

1. As this device is used in DIMM (memory modules) applications, it is strongly recommended that only the active-low polarity (default) is used. This will provide full compatibility with the STTS424E02. This is the recommended configuration for the STTS2002.
2. The actual incident causing the event can be determined from the read temperature register. Interrupt events can be cleared by writing to the clear event bit (writing to this bit will have no effect on overall device functioning).
3. Writing to this register has no effect on overall device functioning in comparator mode. When read, this bit will always return a logic '0' result.

Figure 8. Hysteresis



1. T_H = Value stored in the alarm temperature upper boundary trip register
2. T_L = Value stored in the alarm temperature lower boundary trip register
3. HYS = Absolute value of selected hysteresis

Table 10. Hysteresis as applied to temperature movement

	Below alarm window bit		Above alarm window bit	
	Temperature slope	Temperature threshold	Temperature slope	Temperature threshold
Sets	Falling	T_L - HYS	Rising	T_H
Clears	Rising	T_L	Falling	T_H - HYS

4.2.5 Event output pin functionality

The STTS2002 $\overline{\text{EVENT}}$ pin is an open drain output that requires a pull-up to V_{DD} on the system motherboard or integrated into the master controller. $\overline{\text{EVENT}}$ has three operating modes, depending on configuration settings and any current out-of-limit conditions. These modes are interrupt, comparator or critical.

In interrupt mode the $\overline{\text{EVENT}}$ pin will remain asserted until it is released by writing a ‘1’ to the “Clear Event” bit in the status register. The value to write is independent of the EVENT polarity bit.

In comparator mode the $\overline{\text{EVENT}}$ pin will clear itself when the error condition that caused the pin to be asserted is removed.

In the critical mode the $\overline{\text{EVENT}}$ pin will only be asserted if the measured temperature exceeds the critical limit. Once the pin has been asserted, it will remain asserted until the temperature drops below the critical limit minus hysteresis. *Figure 9 on page 23* illustrates the operation of the different modes over time and temperature.

When the hysteresis bits (bits 10 and 9) are enabled, hysteresis may be used to sense temperature movement around trigger points. For example, when using the “above alarm window” bit (temperature register bit 14, see *Table 12 on page 24*) and hysteresis is set to 3 °C, as the temperature rises, bit 14 is set (bit 14 = 1). The temperature is above the alarm window and the temperature register contains a value that is greater than the value set in the alarm temperature upper boundary register (see *Table 16 on page 26*).

If the temperature decreases, bit 14 will remain set until the measured temperature is less than or equal to the value in the alarm temperature upper boundary register minus 3 °C (see *Figure 8 on page 21* and *Table 10 on page 21* for details.

Similarly, when using the “below alarm window” bit (temperature register bit 13, see *Table 12 on page 24*) will be set to '0'. The temperature is equal to or greater than the value set in the alarm temperature lower boundary register (see *Table 17 on page 26*). As the temperature decreases, bit 13 will be set to '1' when the value in the temperature register is less than the value in the alarm temperature lower boundary register minus 3 °C (see *Figure 8 on page 21* and *Table 10 on page 21* for details.

The device will retain the previous state when entering the shutdown mode. If the device enters the shutdown mode while the $\overline{\text{EVENT}}$ pin is low, the shutdown current will increase due to the additional event output pull-down current.

Figure 9. Event output boundary timings

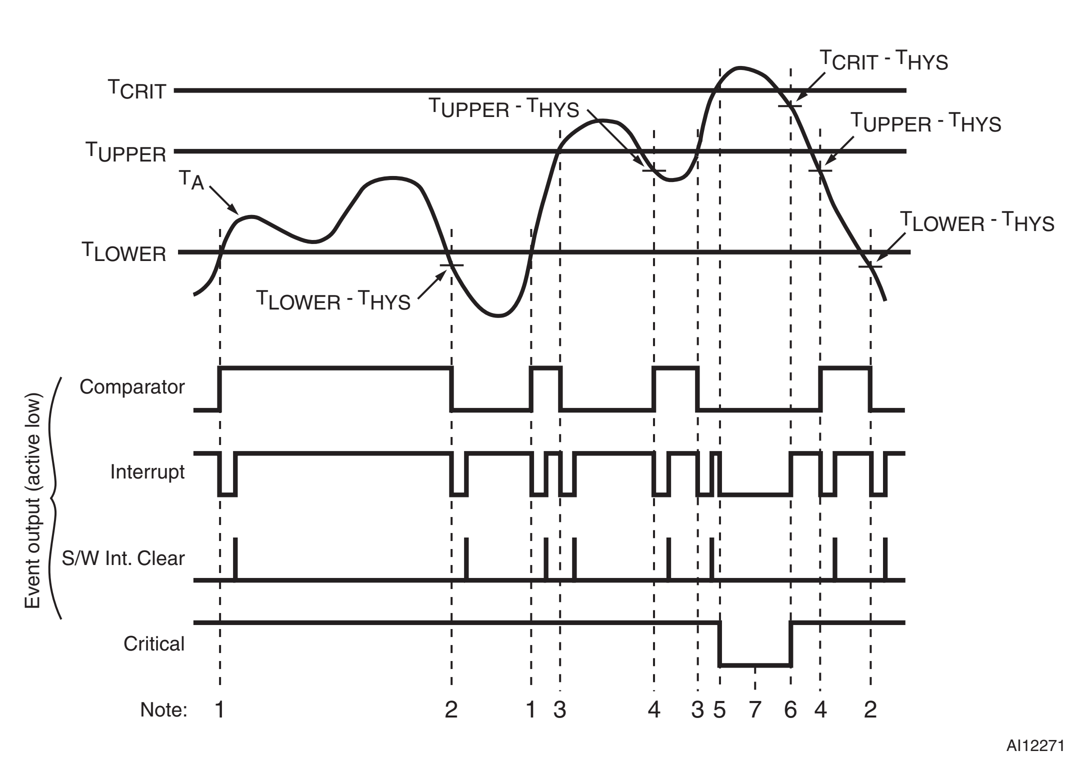


Table 11. Legend for *Figure 9: Event output boundary timings*

Note	Event output boundary conditions	Event output			T_A bits		
		Comparator	Interrupt	Critical	15	14	13
1	$T_A \geq T_{LOWER}$	H	L	H	0	0	0
2	$T_A < T_{LOWER} - T_{HYS}$	L	L	H	0	0	1
3	$T_A > T_{UPPER}$	L	L	H	0	1	0
4	$T_A \leq T_{UPPER} - T_{HYS}$	H	L	H	0	0	0
5	$T_A \geq T_{CRIT}$	L	L	L	1	0	0
6	$T_A < T_{CRIT} - T_{HYS}$	L	H	H	0	1	0
7	When $T_A \geq T_{CRIT}$ and $T_A < T_{CRIT} - T_{HYS}$, the event output is in comparator mode and bit 0 of the configuration register (interrupt mode) is ignored.						

Systems that use the active high mode for Event output must be wired point-to-point between the STTS2002 and the sensing controller. Wire-OR configurations should not be used with active high Event output since any device pulling the Event output signal low will mask the other devices on the bus. Also note that the normal state of Event output in active high mode is a ‘0’ which will constantly draw power through the pull-up resistor.

4.3 Temperature register (read-only)

This 16-bit, read-only register stores the temperature measured by the internal band gap TS as shown in *Table 12*. When reading this register, the MSBs (bit 15 to bit 8) are read first, and then the LSBs (bit 7 to bit 0) are read. The result is the current-sensed temperature. The data format is 2s complement with one LSB = 0.25 °C for the default resolution. The MSB has a 128 °C resolution.

The trip status bits represent the internal temperature trip detection, and are not affected by the status of the event or configuration bits (e.g. event output control or clear event). If neither of the above or below values are set (i.e. both are 0), then the temperature is exactly within the user-defined alarm window boundaries.

4.3.1 Temperature format

The 16-bit value used in the trip point set and temperature read-back registers is 2s complement, with the LSB equal to 0.0625 °C (see *Table 12*). For example:

1. a value of 019C h represents 25.75 °C,
2. a value of 07C0 h represents 124 °C, and
3. a value of 1E74 h represents –24.75 °C

All unused resolution bits are set to zero. The MSB will have a resolution of 128 °C. The STTS2002 supports programmable resolutions (9-12 bits) which is 0.5 to 0.0625 °C/LSB. The default is 0.25 °C/LSB (10 bits) programmable.

The upper 3 bits indicate trip status based on the current temperature, and are not affected by the event output status.

Table 12. Temperature register format

			Sign MSB										**LSB(1)**			
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1(2)**	**Bit 0(3)**	
Flag bit	Flag bit	Flag bit	Sign	128	64	32	16	8	4	2	1	0.5	0.25	0.125	0.0625	°C/LSB
Above critical input(4)	Above alarm window(4)	Below alarm window(4)	Temperature (default - 10 bit)											0	0	
Flag bits			Example hex value of 07C0 corresponds to 124 °C (10-bit)													
0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	07C0 h
Flag bits			Example hex value of 1D80 corresponds to –40 °C (10-bit)													
0	0	0	1	1	1	0	1	1	0	0	0	0	0	0	0	1D80 h

1. Bit 2 is LSB for default 10-bit mode.
2. Depending on status of the resolution register, bit 1 may display 0.125 °C value.
3. Depending on status of the resolution register, bit 0 may display 0.0625 °C value.
4. See *Table 14* for explanation.

A 0.25 °C minimum granularity is supported in all registers. Examples of valid settings and interpretation of temperature register bits for 10-bit (0.25 °C) default resolution are provided in *Table 13*.

Table 13. Temperature register coding examples (for 10 bits)

B15:B0 (binary)	Value	Units
xxx0 0000 0010 11xx	+2.75	°C
xxx0 0000 0001 00xx	+1.00	°C
xxx0 0000 0000 01xx	+0.25	°C
xxx0 0000 0000 00xx	0	°C
xxx1 1111 1111 11xx	–0.25	°C
xxx1 1111 1110 00xx	–1.00	°C
xxx1 1111 1101 11xx	–2.25	°C

Table 14. Temperature register bit definitions

Bit	Definition with hysteresis = 0
13	Below (temperature) alarm window – 0 = Temperature is equal to or above the alarm window lower boundary temperature. – 1 = Temperature is below the alarm window.
14	Above (temperature) alarm window. – 0 = Temperature is equal to or below the alarm window upper boundary temperature. – 1 = Temperature is above the alarm window.
15	Above critical trip – 0 = Temperature is below the critical temperature setting. – 1 = Temperature is equal to or above the critical temperature setting.

4.4 Temperature trip point registers (read/write)

The STTS2002 alarm mode registers provide for 11-bit data in 2s compliment format. The data provides for one LSB = 0.25 °C. All unused bits in these registers are read as '0'.

The STTS2002 has three temperature trip point registers (see *Table 15*):

- Alarm temperature upper boundary threshold (*Table 16*),
- Alarm temperature lower boundary threshold (*Table 17*), and
- Critical temperature trip point value (*Table 18*).

Note: If the upper or lower boundary threshold values are being altered in-system, all interrupts should be turned off until a known state can be obtained to avoid superfluous interrupt activity.