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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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STTS424

Memory module temperature sensor

Features

- Temperature sensor compliant with JEDEC JC42.4

Temperature sensor

- Temperature sensor resolution: 0.25°C (typ)/LSB
- Temperature sensor accuracy:
  - ± 1°C from +75°C to +95°C
  - ± 2°C from +40°C to +125°C
  - ± 3°C from –40°C to +125°C
- ADC conversion time: 125 ms (max)
- Supply voltage: 2.7 V to 3.6 V
- Maximum operating supply current: 200 µA
- Hysteresis selectable set points from: 0, 1.5, 3, 6.0°C
- Ambient temperature sensing range: –40°C to 125°C
- Supports bus timeout

Two-wire bus

- 2-wire SMBus/I^2C - compatible serial interface
- Supports up to 400 kHz transfer rate
- Does not initiate clock stretching

Packages

- 2 mm x 3 mm TDFN8, height: 0.80 mm (max)[a]
- RoHS compliant, halogen-free

TDFN8 (DN)
2 mm x 3 mm (max height 0.80 mm)

a. Compliant to JEDEC MO-229, WCED-3

Contents

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1 Description

The STTS424 is targeted for DIMM modules in mobile personal computing platforms (laptops), server memory modules, and other industrial applications. The thermal sensor (TS) in the STTS424 is fully compliant with the JEDEC specification which defines memory module thermal sensors requirements for mobile platforms.

The TS provides space as well as cost savings for mobile and server platform dual inline memory modules (DIMM) manufacturers as it is packaged in the compact 2 mm x 3 mm (height 0.80 mm) 8-lead TDFN package which is compliant to JEDEC MO-229, variation WCED-3.

The temperature sensor includes a band gap-based temperature sensor and 10-bit analog-to-digital converter (ADC) which monitor and digitize the temperature to a resolution of up to 0.25°C. The typical accuracies over these temperature ranges are:

- ±3°C (max) over the full temperature measurement range of –40°C to 125°C
- ±2°C in the +40°C to +125°C temperature range and
- ±1°C in the +75°C to +95°C temperature range

The temperature sensor in the STTS424 is specified for operating at supply voltages from 2.7 V to 3.6 V. Operating at 3.3 V, the supply current is 100 µA (typ).

The on-board sigma delta ADC converts the measured temperature to a digital value that is calibrated in °C. For Fahrenheit applications, a lookup table or conversion routine is required. The STTS424 is factory-calibrated and requires no external components to measure temperature.

The digital temperature sensor component has user-programmable registers that provide the capabilities for DIMM temperature-sensing applications. The open drain event output pin is active when the monitoring temperature exceeds a programmable limit, or it falls above or below an alarm window. The user has the option to set the event output as a critical temperature output. This pin can be configured to operate in either a comparator mode for thermostat operation or in interrupt mode.

2 Serial communications

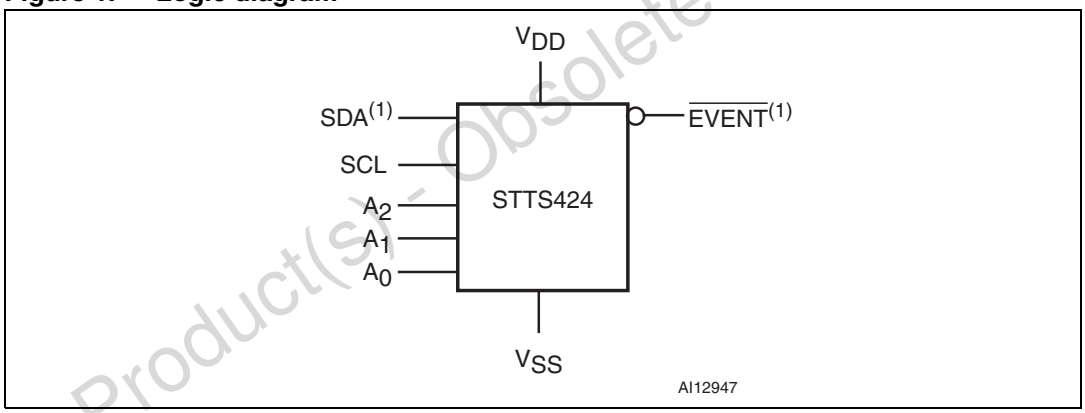
The STTS424 has a simple 2-wire SMBus/I^{2}C-compatible digital serial interface which allows the user to access the data in the temperature register at any time. It communicates via the serial interface with a master controller which operates at speeds of up to 400 kHz. It also gives the user easy access to all of the STTS424 registers in order to customize device operation.

2.1 Device type identifier (DTI) code

The JC42.4 temperature sensor has its own unique I^{2}C address, which ensures that there are no compatibility or data translation issues. The DTI code is the unique 4-bit address, '0011'.

The full I^{2}C address consists of the unique DTI code and 3 bits determined by the A0, A1, and A2 pins. This allows up to 8 unique addresses, hence 8 STTS424 devices may be connected on the same bus.

Figure 1. Logic diagram



1. SDA and $\overline{\text{EVENT}}$ are open drain.

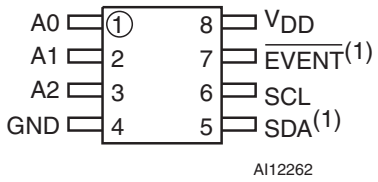
Table 1. Signal names

Pin	Symbol	Description	Direction
1	A0	Serial bus address selection pin. Can be tied to V_{SS} or V_{DD}.	Input
2	A1	Serial bus address selection pin. Can be tied to V_{SS} or V_{DD}.	Input
3	A2	Serial bus address selection pin. Can be tied to V_{SS} or V_{DD}.	Input
4	V_{SS}	Supply ground	
5	SDA(1)	Serial data	Input/output
6	SCL	Serial clock	Input
7	$\overline{\text{EVENT}}$(1)	Event output pin. Open drain and active-low.	Output
8	V_{DD}	Supply power (2.7 V to 3.6 V)	

1. SDA and $\overline{\text{EVENT}}$ are open drain.

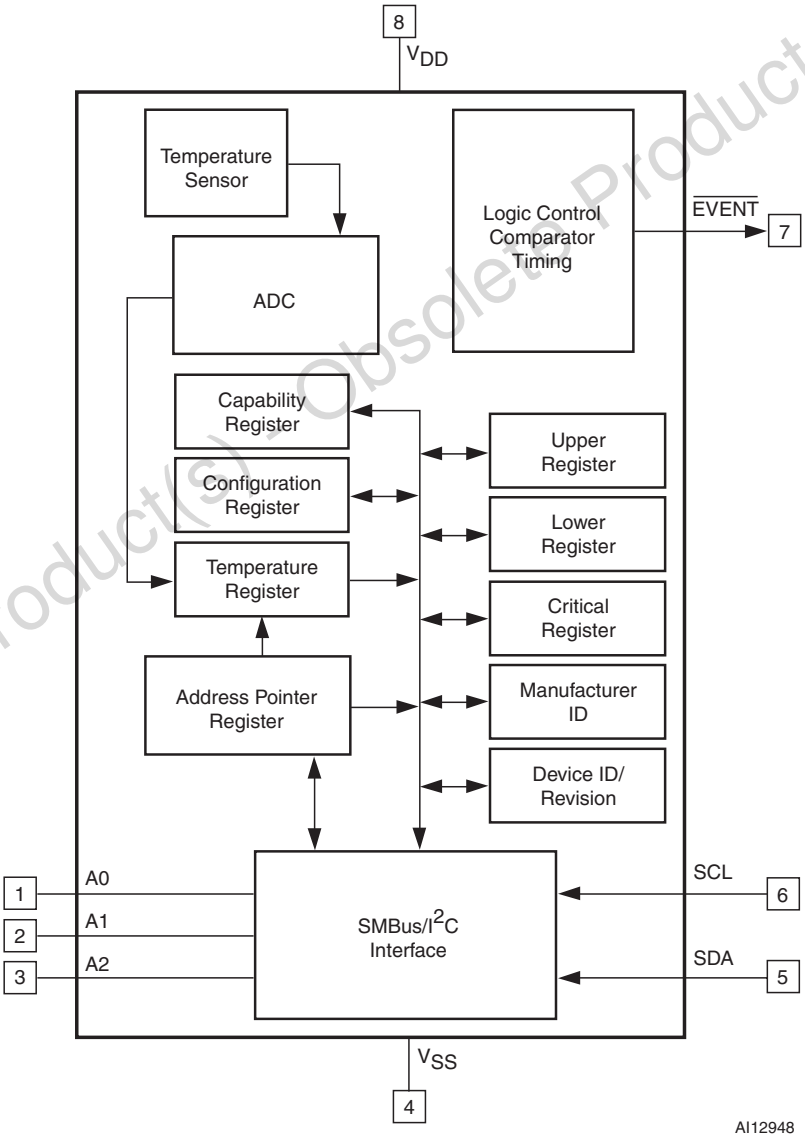
See *Section 2.2: Pin descriptions on page 9* for details.

Figure 2. TDFN8 connections (top view)



1. SDA and $\overline{\text{EVENT}}$ are open drain.

Figure 3. Block diagram



2.2 Pin descriptions

2.2.1 A0, A1, A2

A2, A1, and A0 are selectable address pins for the 3 LSBs of the I^2C interface address. They can be set to V_{DD} or GND to provide 8 unique address selections.

2.2.2 V_{SS} (ground)

This is the reference for the power supply. It must be connected to system ground.

2.2.3 SDA (open drain)

This is the serial data input/output pin.

2.2.4 SCL

This is the serial clock input pin.

2.2.5 $\overline{EVENT}$ (open drain)

This output pin is open drain and active-low and functions as an alert interrupt.

2.2.6 V_{DD} (power)

This is the supply voltage pin, and ranges from +2.7 V to +3.6 V.

3 Operation

The STTS424 TS continuously monitors the ambient temperature and updates the temperature data registers at least eight times per second. Temperature data is latched internally by the device and may be read by software from the bus host at any time.

The SMBus/I^{2}C slave address selection pins allow up to 8 such devices to co-exist on the same bus. This means that up to 8 memory modules can be supported, given that each module has one such slave device address slot.

After initial power-on, the configuration registers are set to the default values. The software can write to the configuration register to set bits per the bit definitions in *Section 3.1: SMBus/I^{2}C communications*.

3.1 SMBus/I^{2}C communications

The registers in this device are selected by the pointer register. At power-up, the pointer register is set to “00”, which is the capability register location. The pointer register latches the last location it was set to. Each data register falls into one of three types of user accessibility:

1. Read-only
2. Write-only and
3. WRITE/READ same address.

A WRITE to this device will always include the address byte and the pointer byte. A WRITE to any register other than the pointer register, requires two data bytes.

Reading this device is achieved in one of two ways:

- If the location latched in the pointer register is correct (most of the time it is expected that the pointer register will point to one of the read temperature registers because that will be the data most frequently read), then the READ can simply consist of an address byte, followed by retrieval of the two data bytes.
- If the pointer register needs to be set, then an address byte, pointer byte, repeat start, and another address byte will accomplish a READ.

The data byte transfers the MSB first. At the end of a READ, this device can accept either an acknowledge (ACK) or no acknowledge (No ACK) status from the master. The No ACK status is typically used as a signal for the slave that the master has read its last byte. This device subsequently takes up to 125 ms to measure the temperature.

Note: STTS424 does not initiate clock stretching which is an optional I^{2}C bus feature.

Figure 4. SMBus/I²C write to pointer register

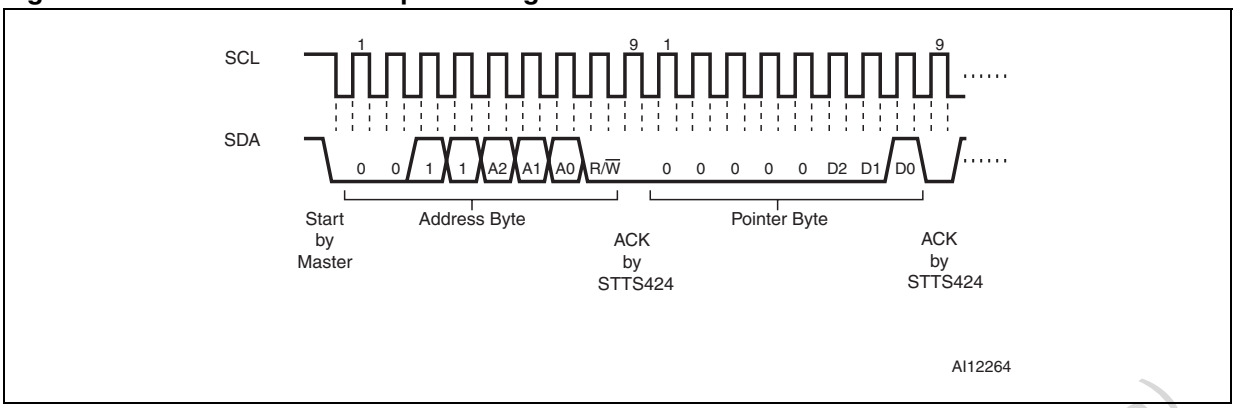


Figure 5. SMBus/I²C write to pointer register, followed by a read data word

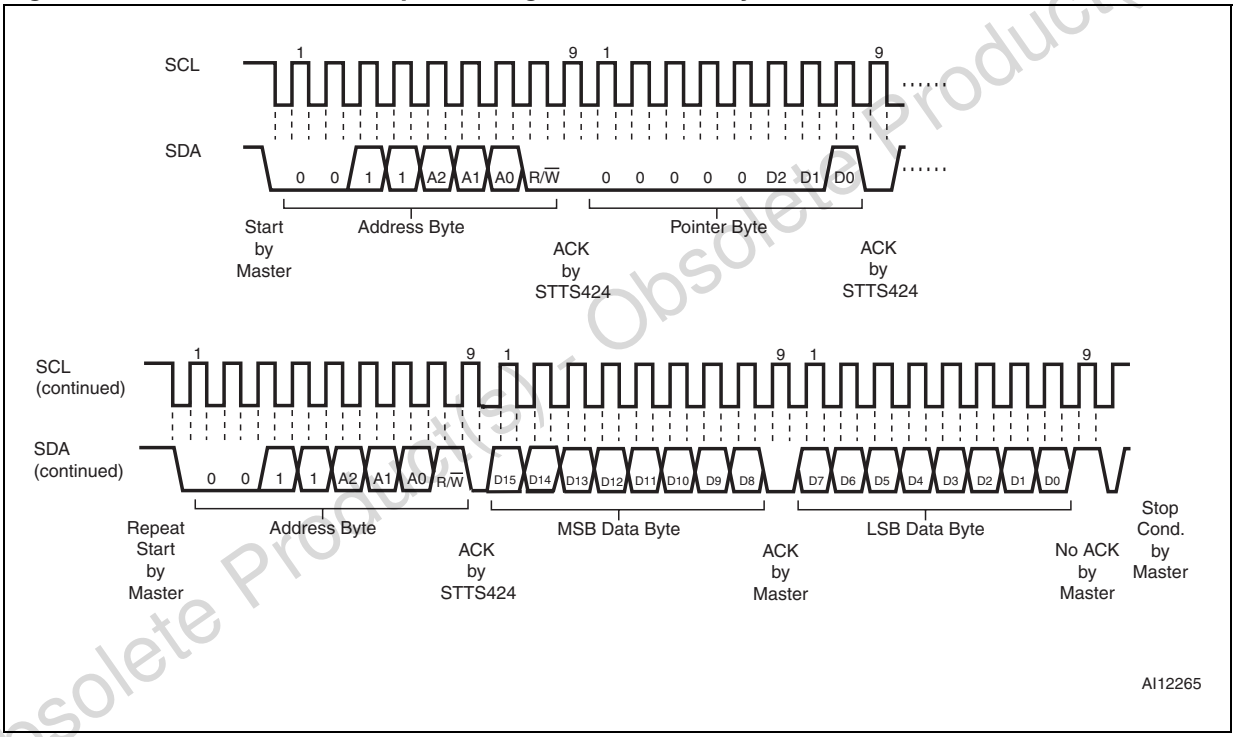
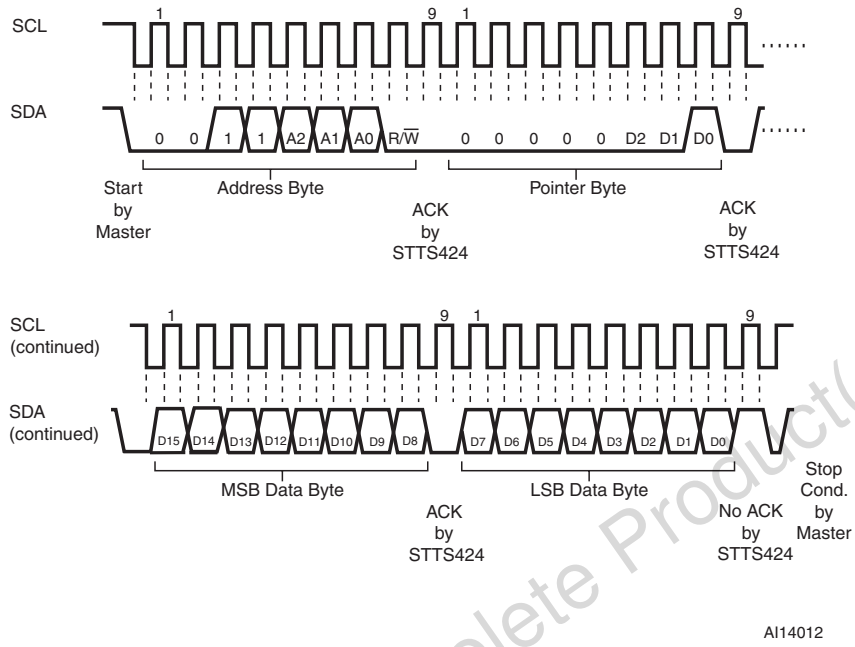


Figure 6. SMBus/I²C write to pointer register, followed by a write data word



3.2 SMBus/I²C slave sub-address decoding

The physical address for the TS is binary 0 0 1 1 A2 A1 A0 RW, whereas A2, A1, and A0 are the three slave sub-address pins, and the LSB “RW” is the READ/WRITE flag.

3.3 SMBus/I²C AC timing consideration

In order for this device to be both SMBus- and I²C-compatible, it complies to a subset of each specification. These interoperability requirements which will enable this device to co-exist with devices on either an SMBus or an I²C bus:

- The SMBus minimum clock frequency is required.
- The 300 ns SMBus data hold time (THD:DAT) is required (see *Figure 7* and *Table 2 on page 13*).
- The SMBus time-out is maximum 50 ms.

Note: Since the voltage levels are specified only within 3.3 V ±10%, there are no compatibility concerns with the SMBus/I²C DC specifications.

Figure 7. SMBus/I²C timing diagram

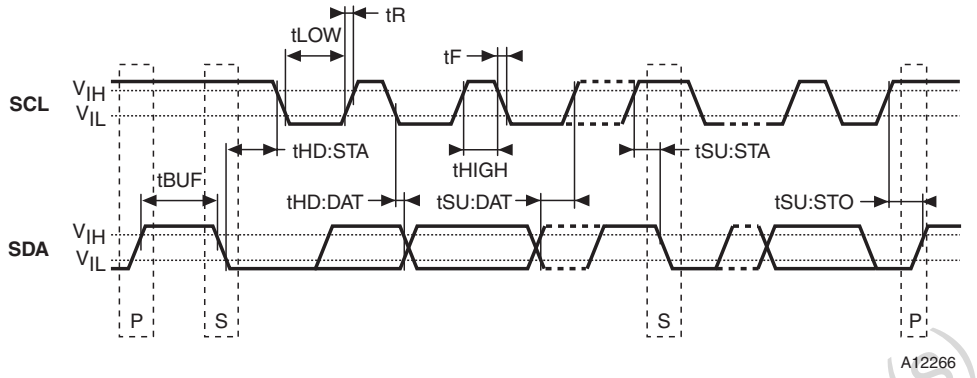


Table 2. AC SMBus and I²C compatibility timings

Symbol	Parameter	Min	Max	Units
t_{BUF}	Bus free time between stop (P) and start (S) conditions	1.3	–	µs
$t_{HD:STA}$	Hold time after (repeated) start condition. After this period, the first clock cycle is generated.	0.6	–	µs
$t_{SU:STA}$ (1)	Repeated start condition setup time	1.3	–	µs
t_{HIGH}	Clock high period	0.6	–	µs
t_{LOW}	Clock low period	1.3	–	µs
t_F	Clock/data fall time	–	300	ns
t_R	Clock/data rise time	–	300	ns
$t_{SU:DAT}$	Data setup time	100	–	ns
$t_{HD:DAT}$	Data hold time	300	–	ns
$t_{SU:STO}$	Stop condition setup time	0.6	–	µs
f_{SCL}	SMBUS/I²C clock frequency	10	400	kHz
$t_{timeout}$	Bus timeout	25	50	ms

1. For a restart condition, or following a WRITE cycle

3.4 SMBus timeout

The STTS424 supports the SMBus timeout feature. If the host holds SCL low for more than 25 ms, the STTS424 resets and releases the bus. This feature is turned on by default.

4 Temperature sensor registers

The temperature sensor component is comprised of various user-programmable registers. These registers are required to write their corresponding addresses to the Pointer register. They can be accessed by writing to their respective addresses (see *Table 3*). Pointer register Bits 7-3 must always be written to '0' (see *Table 4*). This must be maintained, as not setting these bits to '0' may keep the device from performing to specifications.

The main registers include:

- *Capability register (read-only)*
- *Configuration register (read/write)*
- *Temperature register (read-only)*
- *Temperature trip point registers (r/w)*, including
  - Alarm temperature upper boundary,
  - Alarm temperature lower boundary, and
  - Critical temperature.
- *Manufacturer ID register format*
- *Device ID and device revision ID register format*

Note: See Table 5 on page 15 for pointer register selection bit details.

Table 3. Temperature sensor registers summary

Address (Hex)	Register name		Power-on default
Not applicable	Address pointer		Undefined
00	Capability	B-grade only	0x002F
01	Configuration		0x0000
02	Alarm temperature upper boundary trip		0x0000
03	Alarm temperature lower boundary trip		0x0000
04	Critical temperature trip		0x0000
05	Temperature		Undefined
06	Manufacturer's ID		0x104A
07	Device ID/revision		0x0101

Table 4. Pointer register format

MSB							LSB
Bit7	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
0	0	0	0	0	P2	P1	P0
					Pointer/register select bits		

Table 5. Pointer register select bits (type, width, and default values)

P2	P1	P0	Name	Register description		Width (bits)	Type (R/W)	Default state (POR)
0	0	0	CAPA	Thermal sensor capabilities	B-grade only	16	R	00 2F
0	0	1	CONF	Configuration		16	R/W	00 00
0	1	0	UPPER	Alarm temperature upper boundary		16	R/W	00 00
0	1	1	LOWER	Alarm temperature lower boundary		16	R/W	00 00
1	0	0	CRITICAL	Critical temperature		16	R/W	00 00
1	0	1	TEMP	Temperature		16	R	00 00
1	1	0	MANU	Manufacturer ID		16	R	104A
1	1	1	ID	Device ID/revision		16	R	01 01

4.1 Capability register (read-only)

This 16-bit register is read-only, and provides the TS capabilities which comply with the minimum JEDEC 424.4 specifications (see *Table 6* and *Table 7 on page 16*). The STTS424 provides temperatures at 0.25 resolution (10-bit).

4.1.1 Alarm window trip

The device provides a comparison window with an upper temperature trip point in the alarm upper boundary register, and a lower trip point in the alarm lower boundary register. When enabled, the event output will be triggered whenever entering or exiting (crossing above or below) the alarm window.

4.1.2 Critical trip

The device can be programmed in such a way that the event output is only triggered when the temperature exceeds the critical trip point. The critical temperature setting is programmed in the critical temperature register. When the temperature sensor reaches the critical temperature value in this register, the device is automatically placed in comparator mode, which means that the critical event output cannot be cleared by using software to set the clear event bit.

Table 6. Capability register format

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
Bit7	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
RFU	RFU	V_{HV}	TRES1	TRES0	Wider range	Higher precision	Alarm and critical trips

Table 7. Capability register bit definitions

Bit	Definition
0	Basic capability – 0 = Alarm and critical trips turned OFF. – 1 = Alarm and critical trips turned ON.
1	Accuracy – 0 = Accuracy ±2°C over the active range and ±3°C over the monitoring range (C - Grade). – 1 = High accuracy ±1°C over the active range and ±2°C over the monitoring range (B - Grade).
2	Range width – 0 = Values lower than 0°C will be clamped and represented as binary value '0'. – 1 = Temperatures below 0°C can be read and the Sign bit will be set accordingly.
4:3	Temperature resolution – 01 = This 10-bit value is fixed for STTS424, providing temperatures at 0.25°C resolution (LSB).
5	(V_{HV}) High voltage support for A0 (pin 1) – 1 = STTS424 supports a voltage up to 10 volts on the A0 pin (default).
15:6	Reserved These values must be set to '0'.

4.2 Configuration register (read/write)

The 16 bit Configuration register stores various configuration modes that are used to set up the sensor registers and configure according to application and JEDEC 42.4 requirements (see *Table 8 on page 17* and *Table 9 on page 18*).

4.2.1 Event thresholds

All event thresholds use hysteresis as programmed in register address 0x01 (bits 10 through 9) to be set when they de-assert.

4.2.2 Interrupt mode

The interrupt mode allows an event to occur where software may write a '1' to the clear event bit (bit 5) to de-assert the event Interrupt output until the next trigger condition occurs.

4.2.3 Comparator mode

Comparator mode enables the device to be used as a thermostat. READs and WRITEs on the device registers will not affect the event output in comparator mode. The event signal will remain asserted until temperature drops outside the range or is re-programmed to make the current temperature “out of range”.

4.2.4 Shutdown mode

The STTS424 features a shutdown mode which disables all power-consuming activities (e.g. temperature sampling operations), and leaves the serial interface active. This is selected by setting shutdown bit (bit 8) to '1'. In this mode, the devices consume the minimum current (I_{SHDN}), as shown in *Table 22 on page 28*.

Note: Bit 8 cannot be set to '1' while bits 6 and 7 (the lock bits) are set to '1'.

The device may be enabled for continuous operation by clearing bit 8 to '0'. In shutdown mode, all registers may be read or written to. Power recycling will also clear this bit and return the device to continuous mode as well.

Table 8. Configuration register format

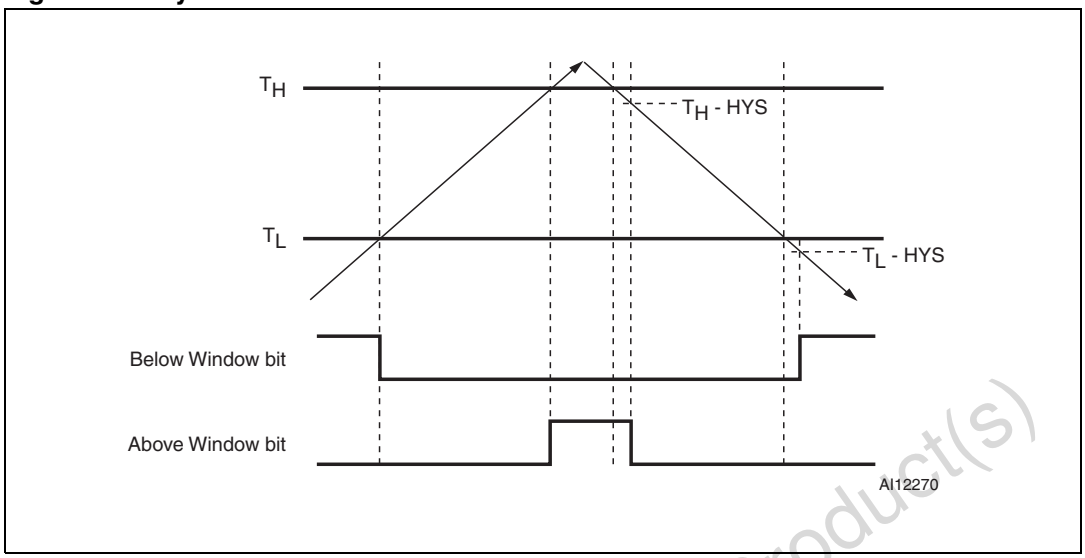
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
RFU	RFU	RFU	RFU	RFU	Hysteresis	Hysteresis	Shutdown mode
Bit7	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
Critical lock bit	Alarm lock bit	Clear event	Event output status	Event output control	Critical event only	Event polarity	Event mode

Table 9. Configuration register bit definitions

Bit	Definition
0	Event mode – 0 = Comparator output mode (this is the default) – 1 = Interrupt mode; when either of the lock bits is set, this bit cannot be altered until it is unlocked.
1	Event polarity – 0 = Active-low (this is the default). – 1 = Active-high; when either of the lock bits is set, this bit cannot be altered until it is unlocked.
2	Critical event only – 0 = Event output on alarm or critical temperature event (this is the default). – 1 = Event only if the temperature is above the value in the critical temperature register; when the alarm window lock bit is set, this bit cannot be altered until it is unlocked.
3	Event output control – 0 = Event output disabled (this is the default). – 1 = Event output enabled; when either of the lock bits is set, this bit cannot be altered until it is unlocked.
4	Event status (read-only)(1) – 0 = Event output condition is not being asserted by this device. – 1 = Event output condition is being asserted by this device via the alarm window or critical trip event.
5	Clear event (write-only)(2) – 0 = No effect – 1 = Clears the active Event in Interrupt mode.
6	Alarm window lock bit – 0 = Alarm trips are not locked and can be altered (this is the default). – 1 = Alarm trip register settings cannot be altered. This bit is initially cleared. When set, this bit returns a logic '1' and remains locked until cleared by an internal power-on reset. These bits can be written to with a single WRITE, and do not require double WRITEs.
7	Critical trip lock bit – 0 = Critical trip is not locked and can be altered (this is the default). – 1 = Critical trip register settings cannot be altered. This bit is initially cleared. When set, this bit returns a logic '1' and remains locked until cleared by an internal power-on reset. These bits can be written to with a single WRITE, and do not require double WRITEs.
8	Shutdown mode – 0 = TS is enabled (this is the default). – 1 = Shutdown TS when the shutdown, device, and A/D converter are disabled in order to save power. No event conditions will be asserted; when either of the lock bits is set, this bit cannot be altered until it is unlocked. However, it can be cleared at any time.
10:9	Hysteresis enable(3) (see *Figure 8* and *Table 10*) – 00 = Hysteresis is disabled. – 01 = Hysteresis is enabled at 1.5°C. – 10 = Hysteresis is enabled at 3°C. – 11 = Hysteresis is enabled at 6°C.

1. The actual incident causing the event can be determined from the read temperature register. Interrupt events can be cleared by writing to the clear event bit (writing to this bit will have no effect on overall device functioning.
2. Writing to this register has no effect on overall device functioning in comparator mode. When read, this bit will always return a logic '0' result.
3. Hysteresis is also applied to the $\overline{\text{EVENT}}$ pin functionality. When either of the lock bits is set, these bits cannot be altered.

Figure 8. Hysteresis



1. T_U = Value stored in the alarm temperature upper boundary trip register.
2. T_L = Value stored in the alarm temperature lower boundary trip register.
3. Hys = Absolute value of selected hysteresis.

Table 10. Hysteresis as applied to temperature movement

	Below alarm window bit		Above alarm window bit	
	Temperature slope	**Temperature threshold**	**Temperature slope**	**Temperature threshold**
Sets	Falling	T_L - HYS	Rising	T_H
Clears	Rising	T_L	Falling	T_H - HYS

4.2.5 Event output pin functionality

The $\overline{\text{EVENT}}$ pin is an open drain output and requires a pull-up resistor to V_{DD} on the system motherboard or incorporated into the master controller.

Figure 9 shows the defined outputs of the $\overline{\text{EVENT}}$ correspondent to the temperature change.

The event outputs can be programmed to be configured as either a comparator output or as an interrupt. This is done by enabling the output control bit (bit 3) and setting the event mode bit (bit 0). The output pin polarity can also be specified as active-high or active-low by setting the event polarity bit (bit 1).

When the hysteresis bit (bits 10 and 9) is enabled, hysteresis may be used to sense temperature movement around trigger points. For example, when using the “above alarm window” bit (temperature register bit 14, see *Table 12 on page 22*) and hysteresis is set to 3°C, as the temperature rises, bit 14 is set (bit 14 = 1). The temperature is above the alarm window and the temperature register contains a value that is greater than the value set in the alarm temperature upper boundary register (see *Table 15 on page 23*).

If the temperature decreases, bit 14 will remain set until the measured temperature is less than or equal to the value in the alarm temperature upper boundary register minus 3°C (see *Figure 8 on page 19* and *Table 10 on page 19* for details.

Similarly, when using the “below alarm window” bit (temperature register bit 13, see *Table 12 on page 22*) will be set to '0'. The temperature is equal to or greater than the value set in the alarm temperature lower boundary register (see *Table 16 on page 24*). As the temperature decreases, bit 13 will be set to '1' when the value in the temperature register is less than the value in the alarm temperature lower boundary register minus 3°C (see *Figure 8 on page 19* and *Table 10 on page 19* for details).

The device will retain the previous state when entering the shutdown mode. If the device enters the shutdown mode while the $\overline{\text{EVENT}}$ pin is low, the shutdown current will increase due to the additional event output pull-down current.

If in interrupt mode and the temperature reaches the critical temperature, the $\overline{\text{EVENT}}$ pin remains asserted until the temperature drops below the critical limit minus hysteresis.

Note: Hysteresis is also applied to the $\overline{\text{EVENT}}$ pin functionality. When either of the lock bits (bits 6 or 7) is set, these bits cannot be altered.

Figure 9. Event output boundary timings

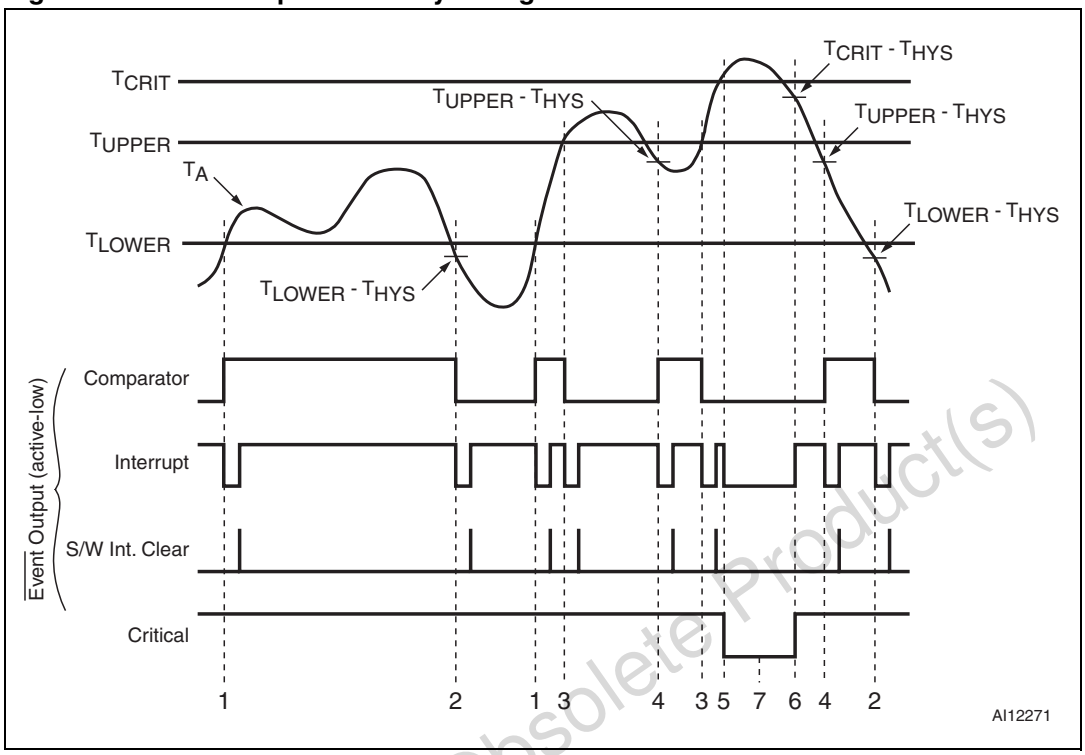


Table 11. Legend for *Figure 9: Event output boundary timings*

Note	Event output boundary conditions	Event output			T_A bits		
		Comparator	Interrupt	Critical	15	14	13
1	$T_A \geq T_{LOWER}$	H	L	H	0	0	0
2	$T_A \geq T_{LOWER} - T_{HYS}$	L	L	H	0	0	1
3	$T_A > T_{UPPER}$	L	L	H	0	1	0
4	$T_A \geq T_{UPPER} - T_{HYS}$	H	L	H	0	0	0
5	$T_A \geq T_{CRIT}$	L	L	L	1	1	0
6	$T_A < T_{CRIT} - T_{HYS}$	L	H	H	0	1	0
7	When $T_A \geq T_{CRIT}$ and $T_A < T_{CRIT} - T_{HYS}$, the event output is in comparator mode and bit 0 of the configuration register (interrupt mode) is ignored.						

Note: Systems that use the active high mode for event output must be wired pont-to-point between the STTS424 and the sensing controller. Wire-OR configurations should not be used with active high EVENT since any device pulling the event output signal low will mask the other devices on the bus. Also note that the normal state of $\overline{EVENT}$ in active high mode is a '0' which will constantly draw power through the pull-up resistor.

4.3 Temperature register (read-only)

This 16-bit, read-only register stores the temperature measured by the internal band gap TS as shown in *Table 12*. The STTS424 meets the JEDEC JC42.4 mandatory 0.25°C resolution requirement. When reading this register, the MSBs (bit 15 to bit 8) are read first, and then the LSBs (bit 7 to bit 0) are read. The result is the current-sensed temperature. The data format is 2s complement with one LSB = 0.25°C. The MSB has a 128°C resolution.

The trip status bits represent the internal temperature trip detection, and are not affected by the status of the event or configuration bits (e.g. event output control or clear event). If neither of the above or below values are set (i.e. both are 0), then the temperature is exactly within the user-defined alarm window boundaries.

4.3.1 Temperature format

The 16-bit value used in the trip point set and temperature read-back registers is 2s complement, with the LSB equal to 0.0625°C (see *Table 13*). For example:

1. a value of 019Ch will represent 25.75°C,
2. a value of 07C0h will represent 124°C, and
3. a value of 1E74h will represent –24.75°C

The 0.0625°C resolution is optional. Supporting a resolution of at least 0.25°C is mandatory. All unused resolution bits will be set to zero. The MSB will have a resolution of 128°C. The STTS424 supports the 0.25°C/LSB only.

The upper 3 bits indicate trip status based on the current temperature, and are not affected by the event output status.

Table 12. Temperature register format

			Sign MSB									LSB			
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	
Above critical input(1)	Above alarm window(1)	Below alarm window(1)	Temperature											0	0	
Flag bits			Example hex value of 07C0 corresponds to 124°C (10-bit)													
0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	07C0 h
Flag bits			Example hex value of 1C00 corresponds to –40°C (10-bit)													
0	0	0	1	1	1	0	1	1	0	0	0	0	0	0	0	1C00 h

1. See *Table 13* for explanation.

Table 13. Temperature register bit definitions

Bit	Definition with hysteresis = 0
13	Below (temperature) alarm window – 0 = Temperature is equal to or above the alarm window lower boundary temperature. – 1 = Temperature is below the alarm window.
14	Above (temperature) alarm window – 0 = Temperature is equal to or below the alarm window upper boundary temperature. – 1 = Temperature is below the alarm window.
15	Above critical trip – 0 = Temperature is below the critical temperature setting. – 1 = Temperature is equal to or above the critical temperature setting.

4.4 Temperature trip point registers (r/w)

The STTS424 alarm mode registers provide for 11-bit data in 2s compliment format. The data provides for one LSB = 0.25°C. All unused bits in these registers are read as '0'.

The STTS424 has three temperature trip point registers (see *Table 14*):

- Alarm temperature upper boundary threshold (*Table 15*),
- Alarm temperature lower boundary threshold (*Table 16*), and
- Critical temperature trip point value (*Table 17*).

Note: If the upper or lower boundary threshold values are being altered in-system, all interrupts should be turned off until a known state can be obtained to avoid superfluous interrupt activity.

Table 14. Temperature trip point register format

P2	P1	P0	Name	Register description	Width (bits)	Type (R/W)	Default state (POR)
0	1	0	UPPER	Alarm temperature upper boundary	16	R/W	00 00
0	1	1	LOWER	Alarm temperature lower boundary	16	R/W	00 00
1	0	0	CRITICAL	Critical temperature	16	R/W	00 00

Table 15. Alarm temperature upper boundary register format

			Sign MSB									LSB		
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	Alarm window upper boundary temperature											0	0

Table 16. Alarm temperature lower boundary register format

			Sign MSB									LSB		
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0	0	0	Alarm window lower boundary temperature											0	0

Table 17. Critical temperature register format

			Sign MSB									LSB		
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0	0	0	Critical temperature trip point											0	0

4.5 Manufacturer ID register (read-only)

The manufacturer's ID (programmed value 104Ah) in this register is the STMicroelectronics identification provided by the Peripheral Component Interconnect Special Interest Group (PCiSIG).

Table 18. Manufacturer ID register format

Bit15	**Bit14**	**Bit13**	**Bit12**	**Bit11**	**Bit10**	**Bit9**	**Bit8**
0	0	0	1	0	0	0	0
Bit7	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
0	1	0	0	1	0	1	0

4.6 Device ID and device revision ID register (read-only)

The device IDs and device revision IDs are maintained in this register. The register format is shown in *Table 19*. The device IDs and device revision IDs are currently '0' and will be incremented whenever an update of the device is made.

Table 19. Device ID and device revision ID register format

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
0	0	0	0	0	0	0	1
Device ID							
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	0	0	0	0	0	1
Device revision ID							