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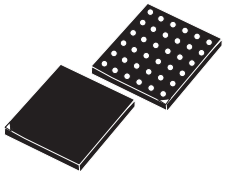
STULPI01A, STULPI01B

High-speed USB On-The-Go ULPI transceiver

Datasheet – production data

Features

- USB-IF high-speed certified to the universal serial bus specification rev. 2.0
- Meets the requirements of the universal serial bus specification rev. 2.0, On-The-Go supplement to the USB 2.0 specification 1.0a and ULPI transceiver specification 1.1
- Standard ULPI (UTMI+ low pin interface) 1.1 digital interface
- Fully compliant with ULPI 1.1 register set
- External square wave clock with V_{DVIO} amplitude must be applied to oscillator input XI
- Supports 480 Mbit/s High-speed, 12 Mbit/s Full-speed and 1.5 Mbit/s Low-speed modes of operation
- Supports 2.7 V UART mode
- Supports session request protocol (SRP) and host negotiation protocol (HNP) for dual-role device features
- Ability to control external charge pump for higher VBUS currents
- Single supply, +3 V to +4.5 V voltage range
- Integrated dual voltage regulator to supply internal circuits with stable 3.3 V and 1.2 V
- Integrated overcurrent detector
- Integrated HS termination and FS/LS/OTG pull-up/pull-down resistors
- Integrated USB 2.0 “short-circuit withstand” protection
- Power-down mode with very low-power consumption for battery-powered devices
- Ideal for system ASICs with built-in USB host, device or OTG cores
- Available in µTFBGA36 RoHS package
- –40 to 85 °C operating temperature range



µTFBGA36

Applications

- Mobile phones
- PDAs
- MP3 players
- Digital still cameras
- Set-top box
- Portable navigation devices

Description

The STULPI01 is a high-speed USB 2.0 transceiver compliant with ULPI (UTMI+ low pin interface) and OTG (On-The-Go) specifications, providing a complete physical layer solution for any high-speed USB host, device or OTG dual-role core. It allows USB ASICs to interface with the physical layer of the USB through a 12-pin interface. It contains VBUS comparators, an ID line detector, USB differential drivers and receivers and a complete ULPI register map and interrupt generator. The STULPI01 transceiver is suitable for mobile applications and battery-powered devices because of its low-power consumption, Power-down operating mode and minimal die/package dimensions.

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1 Application diagrams

Figure 1. Peripheral only, configuration with external clock

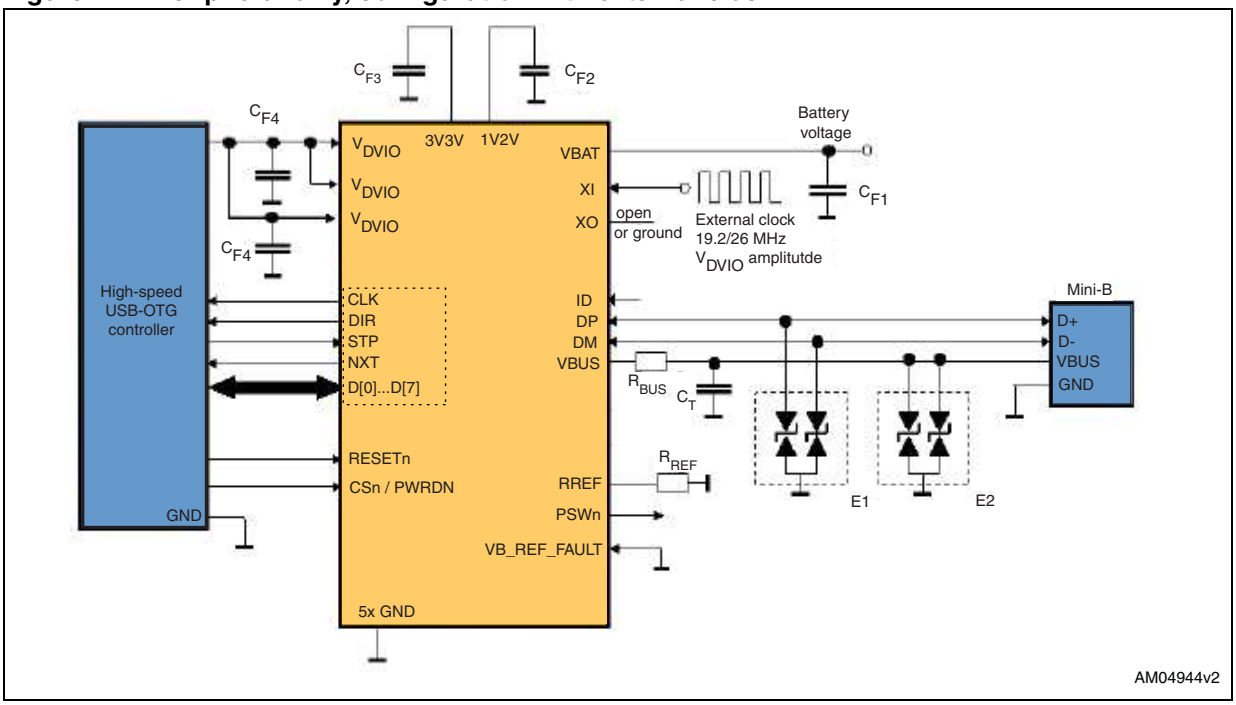
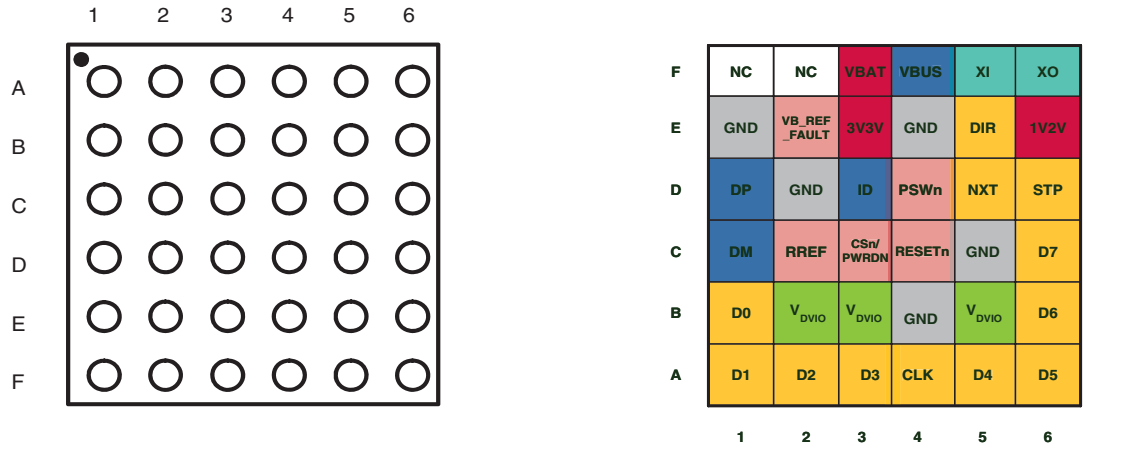


Table 1. Bill of materials - external components

Qty.	Symbol	Value	Description
1	C_{F1}	0.1 - 1 µF	Filtering capacitor. Suggested components: Murata 10 V X5R (GRM188R61A105KA61) or Murata 10 V Y5V (GRM188F51A105ZA01) or TAIYO YUDEN 25 V X5R (TMK107BJ105KA)
2	C_{F4}	0.1 - 1 µF	Filtering capacitor. Suggested components: Murata 10 V X5R (GRM188R61A105KA61) or Murata 10 V Y5V (GRM188F51A105ZA01) or TAIYO YUDEN 25 V X5R (TMK107BJ105KA)
1	C_{F2}	1 µF - 1.5 µF	Filtering capacitor. Suggested components: Murata 10 V X5R (GRM188R61A105KA61) or Murata 10 V Y5V (GRM188F51A105ZA01) or TAIYO YUDEN 25 V X5R (TMK107BJ105KA)
1	C_{F3}	1 - 4.7 µF	Filtering capacitor. Suggested components: Murata 10 V Y5V (GRM188F51A475ZE20) or TAIYO YUDEN 6.3 V X5R (JMK107BJ475KA)
1	C_T	4.7 µF	Tank capacitor
1	R_{REF}	12 kΩ	Reference resistor ±1%
1	E1		USBULC6-2F3
1	E2		ESDA14V2-2BF3
1	R_{BUS}	2.2 kΩ	Series overvoltage protection resistor

2 Bump configuration

Figure 2. Pin connections



µTFBGA36 (through top side view)

µTFBGA36 (bottom view)

AM04945v1

Table 2. Pinout and bump description

Bump	Symbol	Type	Description
B1	D0	I/O	Data bit [0] (V_{DVIO} referred). UART TXD signal.
A1	D1	I/O	Data bit [1] (V_{DVIO} referred). UART RXD signal.
A2	D2	I/O	Data bit [2] (V_{DVIO} referred). UART reserved pin.
A3	D3	I/O	Data bit [3] (V_{DVIO} referred). UART active high interrupt indication.
A4	CLK	O	Clock out (V_{DVIO} referred)
A5	D4	I/O	Data bit [4] (V_{DVIO} referred)
A6	D5	I/O	Data bit [5] (V_{DVIO} referred)
B6	D6	I/O	Data bit [6] (V_{DVIO} referred)
C6	D7	I/O	Data bit [7] (V_{DVIO} referred)
D6	STP	I	ULPI stop signal (V_{DVIO} referred)
D5	NXT	O	ULPI next signal (V_{DVIO} referred)
E5	DIR	O	ULPI direction signal (V_{DVIO} referred)
C3	CSn/PWRDN	I	Chip select active low, power-down active high
C4	RESETn	I	Active low asynchronous reset
D1	DP	I/O	Positive data line of the USB. 5 V tolerant.
C1	DM	I/O	Negative data line of the USB. 5 V tolerant.
D3	ID	I	ID pin of the USB connector for initial device role selection. 5 V tolerant.
F4	VBUS	I/O	V_{BUS} line of the USB interface, requires an external capacitor of 4.7 µF.

Table 2. Pinout and bump description (continued)

Bump	Symbol	Type	Description
F1	NC		Not connected
F2	NC		Not connected.
E2	VB_REF_FAULT	I	Voltage reference for internal OC detector input or digital input from external OC detector (V_{3V3V} referred). 5 V tolerant.
D4	PSWn	O	External charge pump control, active low. 5 V tolerant, open drain.
F5	XI	I	External clock input (V_{DVIO} referred).
F6	XO	O	XO pin must be left floating or grounded (crystal is not supported).
F3	VBAT	PWR	Battery power input for the LDO (3 V – 4.5 V). Bypass V_{BAT} to GND with a 1 µF capacitor.
E3	3V3V	PWR	3.3 V LDO output. Bypass 3V3V to GND with a 1.5 µF capacitor.
E6	1V2V	PWR	1.2 V LDO output. Bypass 1V2V to GND with a 1.5 µF capacitor.
C2	RREF	I/O	Reference resistor (12 kΩ ±1%)
B2/B3/B5	V_{DVIO}	PWR	Digital I/O supply voltage. Bypass each V_{DVIO} to GND with a 100 nF-1 µF capacitor. Balls B2-B5 can share common capacitor.
C5/D2	GND	PWR	Ground
B4/E4/E1	GND	PWR	Ground

3 Maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DVIO}	Digital I/O supply voltage	-0.3 to +4.0	V
V_{1V2}	Digital core supply voltage (provided internally by LDO)	-0.3 to +1.4	V
V_{3V3}	Analog supply voltage (provided internally by LDO)	-0.3 to +4.0	V
V_{BAT}	Battery supply voltage	-0.3 to +7.0	V
V_{DCDIG}	DC voltage on digital pins (CLK, DIR, STP, NXT, D[0-7], RESETn, XI, CSn/PWRDN)	-0.3 to +4.0	V
V_{DCVBUS}	DC voltage on 5 V tolerant pins (VBUS,VB_REF_FAULT, DP, DM, ID)	-0.3 to +5.5	V
T_{STG}	Storage temperature range	-40 to +125	°C
$V_{ESD-HBM}$	Electrostatic discharge voltage on all pins (according to JESD22-A114-B)	±2.0	kV

Note: Absolute maximum ratings are those values above which damage to the device may occur. Functional operation under these conditions is not implied. All voltages are referenced to GND.

Table 4. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction-ambient (simulated value as per JEDEC JSD51)	113.8	°C/W
R_{thJC}	Thermal resistance junction-case (simulated value as per JEDEC JSD51)	47	°C/W
R_{thJB}	Thermal resistance junction-base (simulated value as per JEDEC JSD51)	66.2	°C/W

Table 5. Recommended operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{BAT}	Battery supply voltage	3.0	3.6	4.5	V
V_{DVIO}	Digital I/O supply voltage	1.65	1.80	3.6	V
T_A	Operating temperature range	-40		+85	°C
C_T	Tank capacitor	1	4.7	6.5	µF
R_{REF}	External reference resistor	11.88	12	12.12	kΩ
XTAL	External square wave (01A, 01B versions)	19.2 or 26			MHz
	Recommended rise/fall time	4			ns

4 Electrical characteristics

Table 6. Electrical characteristics

Symbol	Parameter	Test conditions[1]	Min.	Typ.	Max.	Unit
Power consumption						
I_{BAT}	Supply current	Active mode (USB bus idle)		15		mA
		Active mode (FS transmission, 12 Mb/s traffic)			30	mA
		Active mode (HS transmission)			50	mA
		Suspend mode (not including DP pull-up current, external clock stopped)		120		µA
		UART mode (no transmission)		15		mA
		Power-down mode		0.4	2	µA
		VIO OFF mode (V_{DVIO} = 0)		0.4	2	µA
I_{DVIO}	ULPI bus supply current V_{DVIO}	Power-down mode		0.1	10	µA
		Active mode, 4 pF load		1.8		mA
Logic inputs and outputs						
C_{ULPIIN}	ULPI port I/O capacitance			2.4	3.5	pF
V_{OH}	High level output voltage (ULPI bus)	I_{OH} = -2 mA	V_{DVIO} -0.15			V
V_{OL}	Low level output voltage (ULPI bus)	I_{OL} = +2 mA			0.15	V
I_{OZH_PSWn}	High level output leakage (PSWn)	V_{OH_PSWn} = 3.3 V power switch disabled			1.0	µA
V_{OL_PSWn}	Low level output voltage (PSWn)	I_{OL} = +2 mA power switch enabled			0.15	V
V_{IH}	High level input voltage (ULPI port and RESETn)		0.65 x V_{DVIO}			V
V_{IL}	Low level input voltage (ULPI port and RESETn)				0.35 x V_{DVIO}	V
I_{IH}	High level input leakage current	V_{IH} = V_{DVIO} -0.2 V			±1.0	µA

Table 6. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{IL}	Low level input leakage current	V_{IL} = 0.2 V			±1.0	µA
V_{PDH}	High level input voltage (CSn/PWRDN pin)	V_{BAT} = 3.0 V to 4.5 V	1.4			V
V_{PDL}	Low level input voltage (CSn/PWRDN pin)	V_{BAT} = 3.0 V to 4.5 V			0.4	V
I_{PDH}	High level input leakage current (CSn/PWRDN pin)	V_{PD} = 1.4 V, V_{BAT} = 4.5 V			±1.0	µA
I_{PDL}	Low level input leakage current (CSn/PWRDN pin)	V_{PD} = 0.4 V, V_{BAT} = 4.5 V			±1.0	µA
V_{FAULTH}	High level input voltage (VB_REF_FAULT pin)	Overcurrent_PD bit is set	0.65 x V_{3V3}			V
V_{FAULTL}	Low level input voltage (VB_REF_FAULT pin)	Overcurrent_PD bit is set			0.15 x V_{3V3}	V
$R_{IN\_VB\_REF}$	VB_REF_FAULT pin input resistance		112	148	168	kΩ
$V_{XI\_HYST\_EXT}$	External clock input hysteresis	XO = ‘0’ at reset		500		mV
V_{XIH}	High level input voltage (XI pin)	XO = ‘0’ at reset	0.65 x V_{DVIO}			V
V_{XIL}	Low level input voltage (XI pin)	XO = ‘0’ at reset			0.15 x V_{DVIO}	V
VBUS						
V_{BUS_LKG}	V_{BUS} leakage voltage	No load			200	mV
R_{VBUS}	V_{BUS} input impedance		40		100	kΩ
V_{BUS_VLD}	V_{BUS} valid comparator threshold	1 kΩ series resistors	4.4	4.75		V
V_{SESS_VLD}	Session valid comparator threshold for both A and B device	Low to high transition	0.8	1.45	2.0	V
		High to low transition		1.25		V
V_{SESS_END}	Session end comparator threshold		0.2		0.8	V
R_{VBUS_PU}	V_{BUS} charge pull-up resistance		650	950	1150	Ω
R_{VBUS_PD}	V_{BUS} discharge pull-down resistance		800	1250	1500	Ω

Table 6. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Overcurrent detector						
V_{OC}	Overcurrent trip threshold VB_REF_FAULT – VBUS	V_{OC} = VB_REF_FAULT – VBUS	20	45	95	mV
ID						
I_{ID_PU}	ID pin pull-up current	V_{ID} = 0 V		70		µA
R_{ID_GND}	ID line short resistance to detect ID GND state				1	kΩ
R_{ID_FLOAT}	ID line short resistance to detect ID FLOAT state		100			kΩ
UART mode (2.7 V ± 5%)						
V_{OH_UART}	High level output voltage (D1, D3)	I_{OH} = -2 mA	V_{DVIO} - 0.15			V
V_{OL_UART}	Low level output voltage (D1, D3)	I_{OL} = +2 mA			0.15	V
$V_{IH\_UART\_D0}$	High level input voltage (D0)		0.65 x V_{DVIO}			V
$V_{IL\_UART\_D0}$	Low level input voltage (D0)				0.35 x V_{DVIO}	V
V_{OH_DFMS}	High level output voltage (DP)	I_{OH} = -2 mA	2.16		2.85	V
V_{OL_DFMS}	Low level output voltage (DP)	I_{OL} = +2 mA, Pull-up = 10 kΩ	-0.10		0.37	V
V_{IH_DTMS}	High level input voltage (DM)		2.0		3.0	V
V_{IL_DTMS}	Low level input voltage (DM)		-0.3		0.81	V
Full-speed/low-speed driver						
Z_{DRV}	Output impedance (acting also as high-speed termination)		40.5		49.5	Ω
V_{OH_DRV}	High level output voltage	R_{LH} = 14.25 kΩ	2.8		3.6	V
V_{OL_DRV}	Low level output voltage	R_{LL} = 1.425 kΩ	0.0		0.3	V
V_{CRS}	Driver crossover voltage	C_{LOAD} = 50 to 600 pF (2)	1.3	1.67	2.0	V
High-speed driver						
V_{HSOI}	HS idle level		-10		10	mV
V_{HSDPJ}	HS data DP J state level	(2)	380		440	mV
V_{HSDK}	HS data DP K state level		-10		10	mV

Table 6. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{HSDNJ}	HS data DN J state level	(2)	380		440	mV
V_{HSDNK}	HS data DN K state level		-10		10	mV
V_{CHIRPJ}	Chirp J level (differential voltage)	(2)	700		1100	mV
V_{CHIRPK}	Chirp K level (differential voltage		-900		-500	mV
Full-speed/Low-speed receivers						
V_{DI}	Diff. receiver input sensitivity (V_{DP}-V_{DM})	V_{CM} = 0.8 to 2.5 V	200			mV
V_{SE_TH}	SE receivers switching threshold	Low to high transition	0.8	1.6	2.0	V
		High to low transition	0.8	1.1	2.0	V
R_{INP}	Input resistance	PU/PD resistors deactivated	300			kΩ
C_{IN}	Input capacitance	(2)			5	pF
Δ_{CIN}	Difference in capacitance between DP and DM input				10	%
V_{DT_LKG}	Data line leakage voltage	R_{PU_EXT} = 300 kΩ			342	mV
High-speed receiver						
V_{HSSQ}	HS squelch detector threshold		100		150	mV
V_{HSDSC}	HS disconnect detection threshold		525		625	mV
V_{HSCM}	HS data signaling common mode volt. range	(2)	-50		500	mV
V_{HSTERM}	Termination voltage in HS	(2)	-10		10	mV
Data pull-up/pull-down resistors						
R_{PU}	Data line pull-up resistance (DP, DM)		1.425			kΩ
V_{IHZ}	FS idle high level voltage		2.7			V
R_{PD}	Data line pull-down resistance (DP, DM)		14.25		24.8	kΩ
Voltage regulator						
3V3V	3.3 V internal power supply voltage	V_{BAT} = 3.6 V, Active mode	3.26	3.4	3.54	V
1V2V	1.2 V internal power supply voltage	V_{BAT} = 3.6 V, Active mode	1.187	1.25	1.31	V

1. Characteristics measured over recommended operating conditions unless otherwise noted. All typical values are referred to T_A = 25 °C, V_{DVIO} = 1.8 V, V_{BAT} = 3.6 V, R_{REF} = 12 kΩ, C_T = 4.7 µF.
2. Guaranteed by design.

Table 7. Switching characteristics

Symbol	Parameter	Test conditions[1]	Min.	Typ.	Max.	Unit
Reset						
$t_{RESETEXT}$	Width of reset pulse on RESETn pin		10			µs
UART mode						
t_{RISE}	Switching time (max. low to min. high)	C_{LOAD} = 185 pF			215	ns
t_{FALL}	Switching time (min. high to max. low)	C_{LOAD} = 185 pF			215	ns
t_{PD_RX}	Delay time (50% DM to 50% D1)	C_L = 10 pF			60	ns
t_{PD_TX}	Delay time (50% D0 to 50% DP)				60	ns
$t_{UARTON2V7}$	Turn-on time for TXD line (2V7)	UART_2V7 = 1 measured from DIR assertion		2	2.5	ms
$t_{UARTOFF2V7}$	Turn-off time for TXD line (2V7)	UART_2V7 = 1 measured from STP assertion			1	µs
t_{UARTON}	Turn-on time for TXD line	UART_2V7 = 0 measured from DIR assertion			60	ns
$t_{UARTOFF}$	Turn-off time for TXD line	UART_2V7 = 0 measured from DIR de-assertion			60	ns
Low-speed driver						
t_{LR}	Data signal rise time	C_{LOAD} = 600 pF	75	100	300	ns
t_{LF}	Data signal fall time	C_{LOAD} = 600 pF	75	100	300	ns
RFM_{LS}	Rise and fall time matching		-20		20	%
DR_{LS}	Low-speed data rate		1.49925		1.50075	Mb/s
t_{DDJ1}	Data jitter to next transition	Includes freq. tolerances	-25		25	ns
t_{DDJ2}	Data jitter for paired transitions	Includes freq. tolerances	-14		14	ns
t_{LEOPT}	SE0 interval of EOP		1250		1500	ns
Full-speed driver						
t_{FR}	Data signal rise time	C_{LOAD} = 50 pF	4		20	ns
t_{FF}	Data signal fall time	C_{LOAD} = 50 pF	4		20	ns
RFM_{FS}	Rise and fall time matching		-10		+10	%
DR_{HS}	Full-speed data rate		11.994		12.006	Mb/s
t_{DJ1}	Data jitter to next transition	Includes freq. tolerances	-3.5		3.5	ns
t_{DJ2}	Data jitter for paired transitions	Includes freq. tolerances	-4		4	ns
t_{FEOPT}	SE0 interval of EOP		160		175	ns
Clock generation constants						
t_{PLL}	PLL lock time	(2)			200	µs
t_{DLL}	DLL lock time	(2)			280	µs

Table 7. Switching characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
High-speed driver						
t_{HSR}	Data rise time		500			ps
t_{HSF}	Data fall time		500			ps
	Waveform requirements including jitter		Specified by eye pattern (*Figure 3*)			
DR_{HS}	High-speed data rate		479.76		480.24	Mb/s
ULPI interface						
CLOCK (measured on CLK pin)						
f_{START_U}	Frequency (first transition)	(2)	54	60	66	MHz
f_{STEADY_U}	Frequency (steady-state)		59.97	60	60.03	MHz
D_{START_U}	Duty cycle (first transition)		40	50	60	%
D_{STEADY_U}	Duty cycle (steady-state)	(2)	45	50	55	%
T_{STEADY_U}	Time to reach steady-state frequency and duty cycle after first transition	(2)			1.4	ms
T_{JITTER_U}	Jitter			400		ps
$t_{SCLK60OUT}$	Clock startup time	Measured from assertion of STP during suspend, or after release of RESETn pin	250		900	µs
ULPI control signals (SDR mode)(2)						
T_{SC_U}	Control in setup time	C_{LOAD} = 15 pF V_{DVIO} = 1.65 - 3.6 V	6.0			ns
T_{HC_U}	Control in hold time		0.0			ns
T_{DC_U}	Control output delay				9.0	ns
ULPI data signals (SDR mode)(2)						
T_{SD_U}	Data in setup time	C_{LOAD} = 15 pF V_{DVIO} = 1.65 - 3.6 V	6.0			ns
T_{HD_U}	Data in hold time		3.0			ns
T_{DD_U}	Data output delay				9.0	ns

1. Over recommended operating conditions unless otherwise noted. All the typical values are referred to T_A = 25 °C, V_{DVIO} = 1.8 V, V_{BAT} = 3.6 V, C_T = 4.7 µF.
2. Guaranteed by design.

Figure 3. High-speed driver eye pattern

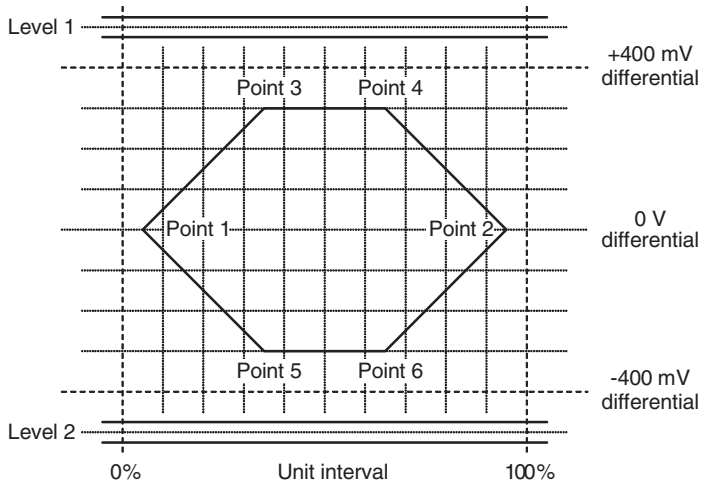


Table 8. High-speed driver eye pattern

Parameter	Level 1	Level 2	Point 1	Point 2	Point 3	Point 4	Point 5	Point 6
Voltage level (DP – DM)	525 mV(1) 475 mV	–525 mV(1) –475 mV	0 V	0 V	300 mV	300 mV	–300 mV	–300 mV
Time (% of unit interval)			5%	95%	35%	65%	35%	65%

1. This value is valid for unit intervals following a transition. For all other intervals the other value is valid.

5 Timing diagram

Figure 4. Rise and fall time

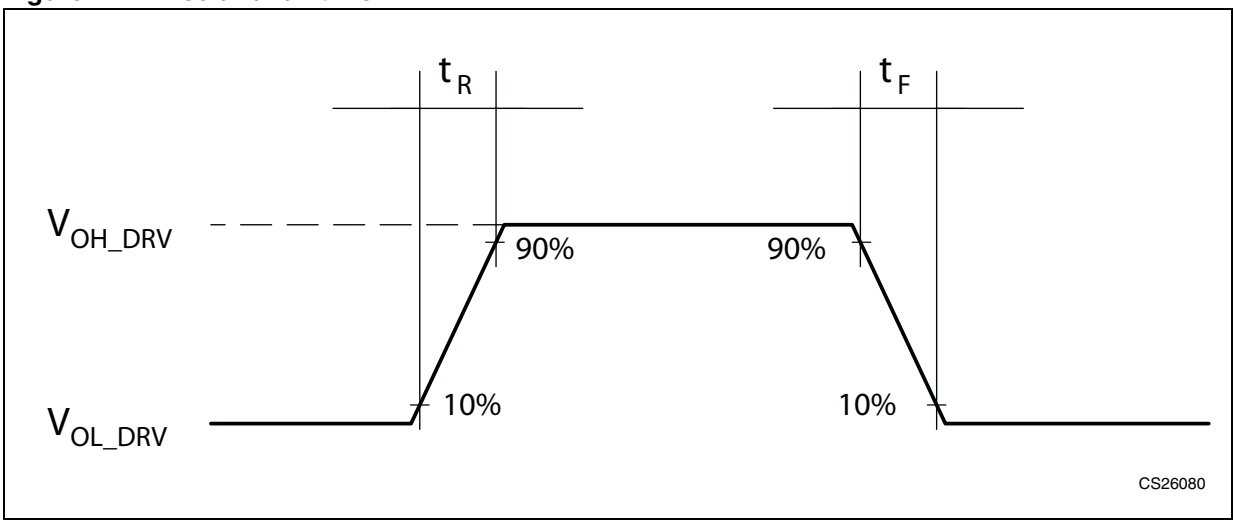
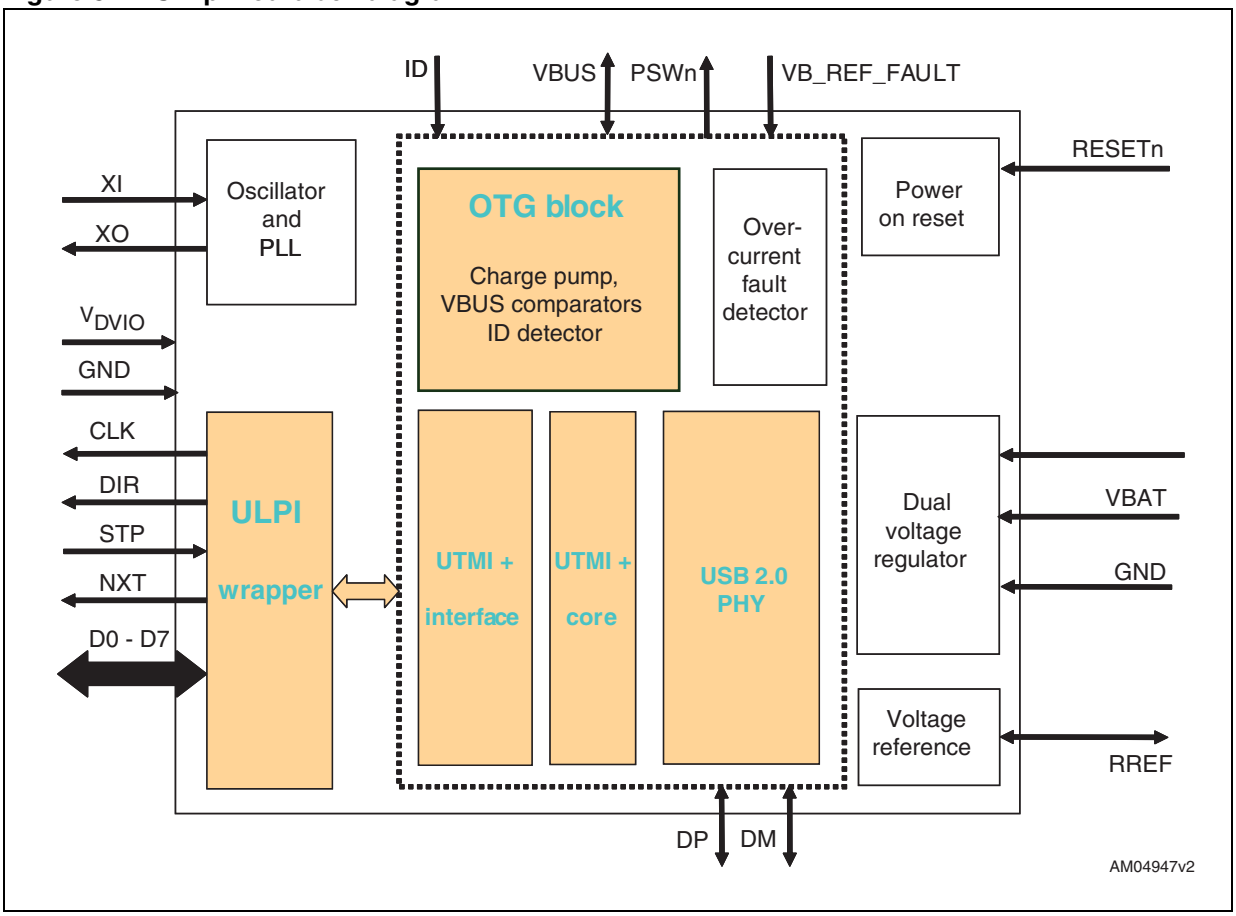


Figure 5. Simplified block diagram



6 Block description

The STULPI01 integrates a comparator for the VBUS, ID line detector, differential HS data driver, differential and single-ended receivers, low dropout voltage regulators, and control logic.

The STULPI01 provides a complete solution for the connection of a digital USB host/device/OTG controller to a USB bus.

6.1 Oscillator and PLL

An external clock (digital square wave V_{DVIO} referred) driven into XI must be used (version STULPI01A or STULPI01B).

The PLL internally produces all frequencies needed for operation:

- 60-MHz clock for the UTMI core and ULPI interface controller
- 1.5 MHz for low-speed USB data
- 12 MHz for full-speed USB data
- 480 MHz for high-speed USB data
- Other internal frequencies for data conversion and data recovery.

6.2 Voltage reference

This block provides the precise reference voltage needed by the internal circuit.
It requires a 12 kΩ +/- 1% resistor connected to the R_{REF} pin.

6.3 Power-on reset (POR)

The power-on reset circuit generates a reset pulse upon power-up which is used to initialize the entire digital logic. Power-on reset senses the V_{3V3V} and V_{1V2V} voltage.
During the power-on reset pulse, the ULPI pins are in a high impedance state with pull-down/pull-up resistors disabled.

6.4 UTMI + core

This is the digital heart of the chip and performs the bit-stuffing, NRZI decoding and serial to parallel conversion during receive and the reverse operation during transmit for HS and FS/LS.

6.5 ULPI wrapper

This implements the ULPI related protocol and conversion from UTMI+ to ULPI interface. This block also implements the interrupt logic and complete ULPI register set.

6.6 External charge pump

It is possible to use an external charge pump or power switch controlled by the PSWn pin (active low open drain). This functionality is controlled by DrvVbus and DrvVbusExternal ULPI OTG control register bits.

6.7 V_{BUS} comparators and V_{BUS} overcurrent (OC) detector

These comparators monitor the V_{BUS} voltage.

V_{BUS} valid status signals that the voltage is above the V_{BUS_VLD} level (4.4 V). Session valid status signals that the V_{BUS} voltage is above the V_{SESS_VLD} level (0.8 to 2.0 V). Session end detector signals that V_{BUS} voltage is below V_{SESS_END} level.

The STULPI01 also implements an embedded V_{BUS} overcurrent detector which compares V_{BUS} voltage to the external analog 5 V reference signal applied to the VB_REF_FAULT pin.

6.8 VB_REF_FAULT pin

V_{BUS} overcurrent conditions can be monitored by either an internal or external OC detector. The internal OC detector is enabled when the overcurrent_PD bit in the power control register (vendor-specific area) is set to 0b and Use External VBUS Indicator is set to 1b. In this mode, the VB_REF_FAULT pin functions as the input of the analog reference for internal overcurrent detector.

If the external charge pump is already equipped with an overcurrent detector, its output can be also monitored through the VB_REF_FAULT pin, but the overcurrent_PD bit must be set to 1b. In this mode, VB_REF_FAULT functions as the standard digital input pin with 5 V tolerance. Functionality of the VB_REF_FAULT pin can be seen in more detail in *Figure 6*.

Note: After reset, the overcurrent_PD bit is 1b, the internal overcurrent detector is disabled.

Figure 6. VB_REF_FAULT pin functionality

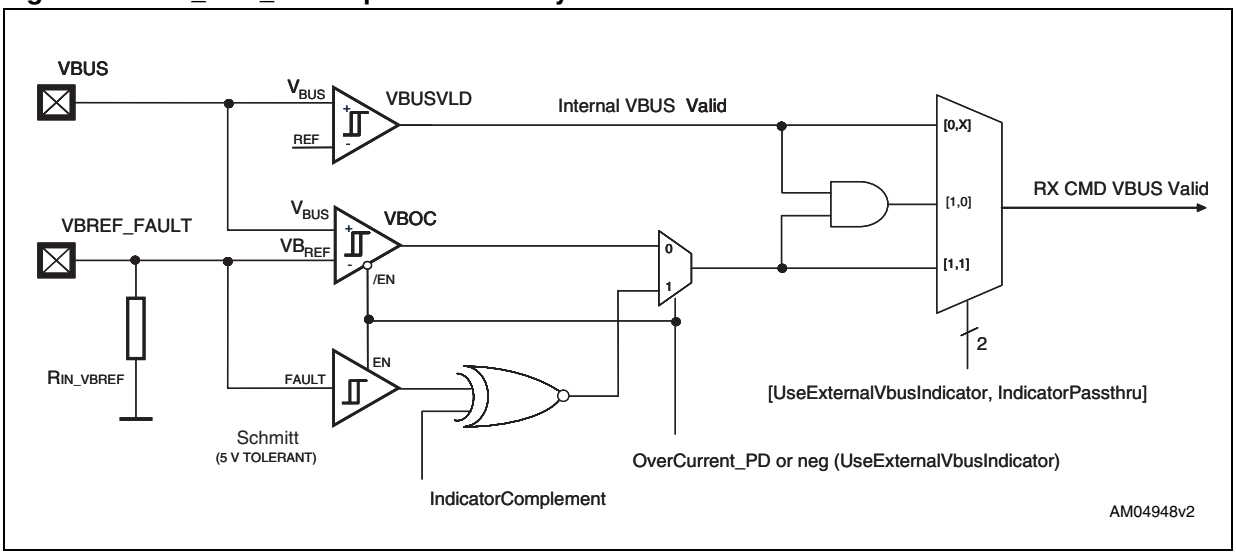


Table 9. VB_REF_FAULT configuration bit settings

RX CMD VBUS valid	Use External Vbus Indicator	Overcurrent_PD	Indicator Pass-Thru	Indicator complement
VBUSVLD	0	1	X	X
VBOC	1	0	1	X
VBOC and VBUSVLD	1	0	0	X
neg (FAULT)	1	1	1	0
FAULT	1	1	1	1
VBUSVLD and FAULT	1	1	0	1
VBUS_VLD and neg (FAULT)	1	1	0	0

6.9 Voltage regulator

The dual output ultra low dropout voltage regulator provides the power supply for analog and digital internal circuits. An external capacitor on both the 3V3V and 1V2V pins is needed for proper operation.

6.10 ID detector

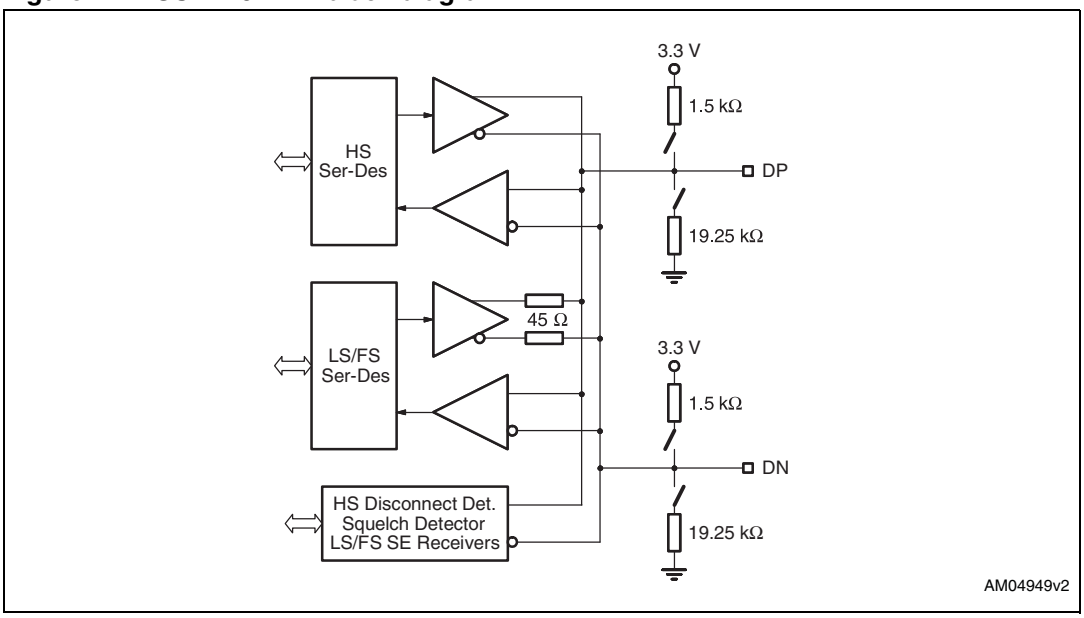
This block provides the sensing of the status of the ID line. It is capable of detecting whether the pin is floating or tied to the ground.

6.11 USB 2.0 PHY

The USB 2.0 PHY block provides a complete physical layer transceiver for low-speed, full-speed, and high-speed USB operating modes. The analog part of this block deals with impedance adaptation, controlled voltage swing, and Common mode voltage generation

and sensing. The digital part consists of a serializer and deserializer, transforming serial bit stream to 8-bit parallel port, and finite state machine implementing the PHY protocol layer, bit stuffing, unstuffing, etc.

Figure 7. USB 2.0 PHY block diagram



6.12 Power saving features

To reduce power consumption, the STULPI01 implements 2 Low-power modes of operation.

1. Low-power mode, which is defined in the ULPI specification.
2. Power-down mode to save more power in case USB function is not needed.

More information on these modes can be found in the following paragraphs.

6.13 Modes of operation

6.13.1 ULPI synchronous mode

The STULPI01 transceiver supports SDR mode operation (12-pin interface). The selection of SDR mode is performed during the startup reset procedure.

6.13.2 6-pin FS/LS serial mode

This mode is entered by writing to the corresponding bit in the Interface Control register.

6.13.3 3-pin FS/LS serial mode

This mode is entered by writing to the corresponding bit in the Interface Control register.

6.14 Car Kit (UART) mode

This mode is entered by writing to the Car Kit mode bit in the interface control register. The STULPI01 does not implement all features of Car Kit mode, only the UART functionality is preserved.

Table 10. Car kit signals mapping

Default car kit signals mapping (UART_DIR = 0)		
Signal	ULPI lines	USB lines
TXD	DATA[0] (input) ->	DM (output)
RXD	DATA[1] (output) <-	DP (input)
Reserved	DATA[2] (input)	
INT	DATA[3] (output)	
Car kit signals mapping (UART_DIR = 1)		
Signal	ULPI lines	USB lines
TXD	DATA[0] (input) ->	DP (output)
RXD	DATA[1] (output) <-	DM (input)
Reserved	DATA[2] (input)	
INT	DATA[3] (output)	

TXD or RXD paths are activated only when the corresponding bits TXD_EN/RXD_EN in car kit control register bits (*Table 23*) are set.

The UART_2V7 bit controls the voltage level of UART signaling. If 2V7 volt signaling is used, after the UART mode is entered, PLL is disabled and the voltage on the regulator output starts to decrease to 2.7 V. After a time marked as $t_{UARTON2V7}$, the TXD output on the USB bus is enabled.

When leaving Car Kit mode, TXD is disabled immediately when the STP pin is asserted. The time required to exit Car Kit mode is equivalent to the time needed for PLL startup.

When 3.3 volt UART signaling is selected, the TXD line is enabled immediately after entering Car Kit mode, and disabled after exiting this mode.

Note: When Car Kit mode is used with 2V7 signaling, the PLL and output clock are always stopped regardless of the setting of the ClockSuspendM bit.

6.15 Low-power mode

The STULPI01 enters Low-power mode when the SuspendM bit in the interface control register is set to 0b. Most of the references are turned off, PLL and clock are turned off, but the full wake-up capability as defined in the ULPI specification is still maintained.

When in Low-power mode, the PHY drives D3-D0 with the signals listed in *Table 11*. Line state is driven combinatorially from the SE receivers. The INT signal is asserted whenever any unmasked interrupt occurs. The PHY latches interrupt events directly from analog circuitry because the clock is powered down.

Table 11. Low-power mode

Signal	Map to	Dir	Description
Linestate (0)	D0	out	Driven combinatorially from SE receivers
Linestate (1)	D1	out	Driven combinatorially from SE receivers
Reserved	D2	out	Reserved
INT	D3	out	Active high interrupt indication. Asserted whenever any unmasked interrupt occurs.

Low-power mode is exited by asserting the STP pin high. PLL is started immediately, and when the clock becomes stable, it is passed on the output of the CLK pin. Then, after a minimum of 5 clock cycles, DIR is deasserted and Low-power mode is exited. The SuspendM bit is reset to 1b.

Note: The STP signal must be kept high until the DIR is deasserted, otherwise Low-power mode is not exited.

6.16 Power-down mode

Power-down mode is entered by asserting the CSn/PWRDN pin high. Internal voltage regulators are disabled, and the device has minimum possible power consumption. The STULPI01 has no wake-up capability or USB functionality during Power-down mode. This mode can be exited by deasserting the CSn/PWRDN pin. Voltage regulators are turned on and the internal power-on reset circuit resets the chip to initial state. ULPI interface pins are in high impedance state during Power-down mode.

6.17 VIO OFF mode

If V_{DVIO} is below the minimum value, VIO OFF mode is entered. The behavior of the device in VIO OFF mode is the same as in Power-down mode.

6.18 Startup procedure

6.18.1 ULPI device detection

The link detects ULPI device presence by sampling the DIR signal at the reset time (*Figure 8*). The NXT signal is '0' after reset to signal an 8-bit device to the link controller. CLK is '1' to signal a DDR capable device.

6.18.2 SDR mode selection

The STULPI01 samples the D0 line on the first rising edge of the output clock on the CLK pin. When the sampled value is '0', the STULPI01 remains in SDR mode.

SDR mode can be selected again only after hardware reset. During software reset mode, selection is not performed.

Note: IMPORTANT: The controller must not drive the DATA lines to a value other than 0x00 or 0x01 during the first rising edge of ULPI CLK, otherwise the behavior of the device may be undefined.

6.18.3 External clock detection

The square wave clock can be applied to the oscillator input. The input square wave clock amplitude is referenced to V_{DVIO}.

The XO pin can be left floating or grounded.

6.18.4 Reset behavior

A typical startup sequence is shown in *Figure 12*.

The STULPI01 contains an internal power-on reset generator which senses the V3V3V and V1V2V voltage. Assertion of RESETn is not necessary for proper initialization. However, if required, this pin can be also used. The internal reset signal is the combination of the signal from the RESETn pin and the signal from the internal power-on reset circuit.

When RESETn is asserted, all internal registers are reset to their default values, the output DIR signal is driven to '1', and data lines are pulled low by weak pull-downs.

During reset, the STP pin can be driven low, high, or can be left floating. It is pulled up by internal pull-up and the ULPI interface enters a holding state.

During the reset state, the NXT signal is driven low and the CLK is driven high.

When the PLL is stabilized, the clock on the CLK pin is enabled, and DIR is deasserted.

Note: The minimum duration of the external reset signal is TRESETEXT. (See Table 7).

When internal POR reset is asserted, the reset procedure is equivalent to the RESETn signal, with the only exception being that the ULPI lines are in high impedance state. All pull-downs and pull-ups on the ULPI signals are also disabled.

6.18.5 Interface protection

The STULPI01 activates weak pull-downs on data lines and pull-up on the STP during reset and holding state. These are to provide interface protection during startup and anytime the link is not able to drive the ULPI lines properly.

The holding state is entered when the controller drives the STP for more than 1 clock cycle. Any command on the ULPI bus is ignored in this state. For more information see ULPI specification 1.1, section 3.12 (Safeguarding PHY input signals).

Interface protection can be switched off at any time after startup in order to save power, by writing the Interface Protect Disable bit in the Interface Control register to 1b.

6.18.6 Software reset

The STULPI01 supports software reset by writing the RESET bit in the function control register to 1b.

During software reset, DIR is asserted and the pull-down resistors on data lines are enabled, but the ULPI registers remain unaffected. Software reset initializes UTMI core logic only. Also, during software reset, external clock detection, SDR mode selection is not performed, and the clock is not turned off (PLL is not restarted).

Note: Software reset is not required in the startup procedure for the STULPI. The chip is ready for operation after the hardware reset procedure.

6.18.7 High-speed mode entry

In High-speed mode, the internal 480-MHz clock is generated by the DLL, which must be calibrated any time the device enters High-speed mode by writing '00' to the XcvrSel field in the Function Control register. During the DLL calibration, it is not possible to accept any commands, therefore, to avoid any communication problems with the controller, the clock on the ULPI interface is stopped. See *Figure 10* for more information.

Figure 8. Startup sequence