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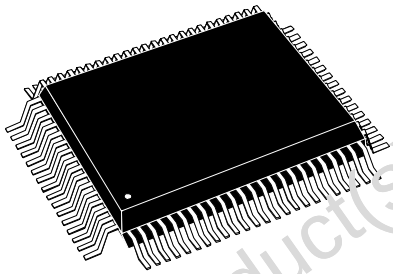
STV2050A

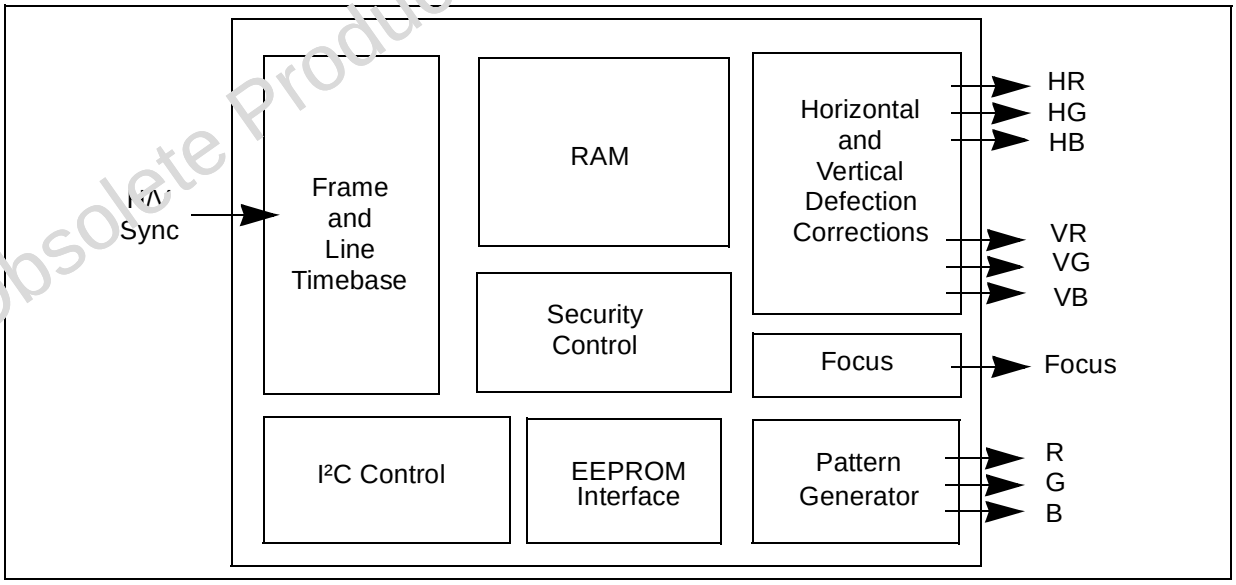
AUTOMATIC MULTISCAN DIGITAL CONVERGENCE PROCESSOR

- Multiscan 1H, 2H, HDTV and SVGA applications
- 6 Convergence channels
- 14-bit embedded DACs
- 1 Focus channel
- Second order interpolation in vertical direction
- Digital filtering in horizontal direction
- On-chip PLL
- On-chip video pattern generator
- Automatic compensation of temperature drift and aging of external components
- Pattern and synchronisation signals for optional optical sensor support
- Adjustable horizontal and vertical size
- Up to 7 different data sets
- Self-controlled power-on sequence



Package: PQFP80
Power Supply: 3.3 V
Tape and Reel: STV2050ATR

Figure 1. Functional Block Diagram



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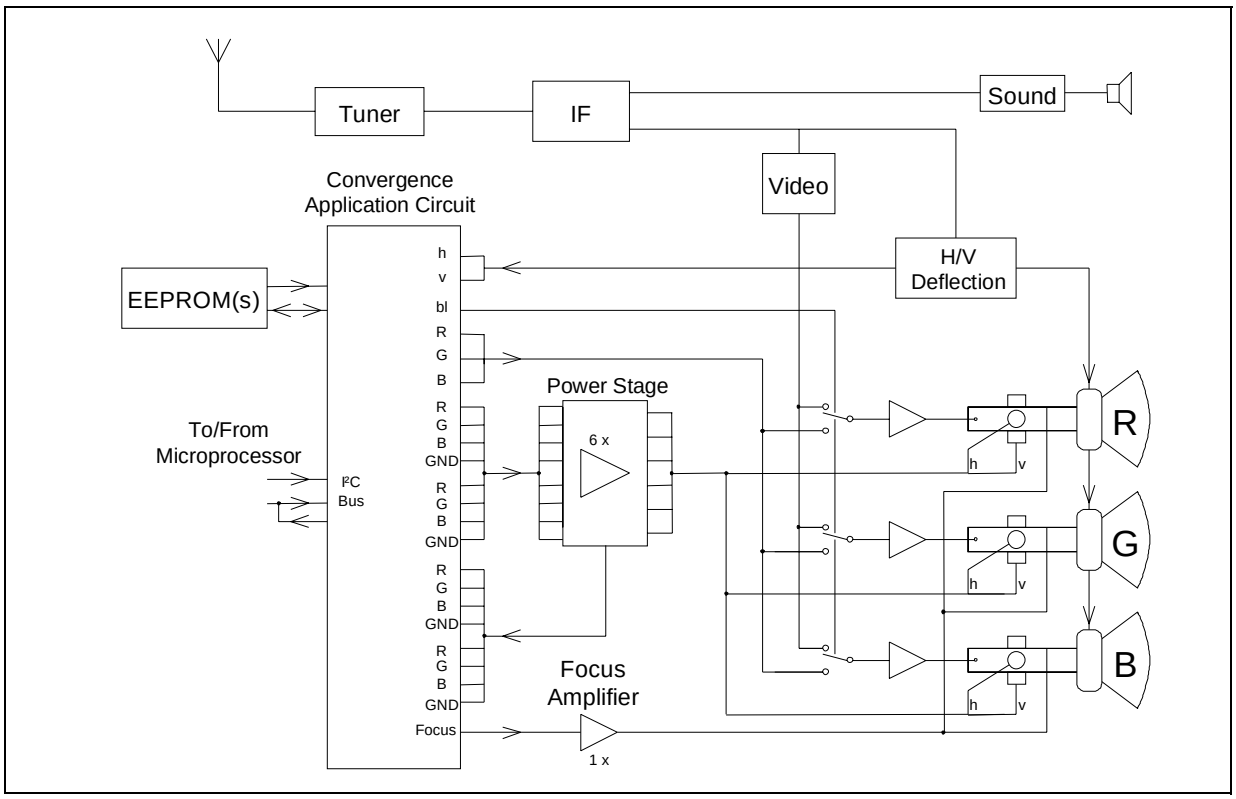
1 GENERAL OVERVIEW

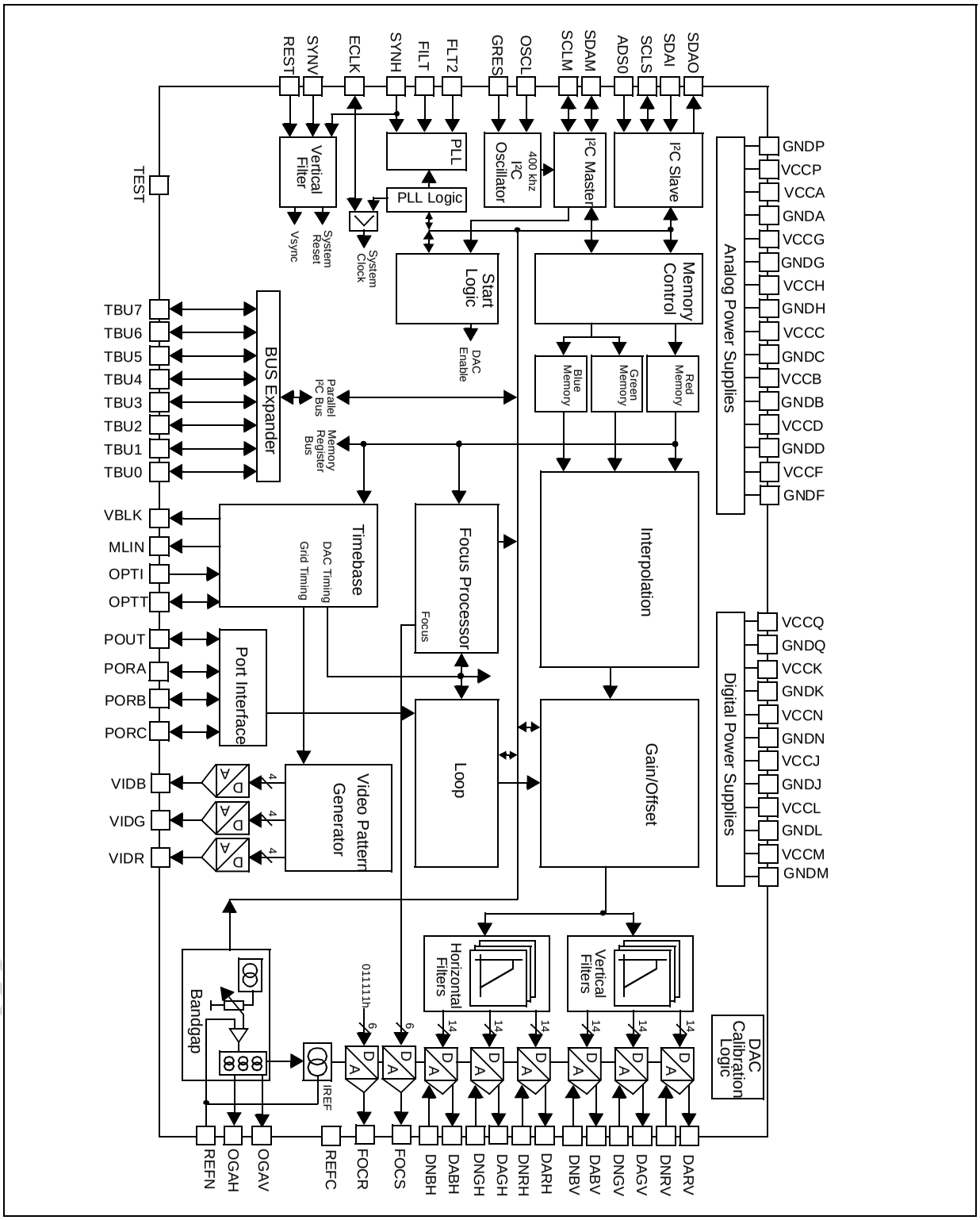
1.1 SYSTEM BLOCK DIAGRAM

Figure 2. TV Set Convergence System Diagram



1.2 DEVICE BLOCK DIAGRAM

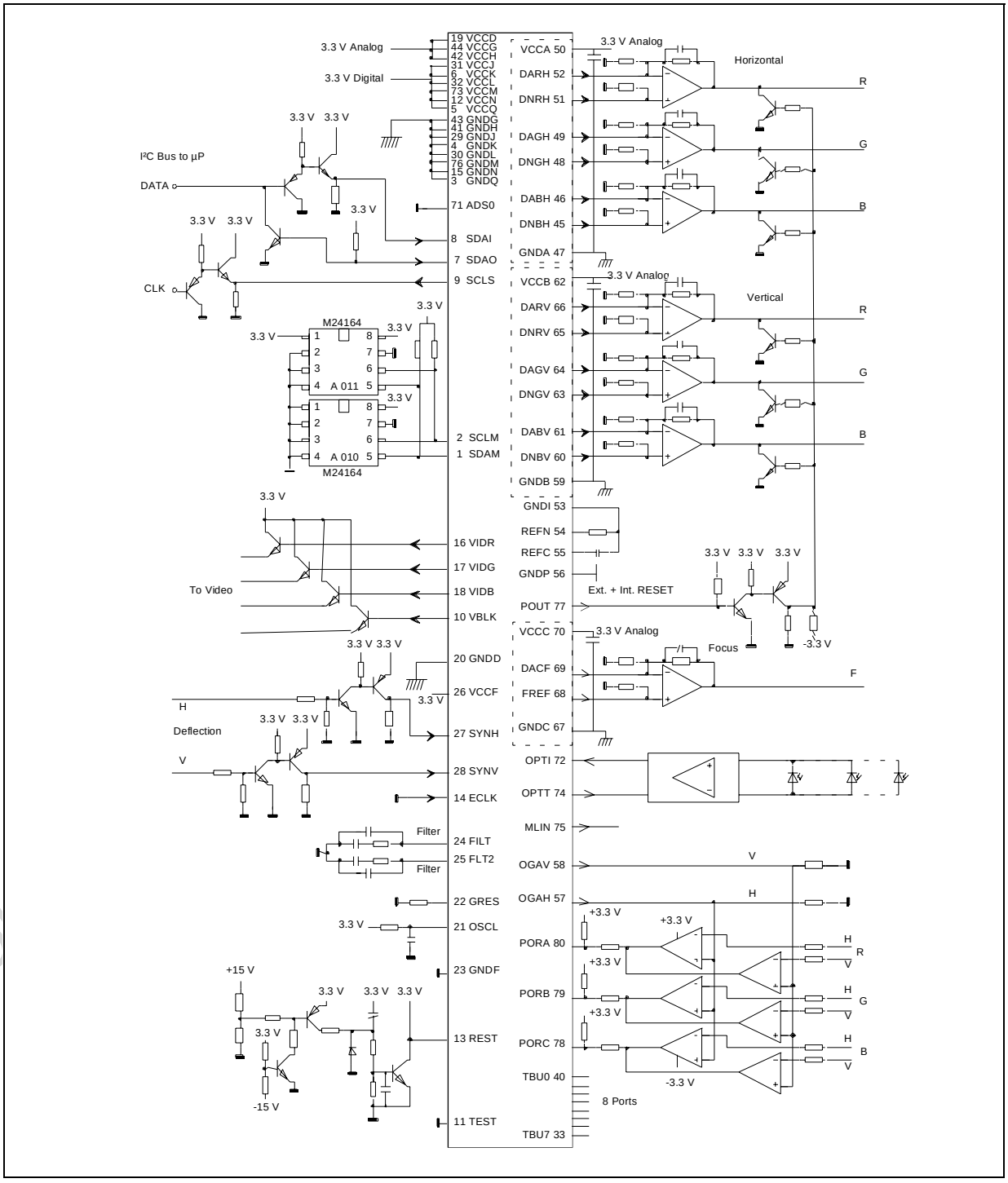
Figure 3. STV2050A Block Diagram



1.3 APPLICATION CIRCUIT

An application circuit with 2nd EEPROM, Electrical Offset and Gain Adjustment Loop and Optical Sensors is shown in the following figure.

Figure 4. Application Circuit



1.4 PIN DESCRIPTION AND PINOUT DIAGRAM

The following legend applies to the Pin Description Table below:

X = Undefined HZ = High Impedance

"0" = Low Level Output "1" = High Level Output

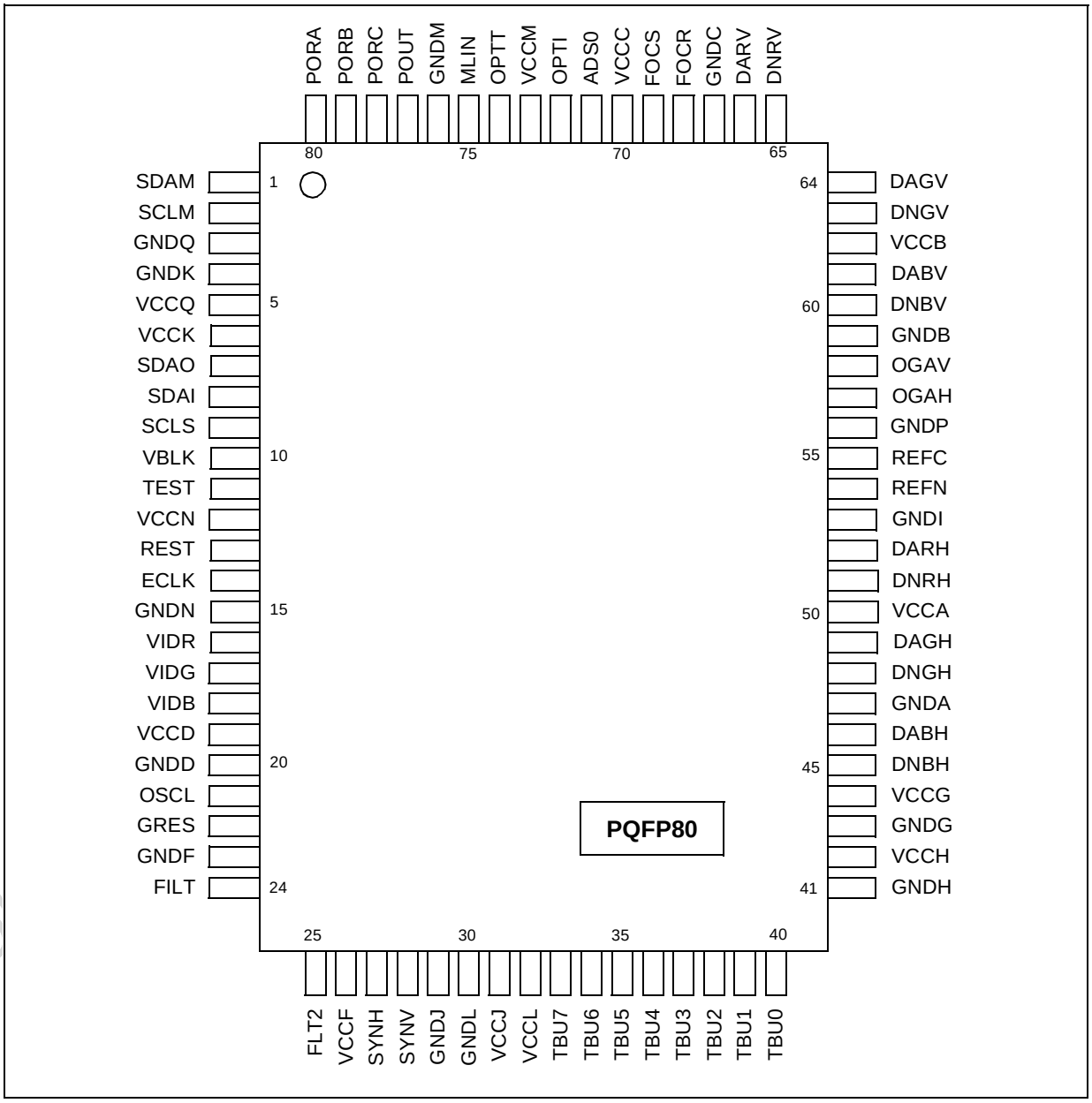
Table 1. Pin Description

Pin No.	Pin Name	Reset Status and Remarks	Description
1	SDAM	HZ	Master Bus: "Data"
2	SCLM		Master Bus: "Clock"
3	GNDQ		Digital Supply: Ground
4	GNDK		Digital Supply: Ground
5	VCCQ		Core / RAM Digital Supply: 3.3 V
6	VCCK		Core / Digital Supply: 3.3 V
7	SDAO	"0"	Slave Bus: "Data" output
8	SDAI		Slave Bus: "Data" input
9	SCLS		Slave Bus: "Clock"
10	VBLK		Video Pattern Blanking
11	TEST	Must be grounded	Reserved
12	VCCN		Shield Supply Digital Supply: 3.3 V
13	REST	"0"	Reset
14	ECLK	Must be grounded	Reserved
15	GNDN		Digital Supply: "Ground"
16	VIDR	0 Volts	Video Pattern Output: "Red"
17	VIDG	0 Volts	Video Pattern Output: "Green"
18	VIDB	0 Volts	Video Pattern Output: "Blue"
19	VCCD		Video Generator Supply: 3.3 V
20	GNDD		Video Generator Supply: Ground
21	OSCL	HZ	RC for internal oscillator
22	GRES	HZ	R for internal oscillator
23	GNDF		PLL Supply: Ground
24	FILT	HZ	Filter for PLL
25	FLT2	HZ	Filter for PLL
26	VCCF		Supply PLL: 3.3 V
27	SYNH		Horizontal Synchronization input
28	SYNV		Vertical Synchronization input
29	GNDJ		Digital Supply: Ground
30	GNDL		Digital Supply: Ground
31	VCCJ		Core Digital Supply: 3.3 V
32	VCCL		Ring / Buffer Digital Supply: 3.3 V
33	TBU7	X	I²C BUS Expander
34	TBU6	X	I²C BUS Expander
35	TBU5	X	I²C BUS Expander
36	TBU4	X	I²C BUS Expander

Pin No.	Pin Name	Reset Status and Remarks	Description
37	TBU3	X	I²C BUS Expander
38	TBU2	X	I²C BUS Expander
39	TBU1	X	I²C BUS Expander
40	TBU0	X	I²C BUS Expander
41	GNDH		Analog Supply: Ground
42	VCCH		D/A Interface Analog Supply: 3.3 V
43	GNDG		Analog Supply: Ground
44	VCCG		Analog Supply: 3.3 V
45	DNBH	HZ	Horiz. Convergence Output: Blue, negative
46	DABH	HZ	Horiz. Convergence Output: Blue, positive
47	GNDA		Horiz. Convergence Output Supply: Ground
48	DNGH	HZ	Horiz. Convergence Output: Green, negative
49	DAGH	HZ	Horiz. Convergence Output: Green, positive
50	VCCA	HZ	Horiz. Convergence Output Supply: 3.3 V
51	DNRH	HZ	Horiz. Convergence Output: Red, negative
52	DARH	HZ	Horiz. Convergence Output: Red, positive
53	GNDI		Floating GND for bandgap filter
54	REFN	Reference Current Code 0(hex)	I_{REF} Loop for H&V Convergence & Focus
55	REFC	X	Filter pin for I_{REF} current
56	GNDP		I_{REF} GND for Bandgap
57	OGAH	HZ	Horiz. Reference output for electrical loop
58	OGAV	HZ	Vert. Reference output for electrical loop
59	GNDB	HZ	Vert. Convergence Output Supply: Ground
60	DNBV	HZ	Vert. Convergence Output: Blue, negative
61	DABV	HZ	Vert. Convergence Output: Blue, positive
62	VCCB		Vert. Convergence Output Supply: 3.3 V
63	DNGV	HZ	Vert. Convergence Output: Green, negative
64	DAGV	HZ	Vert. Convergence Output: Green, positive
65	DNRV	HZ	Vert. Convergence Output: Red, negative
66	DARV	HZ	Vert. Convergence Output: Red, positive
67	GNDC		Focus Supply: Ground
68	FOCR		Focus Reference Output
69	FOCS		Focus Signal Output
70	VCCC		Focus Supply
71	ADS0		I²C Slave Bus Address Selection
72	OPTI		Input for optical sensor support
73	VCCM		Ring / Inputs Digital Supply: 3.3 V
74	OPTT	Input	I pin: Latched at measuring line or with sys. clock; O pin: Push/pull, output can be switched to high impedance
75	MLIN	"0"	Measuring Line Signal Output
76	GNDM		Digital Supply: Ground

Pin No.	Pin Name	Reset Status and Remarks	Description
77	POUT	HZ	Protection Pin Control
78	PORC	Input	Normally used for electrical loop feedback detection. Can also be set as an inpout or an output.
79	PORB		
80	PORA		

Figure 5. Pinout Diagram



2 STRUCTURE OF THE PROGRAMMING SYSTEM

2.1 DATA STORAGE

The STV2050A is a programmable device. Some of the data, mainly the convergence parameters, must be able to be easily changed during TV set alignment or by the user, and must be memorized when the TV set is switched off in order to be recovered when switched back on. This data must therefore be stored in EEPROM.

The STV2050A has an **embedded RAM** for storing data used “in real time” at a high speed.

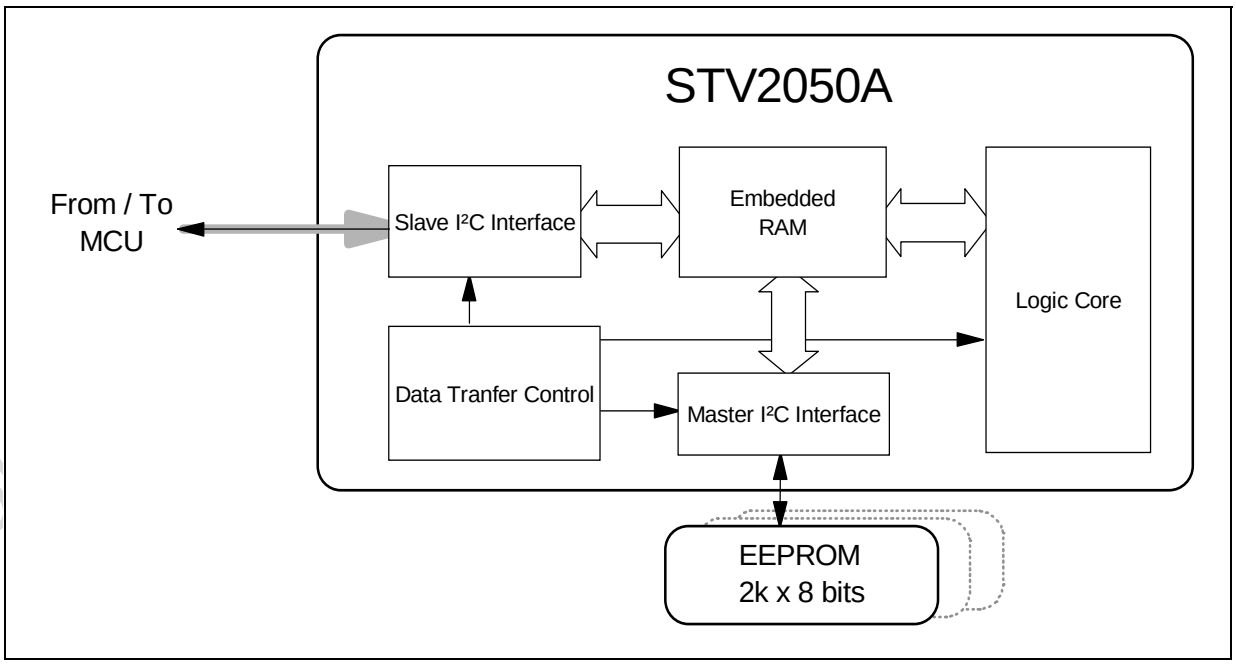
In order to simplify the microcontroller software, and to ensure a quick startup, the STV2050A directly controls one or more (or up to seven) EEPROMs.

The STV2050A has 2 ports for I²C connections:

– The first one is used only for “**SLAVE**” connections: it is used to interface with a microcontroller in order to control the IC (customer adjustments,...). The microcontroller can write and read the embedded RAM via this slave port.

– The second one is used only for “**MASTER**” connections: it is used to interface the STV2050A with the EEPROM that stores the convergence data and some user adjustments. The transfer of data between the EEPROM and the embedded RAM is fully managed by the STV2050A.

Figure 6. I²C BUS Data Transfer



2.2 OVERVIEW OF EMBEDDED RAM ORGANIZATION

The RAM consists of 3 banks:

The first one, the “Red and I²C Bank”, uses 24-bit words. The two other banks, the “Green Bank” and “Blue Bank”, both use 22-bit words. Each bank has 208 words with addresses from 00(hex) to CF(hex).

These 3 x 208 words are allocated to the “dynamic” convergence parameters. (Refer to Section 4.1 "CONVERGENCE CORRECTION VALUES" on page 18.)

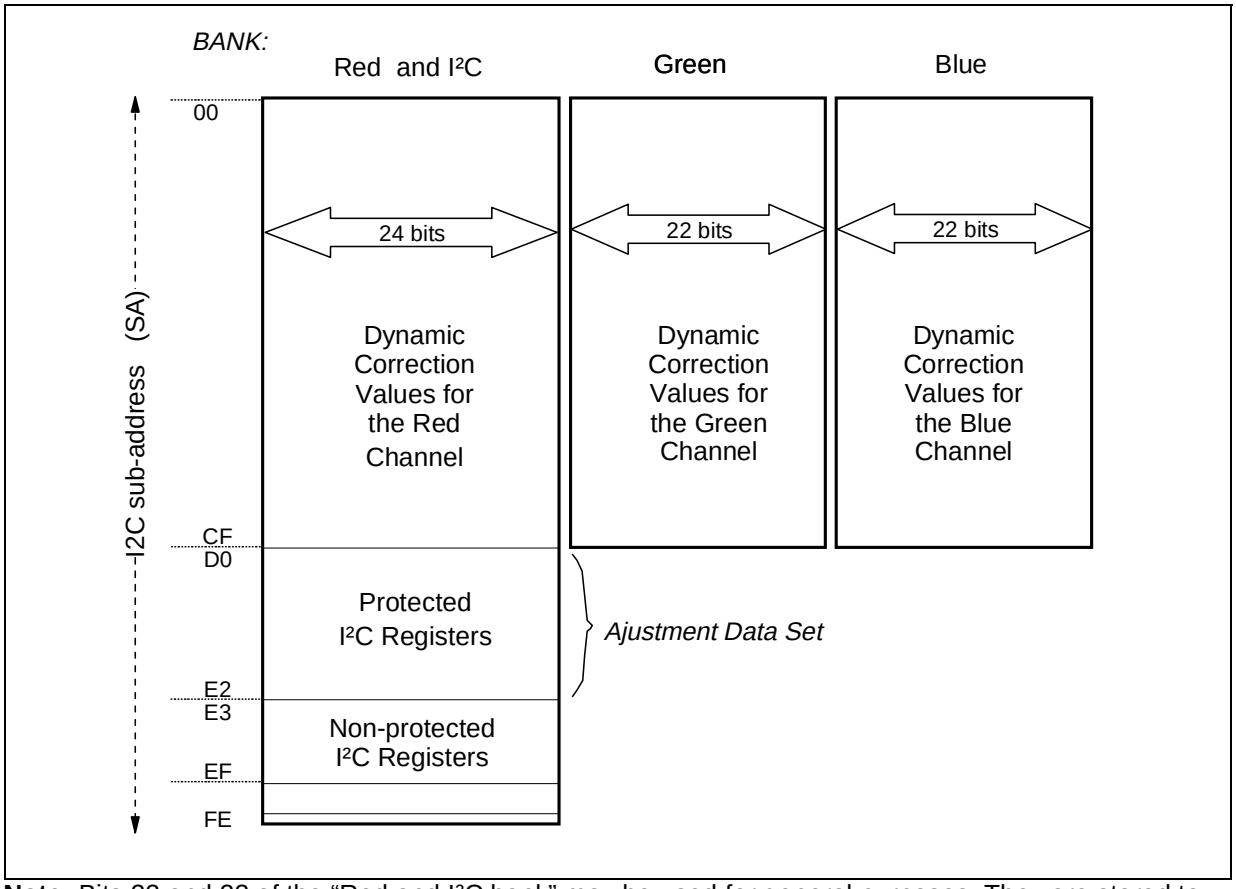
The “Red and I²C Bank” has 33 additional words: addresses from D0(hex) to EF(hex) and FE(hex). These words are used to buffer the I²C Bus registers.

As shown in this figure, each word can be pointed to by a sub-address (SA). Thus, each sub-address points to 24- (or 22-, depending on the bank) bit wide words. A word virtually consists of three bytes (24-bits) named D0, D1 and D2 as shown in the following figure. The bit order is named as follows: D0[7] is the MSB and D2[0] is the LSB

	MSB															LSB								
	D0 Byte								D1 Byte								D2 Byte							
Bit	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0

Note: Bit D0[7:6] is not physically implemented in the “Green” and “Blue” banks.

Figure 7. Color Banks



Note: Bits 22 and 23 of the “Red and I²C bank” may be used for general purposes. They are stored together with the convergence data in the external EEPROM.

2.3 ADJUSTMENT DATA SETS

The set of data stored at addresses D0 to E2 is called an ADS (Adjustment Data Set).

The STV2050A can store up to three ADSs in one standard EEPROM. Refer to Section 6 "MASTER I²C BUS INTERFACE" on page 28.

3 SLAVE I²C BUS INTERFACE

3.1 FEATURES

The I²C interface is controlled by 4 pins:

3.1.1 ADS0: IC Address and PLL Mode

The level at this pin corresponds to bit 1 in the first byte in bus transmissions.

– If ADS0 is connected to GND, the analog outputs will be automatically switched on after the reset sequence, and once the internal PLL is activated.

– If the pin is connected to VCC, the DACs will remain in high impedance. The internal PLL is inhibited, and the IC must use an external PLL.

3.1.2 SCLS Bus Clock

The polarity and timing for this pin comply with I²C Bus specifications.

3.1.3 SDAI Bus Data Input

The polarity and timing for this pin comply with I²C Bus specifications.

3.1.4 SDAO Bus Data Output

The polarity reversal and timing for this pin comply with I²C Bus specifications.

Abbreviations used:

S	=	Start condition
P	=	Stop condition
DA	=	Device address
DR	=	Device address for read
DW	=	Device address for write
SA	=	Sub-address
D0, D1,... Dn	=	Data bytes

The slave accepts the following DA subaddresses depending on the hardware configuration defined on pin ADS0.

ADS0	0 (grounded, internal PLL only) DR = 39, DW = 38 1 (3.3 Volt, external PLL only) DR = 3B, DW = 3A

For the 00 to CF address range (RAM), an autoincrement function can be enabled using the AIE (Auto Increment Enable) bit in the E7 register.

AIE	0 = Autoincrement disabled 1 = Autoincrement enabled

If the autoincrement function is enabled, the internal address is automatically incremented after 3 bytes are either written or read. When the autoincrement counter reaches the CF address, the counter stops counting and any additional data will be written to or read from the CF address.

3.2 COLOR BANK SELECTION

As previously mentioned, the embedded RAM is mapped in 3 banks called the “Red and I²C Bank”, “Green Bank” and the “Blue Bank”. A bank is selected using the CBS[1:0] (Color Bank Selection) bits located in the E7 register address.

CBS[1:0]	00 = Red and I²C bank selected 01 = Green bank selected 10 = Blue bank selected 11 = Red and I²C bank selected

However, sub-addresses D0 to EF and FE (physically mapped in the “Red and I²C Bank”) are independent of the actual bank selection.

3.3 WRITE COMMANDS

Three formats of write commands are supported:

– **5-byte write commands to any valid sub-address**

S DW SA D0 D1 D2 P

If the auto-increment function is enabled, the internal address is at SA+1 after the command, otherwise it is still at SA.

– **2-byte write commands for defining a sub-address cursor position or for changing the current sub-address without transmitting data.**

S DW SA P

The sub-address is at SA after the command.

– **Auto-increment write commands for sub-address range 00 to CF**

If the auto-increment function is enabled, the internal address counter is incremented each time 3 bytes are written:

S DW SA_i D_i0 D_i1 D_i2 $D_{i+1}0$ $D_{i+1}1$ $D_{i+1}2$... Dn P

otherwise every group of 3 bytes is written to SA and the sub-address does not change.

S DW SA_i D_i0 D_i1 D_i2 D_i0 D_i1 D_i2... ... Dn P

When a group of three data bytes within the 00 to E2 address range has been received, the slave will store them in the appropriate embedded RAM location. Only complete groups of three data bytes are stored. I²C registers start to be updated when the first data byte is received. Only complete bytes are written.

All write commands which do not comply with the formats described above are rejected.

3.4 READ COMMANDS

Read commands may access the IC internal RAM as well as all I²C registers. Read commands in the 00 to CF range read from the RAM bank that is defined by the two CBS bits that have been previously transmitted to the E7 register by a write command.

Addresses in the D0 to E2 range are mapped to the corresponding section of the red color RAM if the RRP bit in the EF register is '0'. Otherwise the corresponding internal register values are transmitted.

If the SA is in the 00 to CF address range, the position of the cursor is implicitly defined by the SA. An access to any other SAs will switch off the cursor. It will be switched on again if an address in the 00 to CF range is selected.

Three formats of read commands are supported:

– **Random read commands from any valid IC internal address**

S DW SA S DR SA D0 D1 D2 P

If the auto-increment function is enabled, the internal address is at the SA+1 after the command, otherwise it is still at the SA.

– **Read commands from the actual internal address**

S DR SA D0 D1 D2 P

If the auto-increment function is enabled, the internal address is at the SA+1 after the command, otherwise it is still at the SA.

– **Auto-increment read commands from addresses within the 00 to CF address range with random start address.**

S DW SA S DR SA D0 D1 D2..... Dn P

If the auto-increment function is enabled, the internal address counter is incremented after 3 bytes are read, otherwise the SA is always read and the internal address does not change.

When the last byte of the CF address has been transmitted, the IC internal auto-increment address counter stops counting and the CF value will be read out again.

3.5 I²C I/O LINES

Digital filters suppress pulses that are less than 1 or 2 clock pulses at the SDAI and SCLS inputs.

4 RAM ALLOCATION

4.1 CONVERGENCE CORRECTION VALUES

The convergence correction values are either dedicated to each correction point of each red/blue/green channel, or common for all points of each channel. (Refer to Section 9 "CONVERGENCE" on page 45.)

The values are grouped into 2 families:

– Dynamic correction values

– Common correction values

4.1.1 Dynamic Correction Values

The dynamic values are stored as described in Section 2.2 "Overview OF EMBEDDED RAM ORGANIZATION" on page 13.

For each Red, Green and Blue channel, the following can be stored in the embedded RAM:

– 13 horizontal "dynamic" correction values on 10 bits, plus 1 parity bit

– Up to 16 vertical "dynamic" correction values on 10 bits, plus 1 parity bit

For each correction point there is one corresponding word in the 00(hex) to CF(hex) sub-address range. Bits are stored in the corresponding “Red Bank”, “Green Bank” and “Blue Bank” as follows:

	MSB																								LSB
	BYTE D0								**BYTE D1**								**BYTE D2**							
Bit	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
			Horizontal Correction[9:0]												Vertical Correction[9:0]									

– Bit D1[3] is the horizontal correction parity bit

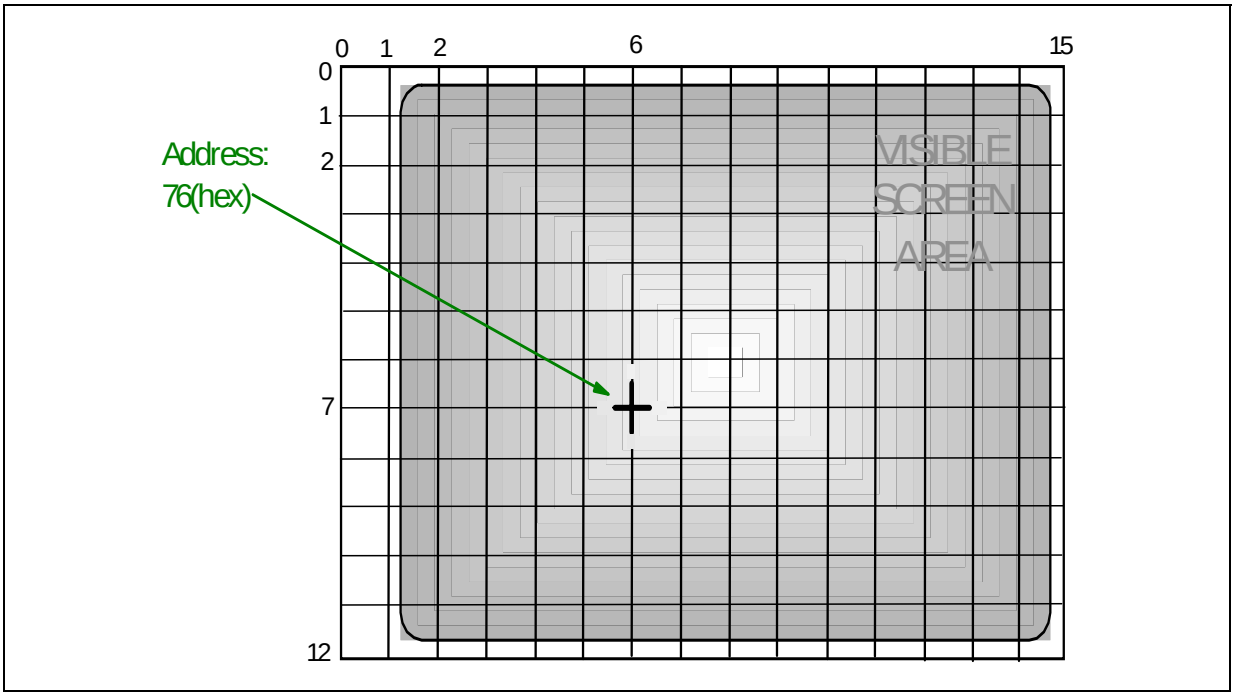
– Bit D1[2] is the vertical correction parity bit

– Bits D1[3:2] are generated by the STV2050A. Their value can be read out only.

Note: The STV2050A automatically checks the parity bits of each convergence value before applying them to the DACs. Refer to Section 14 "SECURITIES" on page 62.

The sub-address corresponds to the coordinates of the point on the screen where the vertical and horizontal lines meet, as shown in the following figure:

Figure 8. Addressing a Correction Point



4.1.2 Common Correction Values

The common correction values are stored in the “adjustment data sets” of the Red and I²C channel. See Figure 7 "Color Banks" on page 14 and Section 9.1 "GLOBAL ADJUSTMENTS - COMMON PARAMETERS" on page 45.

4.2 I²C REGISTERS

All I²C registers are implemented in the “Red and I²C Bank” of the embedded RAM. As it can be useful to store some of the I²C register content in the EEPROM, the embedded RAM allocation is divided into two parts:

– From sub-address D0 to E2 (included), contents can be stored in the EEPROM, and can then be restored,

– From sub-addresses E3 to EF and FE, contents are lost when the STV2050A is switched off.

4.2.1 Registers Storable in the EEPROM

	MSB							LSB																
	BYTE D0								BYTE D1								BYTE D2							
SA	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
D0	RFH[7:0]								GFH[7:0]								BFH[7:0]							
D1	RFV[7:0]								GFV[7:0]								BFV[7:0]							
D2	ORH[7:0]								OGH[7:0]								OBH[7:0]							
D3	ORV[7:0]								OGV[7:0]								OBV[7:0]							
D4	x	PDC	PDB	PDA	x	POC	POB	POA	X	PLT	GOS	HVM	GAV[1:0]		GAH[1:0]		X	X	X	X	X	X	X	X
D5	PRS	0	AMS[0		BGA[4:0]				PMH	PMV	X	X	X	X	MLE		MLN[8:0]							
D6	PBH[3:0]				PBV[3:0]				HBE	HAE	HVB[5:0]						VBE	VAE	VVB[5:0]					
D7	x	HGP[6:0]							TVH	TVV	BPH[5:0]						FAS	STA	BPV[5:0]					
D8	ACW	x	HGD[5:0]						ACL[1:0]		HRD[5:0]						AFS[1:0]		ASP[2:0]			FSO	HIF[1:0]	
D9	VGP[7:0]								VGP	VFP	VGD[5:0]						VFP[7:0]							
DA	IIE	IFA	x	ICV[5:0]					VST[7:0]								FSB[7:0]							
DB	DCT[8]	HDP[6:0]							DCT[7:0]								DCB[7:0]							
DC	CRH[7:0]								CGH[7:0]								CBH[7:0]							
DD	CRV[7:0]								CGV[7:0]								CBV[7:0]							
DE	FV1[5:0]								FV2[5:0]								FV3[5:0]							
DF	OLE	GLE	FIN	DIO	DIG	x	x	x	NOM[7:0]								TOL[7:0]							
E0	RCH[3:0]				RCV[3:0]				GCH[3:0]				GCV[3:0]				BCH[3:0]				BCV[3:0]			
E1	SRH[7:0]								SGH[7:0]								SBH[7:0]							
E2	SRV[7:0]								SGV[7:0]								SBV[7:0]							

4.2.2 Registers Not Storable in the EEPROM

	MSB							LSB																
	BYTE D0								**BYTE D1**								**BYTE D2**							
ADD	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
E3	STL	X	X	GCD	DHV	PPL	CDO	CDN	STV2050A code = 30(hex)								S01	S19	RESERVED				S02	S03
E4	X	PDC	PDB	PDA	X	POC	POB	POA	X	PLT	GOS	HVM	GAV [1:0]		GAH [1:0]		S01	S19	MSY	ELO	X	PIC	PIB	PIA
E5	OPI	ODS	OOS	ODT	X	X	X	X	S09 [3:0]				S10 [3:0]				S01	S19	S05	S11	S12 [3:0]			
E6	X	X	X	X	X	X	X	X	S13[7:0]								S14[7:0]							
E7	AIE	X	X	X	X	X	CBS [1:0]		X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	TE1
E8	MVR[7:0]								MVG[7:0]								MVB[7:0]							
E9	EEPRO-Madd [2:0]			X	X	X	ADS[1:0]		RWM [2:0]			X	HAM[3:0]				S01	S19	X	X	STX[3:0]			
EA	X	X	X	X	VDC	COV[2:0]			GCP	VHV	X	PAS[4:0]					X	X	X	X	X	X	X	X
EB	X	X	HO1 [5:0]						HG1[3:0]				X	X	HO2[5:0]						HG2[3:0]			
EC	X	X	VO1[5:0]						VG1[3:0]				X	X	VO2[5:0]						VG2[3:0]			
ED	X	X	HO3[5:0]						HG3[3:0]				X	X	HO4[5:0]						HG4[3:0]			
EE	X	X	VO3[5:0]						VG3[3:0]				X	X	VO4[5:0]						VG4[3:0]			
EF	X	X	X	X	X	RUE	RU1	RU2	X	X	X	X	TE2	TE3	TE4	RRP	X	X	X	X	X	X	0	0
FE	X	SSE	DTE	0	0	0	0	0	0	0	0	0	0	0	0	0	TBU[7:0]							

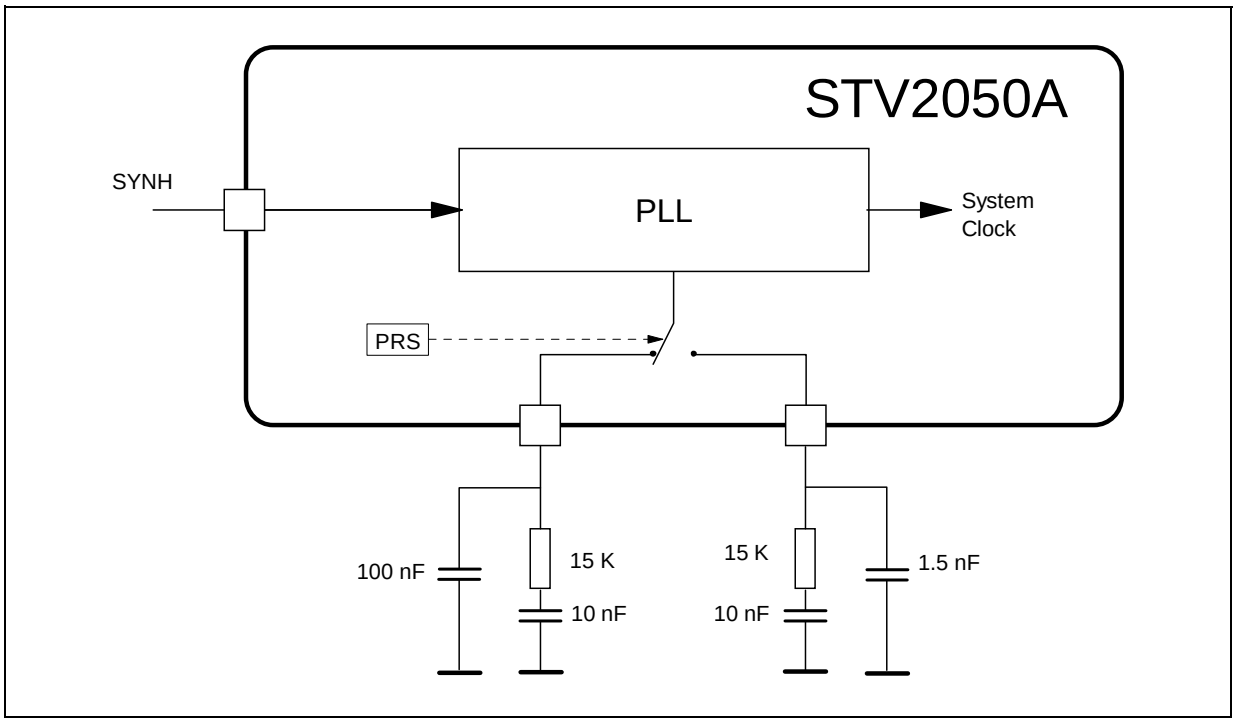
Note: X = Don't care, 0 or 1: The corresponding bit MUST be set to this value for normal operation.

5 TIMEBASES

5.1 LINE LOCKED PLL AND SYSTEM CLOCK

A frequency-multiplying PLL derives the internal ***system clock*** from the incoming signal at the SYNH pin. This signal is derived from horizontal deflection.

Figure 9. Line-Locked PLL and System Clock



The PLL is designed to drive 1H, 2H, HDTV and SVGA applications. Two loop filters can be implemented using the FILT (pin 24) and FLT2 (pin 25) pads. The selection can be forced by the PRS bit in the D5 register.

PRS	0 = FILT selected (2H and above range operation recommended) 1 = FLT2 selected (1H range operation recommended)

The horizontal deflection is often turned off when switching TV set modes. Therefore the PLL provides a base frequency when the external sync signal is missing (both H and V sync signals are missing).

The $N_{(clk/line)}$ ratio between the system clock and the incoming sync signal is calculated using the HGD[5:0] and HRD[5:0] values in the D8 register. (Refer to Section 7.2.1 "Horizontal Grid Adjustment" on page 35):

$$N_{(clk/line)} = 14 * (HGD+1) + 2 * (HRD+1)$$

where: $N_{(clk/line)} < 512$

$HGD > 15$

$HRD > 15$

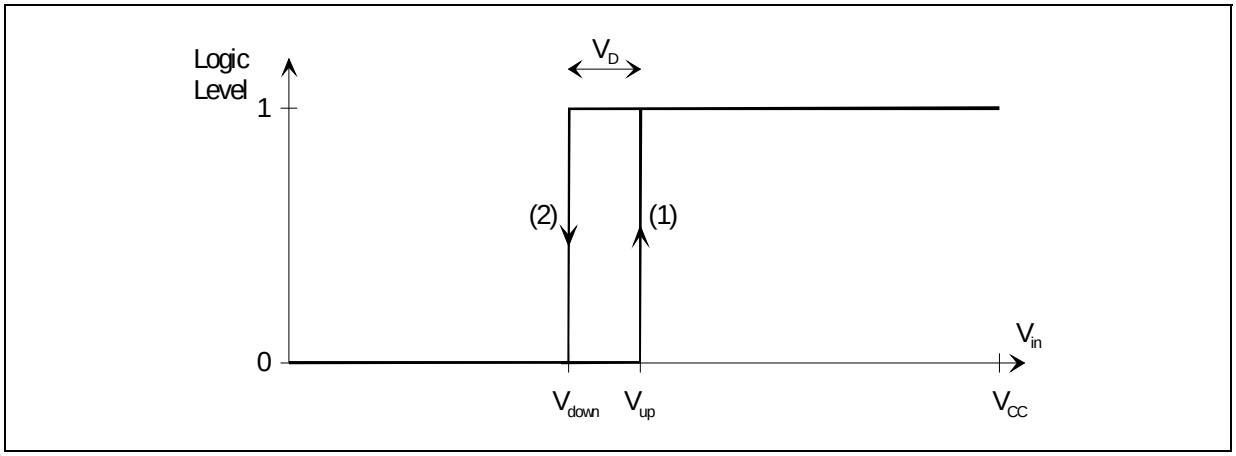
For all modes, in normal operation, the incoming timing signal at the SYNH pin will not have a phase deviation greater than ± 2 µs from line to line. Greater phase deviations may occur when switching modes or changing channels. The PLL is expected to recover from these events and lock within one vertical field of consistent phase that is within the normal horizontal operation limits.

5.2 SYNCHRONIZATION INPUTS

The two synchronization inputs, SYNH (pin 27) and SYNV (pin 28) slice the Line or the Frame Flyback, respectively, via a Schmitt trigger.

This also ensures a very stable detection of the synchronization signals, regardless of the temperature.

Figure 10. Synchronisation Signals



5.3 HORIZONTAL TIMEBASE

The horizontal timing is based on the built-in PLL.

5.3.1 Horizontal DAC Phase

In order to compensate the delay of the external amplifiers and the response time of the convergence coils (t_d), the values for convergence correction are given out prior to the corresponding horizontal video position. The time delay between video position and the output of

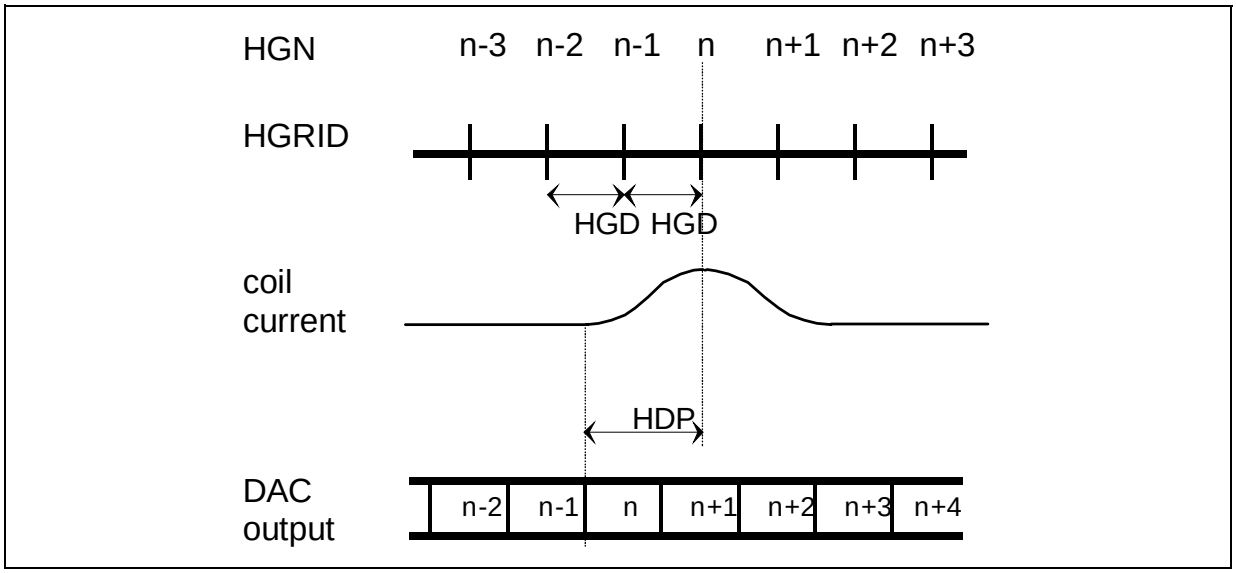
the corresponding convergence correction value is defined by the Horizontal DAC phase HDP[6:0] value in the DB register.

The following range for the horizontal DAC phase is allowed:

$$0 \leq HDP \leq 2 \times HGD$$

The timing of the DAC output leads the most if HDP is equal to zero.

Figure 11. Horizontal DAC Phase



5.3.2 Horizontal Width Adjustment

In order to fit the video pattern into the full visible area of the screen, the width of the pattern may be adjusted. Horizontal width adjustment is done by changing the number of clock cycles between the vertical grid lines during retrace and the visible grid. The timing for the corresponding DAC values is changed accordingly. Refer to Section 7.2.1 "Horizontal Grid Adjustment" on page 35.

5.3.3 Auto-Calibration of DACs

All the DACs of the STV2050A can be automatically calibrated. This feature ensures a high matching stability in both time and temperature. The process involves the sequential calibration of 120 cells.

To ensure optimal results, each cell must be calibrated at least every 4 ms.

The duration of one cell calibration must be greater than 2us. This duration is controlled by the internal “calibration clock”. The calibration clock is generated using a divider of the system clock. (Refer to Section 5.1 "LINE LOCKED PLL AND SYSTEM CLOCK" on page 22). The division ratio is programmable via the ACL[1:0] bits in D8.

ACL[1:0]	00: No calibration 01: Division by 16 10: Division by 32 11: Division by 48

Autocalibration can take place either during the full line, or during the line retrace only. This is controlled by the ACW bit in the D8 register.

ACW	0: During line retrace only 1: During the full line

If the “During Line Retrace Only” autocalibration is selected, the number of DAC cells calibrated during each line retrace is defined by the AFS[1:0] value in the D8 register.

AFS[1:0]	00: 1 cell / line 01: 2 cells / line 10: 3 cells / line 11: 4 cells / line

Two autocalibration modes can be selected by the AMS[0] bit in the D5 register.

AMS[0]	0: The autocalibration process is not synchronized to vertical timing 1: The autocalibration is synchronized to vertical IC timing. The counter which selects the DAC cells that are to be calibrated is reset on each frame retrace.

The time interval for auto-calibration is normally centred to the retrace. But it is possible to adjust the start point by programming the ASP[2:0] bits in the D8 register. One step corresponds to one system clock cycle.

5.4 VERTICAL TIME BASE

5.4.1 Vertical Synchronization Signal

The vertical timing is based on the vertical deflection signal. A debounce filter is implemented to prevent interference on the SYNV signal caused by crosstalk, mainly from horizontal deflection. This filter accepts a rising edge of the SYNV signal only when SYNV is 'LOW' for a time ≥ 8 TV lines (determined by 8 pulses at the SYNH input).

Figure 12. Vertical Synchronization Signal