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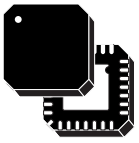
STW81100

MULTI-BAND RF FREQUENCY SYNTHESIZER WITH INTEGRATED VCOs

1 Features

- Integer-N Frequency Synthesizer
- Dual differential integrated VCOs with automatic central frequency calibration:
  - Direct Output:
    3300 – 3900 MHz
    3800 – 4400 MHz
  - Internal divider by 2:
    1650 – 1950 MHz
    1900 – 2200 MHz
  - Internal divider by 4:
    825 – 975 MHz
    950 – 1100 MHz
- Fast lock time: 150µs
- Dual modulus prescaler (64/65) and 2 programmable counters to achieve a feedback division ratio from 4096 to 32767.
- Programmable reference frequency divider (9 bits)
- Phase frequency comparator and charge pump
- Programmable charge pump current
- Digital Lock Detector
- I^2C bus interface with 3 bit programmable address ($1100A_2A_1A_0$)
- 3.3V Power Supply
- Power down mode
- Small size exposed pad VFQFPN28 package 5x5x1.0mm
- Process: BICMOS 0.35µm SiGe

Figure 1. Package



VFQFPN28

Table 1. Order Codes

Part Number	Package
STW81100AT-1	VFQFPN28
STW81100ATR-1	VFQFPN28 in Tape & Reel

2 Description

The STMicroelectronics STW81100 is an integrated RF synthesizer and voltage controlled oscillators (VCOs).

Showing high performance, high integration, low power, and multi-band performances, STW81100 is a low cost one chip alternative to discrete PLL and VCOs solutions.

STW81100 includes an Integer-N frequency synthesizer and two fully integrated VCOs featuring low phase noise performance and a noise floor of -153dBc/Hz. The combination of wide frequency range VCOs (thanks to center-frequency calibration over 32 sub-bands) and multiple output options (direct output, divided by 2 or divided by 4) allows to cover the 825MHz-1100MHz, the 1650MHz-2200MHz and the 3300MHz-4400MHz bands.

The STW81100 is designed with STMicroelectronics advanced 0.35µm SiGe process.

3 Applications

- Cellular 3G Infrastructure Equipment
- Other Wireless Communication Systems

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Figure 2. Block Diagram

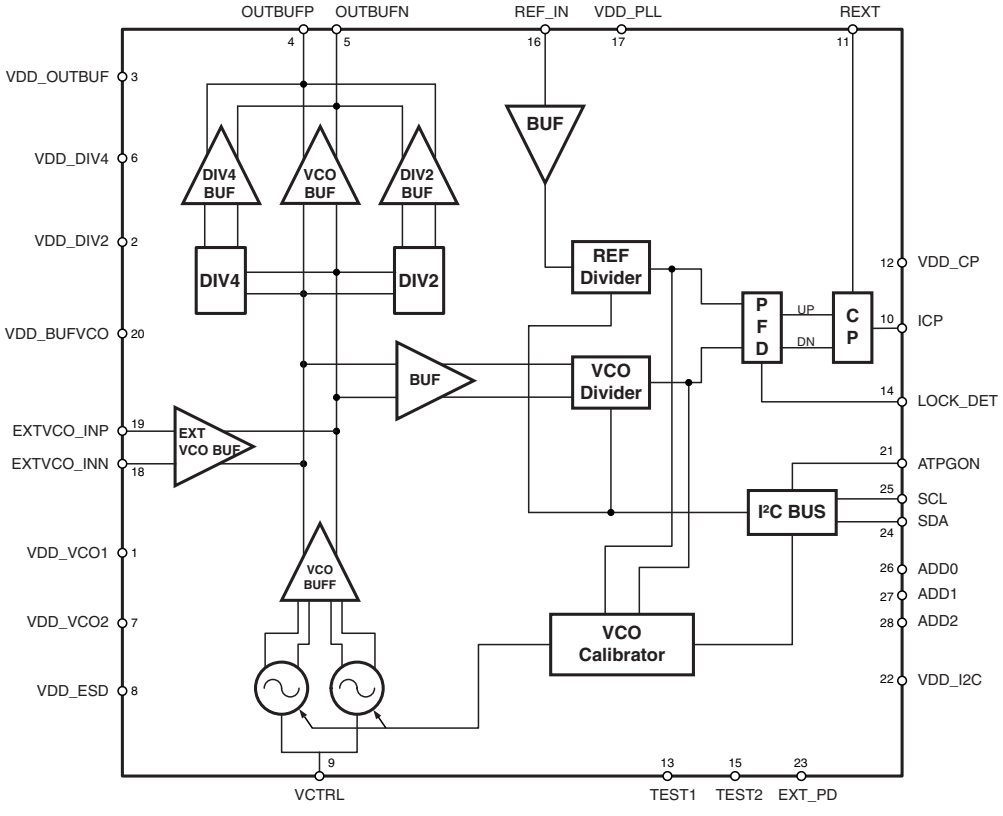


Figure 3. Pin Connections

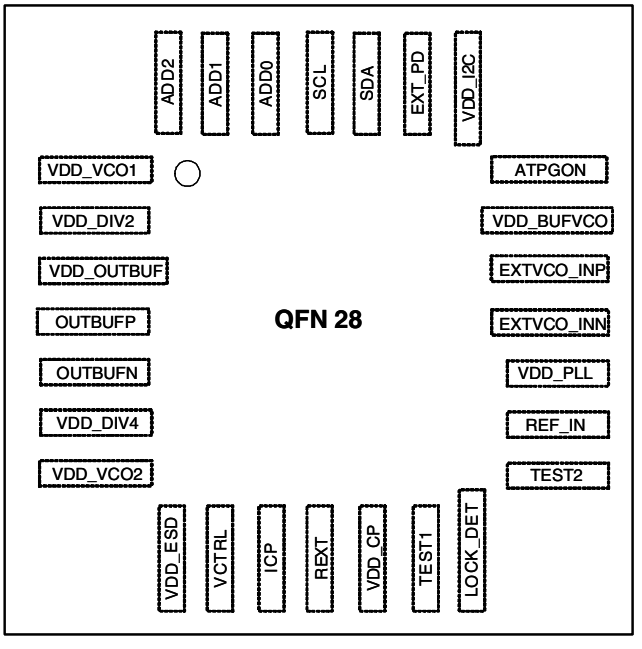


Table 2. Pin Description

Pin No	Name	Description	Observations
1	VDD_VCO1	VCO power supply	
2	VDD_DIV2	Divider by 2 power supply	
3	VDD_OUTBUF	Output buffer power supply	
4	OUTBUFP	LO buffer positive output	Open collector
5	OUTBUFN	LO buffer negative output	Open collector
6	VDD_DIV4	Divider by 4 power supply	
7	VDD_VCO2	VCO power supply	
8	VDD_ESD	ESD positive rail power supply	
9	VCTRL	VCO control voltage	
10	ICP	PLL charge pump output	
11	REXT	External resistance connection for PLL charge pump	
12	VDD_CP	Power supply for charge pump	
13	TEST1	Test input 1	Test purpose only; must be connected to GND
14	LOCK_DET	Lock detector	CMOS Output
15	TEST2	Test input 2	Test purpose only; must be connected to GND
16	REF_IN	Reference frequency input	
17	VDD_PLL	PLL digital power supply	
18	EXTVCO_INN	External VCO negative input	Test purpose only; must be connected to GND
19	EXTVCO_INP	External VCO positive input	Test purpose only; must be connected to GND
20	VDD_BUFVCO	VCO buffer power supply	
21	ATPGON	SCAN mode activated	Test purpose only; must be connected to GND
22	VDD_I^2C	I^2C bus power supply	
23	EXT_PD	Power down hardware	CMOS Input
24	SDA	I^2CBUS data line	CMOS Bidir Schmitt triggered
25	SCL	I^2CBUS clock line	CMOS Input
26	ADD0	I^2CBUS address select pin	CMOS Input
27	ADD1	I^2CBUS address select pin	CMOS Input
28	ADD2	I^2CBUS address select pin	CMOS Input

Table 3. Absolute Maximum Ratings

Symbol	Parameter	Values	Unit
AV_{CC}	Analog Supply voltage	0 to 4.6	V
DV_{CC}	Digital Supply voltage	0 to 4.6	V
T_{stg}	Storage temperature	+150	°C
ESD	Electrical Static Discharge - HBM [1] - CDM-JEDEC Standard	 2 0.5	KV

Note: 1. The maximum rating of the ESD protection circuitry on pin 4 and pin 5 is 800V with respect to other supply pins and 2KV with respect to ground.

Table 4. Operating Conditions

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
AV_{CC}	Analog Supply voltage		3.0	3.3	3.6	V
DV_{CC}	Digital Supply voltage		3.0	3.3	3.6	V
I_{CC}	Current Consumption				100	mA
T_{amb}	Operating ambient temperature		-40		85	°C
T_j	Maximum junction temperature				125	°C
$R_{th\ j\text{-}a}$	Junction to ambient package thermal resistance	Multilayer JEDEC board		35		°C/W

Table 5. Digital Logic Level[1]

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{il}	Low level input voltage				0.2*Vdd	V
V_{ih}	High level input voltage		0.8*Vdd			V
V_{hyst}	Schmitt trigger hysteresis		0.8			V
V_{ol}	Low level output voltage				0.4	V
V_{oh}	High level output voltage		0.85*Vdd			V

Note: 1. All parameters are guaranteed by design and characterization.

4 Electrical Characteristcs

All Electrical Specifications are intended at 3.3V supply voltage.

Table 6. Electrical Characteristcs

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
OUTPUT FREQUENCY RANGE						
F_{OUTA}	VCOA Frequency Range	Direct Output	3300		3900	MHz
		Divider by 2	1650		1950	MHz
		Divider by 4	825		975	MHz
F_{OUTB}	VCOB Frequency Range	Direct Output	3800		4400	MHz
		Divider by 2	1900		2200	MHz
		Divider by 4	950		1100	MHz

Table 6. Electrical Characteristcs (continued)

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
VCO DIVIDERS						
N	VCO Divider Ratio [1]		4096		32767	
REFERENCE and PHASE FREQUENCY DETECTOR						
f_{ref}	Reference input frequency		10	19.2	100	MHz
	Reference input sensitivity		0.35	1	1.5	Vpeak
f_{PFD}	PFD input frequency[4]				10	MHz
f_{step}	Frequency step[1]		F_{OUT}/ 32767		F_{OUT}/ 4096	Hz
CHARGE PUMP						
I_{CP}	ICP sink/source[2]	3bit programmable			4	mA
V_{OCP}	Output voltage compliance[4] range		0.4		V_{dd}-0.3	V
	Spurious[3,4]	Direct Output		-65	-54	dBc
		Divider by 2		-70	-60	dBc
		Divider by 4		-70	-66	dBc
VCOs						
$Kvco_A$	VCOA sensitivity[3,4]	Sub-Band 00000	85	105	135	MHz/V
		Sub-Band 01111	55	70	95	MHz/V
		Sub-Band 11111	35	50	65	MHz/V
$Kvco_B$	VCOB sensitivity[3,4]	Sub-Band 00000	60	75	100	MHz/V
		Sub-Band 01111	35	45	60	MHz/V
		Sub-Band 11111	20	25	35	MHz/V
	VCO_A Pushing[3,4]			7	10	MHz/V
	VCO_B Pushing[3,4]			9	14	MHz/V
	VCO control voltage[4]		0.4		3	V
	LO Harmonic Spurious[4]				-20	dBc
	VCO current consumption			25		mA
	VCO buffer consumption			15		mA
I_{DIV2}	DIVIDER by 2 consumption			18		mA
I_{DIV4}	DIVIDER by 4 consumption			14		mA
LO OUTPUT BUFFER						
P_{OUT}	Output level			0		dBm
RL	Return Loss[4]	Matched to 50ohm		15		dB

Table 6. Electrical Characteristcs (continued)

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
I_{LOBUF}	Current Consumption	DIV4 Buff		26		mA
		DIV2 Buff		23		mA
		Direct Output		37		mA
EXTERNAL VCO (Test purpose only)						
f_{INVCO}	Frequency range		3.3		4.4	GHz
P_{IN}	Input level		0		+6	dBm
V_{INDC}	DC Input level			2		V
I_{EXTBUF}	Current Consumption	VCO Internal Buffer		15		mA
PLL MISCELLANEOUS						
I_{PLL}	Current Consumption	Input Buffer, Prescaler, Digital Dividers, misc		10		mA
t_{LOCK}	Lock up time[4]	40 KHz PLL bandwidth; within 1 ppm of frequency error		150		µs

Notes: 1. Frequency step higher than $F_{OUT}/4096$ (i.e. N values less than 4096) can be used but it is not guaranteed the channel contiguity (Only configurations with B>A and $f_{PFD} \leq 10$ MHz are allowed)
2. see relationship between ICP and REXT in the Circuit Description section (Charge Pump)
3. PFD frequency leakage (400KHz) and harmonics
4. Guaranteed by design and characterization.

Table 7. Phase Noise Performance[1]

Parameter	Test Condition	Min	Typ	Max	Units
In Band Phase Noise – Closed Loop[2]					
Normalized In Band Phase Noise Floor	ICP= 2mA, PLL BW = 50KHz; including reference clock contribution		-212		dBc/Hz
In Band Phase Noise Floor Direct Output		-212+20log(N)+10log(f_{PFD})			dBc/Hz
In Band Phase Noise Floor Divider by 2		-218+20log(N)+10log(f_{PFD})			dBc/Hz
In Band Phase Noise Floor Divider by 4		-224+20log(N)+10log(f_{PFD})			dBc/Hz
PLL Integrated Phase Noise with Divider by 2					
Integrated Phase Noise (single sided) 400Hz to 4MHz	ICP = 4mA, f_{PFD} = 400KHz (N = 10000), PLL BW = 15KHz		-39	-37	dBc
Integrated Phase Noise (single sided) 100Hz to 25MHz			-38	-36	dBc
VCO A Direct (3300MHz-3900MHz) – Open Loop					
Phase Noise @ 1 KHz			-56	-53	dBc/Hz
Phase Noise @ 10 KHz			-83	-82	dBc/Hz
Phase Noise @ 100 KHz			-105	-102	dBc/Hz
Phase Noise @ 1 MHz			-128	-125	dBc/Hz
Phase Noise @ 10 MHz			-148	-145	dBc/Hz
Phase Noise @ 40 MHz			-156	-153	dBc/Hz

Table 7. Phase Noise Performance[1] (continued)

Parameter	Test Condition	Min	Typ	Max	Units
VCO B Direct (3800MHz-4400MHz) – Open Loop					
Phase Noise @ 1 KHz			-55	-52	dBc/Hz
Phase Noise @ 10 KHz			-82	-79	dBc/Hz
Phase Noise @ 100 KHz			-104	-101	dBc/Hz
Phase Noise @ 1 MHz			-127	-124	dBc/Hz
Phase Noise @ 10MHz			-147	-143	dBc/Hz
Phase Noise @ 40 MHz			-155	-152	dBc/Hz
VCO A with divider by 2 (1650MHz-1950MHz) – Open Loop					
Phase Noise @ 1 KHz			-62	-59	dBc/Hz
Phase Noise @ 10 KHz			-89	-86	dBc/Hz
Phase Noise @ 100 KHz			-111	-108	dBc/Hz
Phase Noise @ 1 MHz			-134	-131	dBc/Hz
Phase Noise @ 10 MHz			-150	-148	dBc/Hz
Phase Noise @ 20 MHz			-152	-150	dBc/Hz
Phase Noise Floor @ 40 MHz			-153	-151	dBc/Hz
VCO B with divider by 2 (1900MHz-2200MHz) – Open Loop					
Phase Noise @ 1 KHz			-61	-58	dBc/Hz
Phase Noise @ 10 KHz			-88	-85	dBc/Hz
Phase Noise @ 100 KHz			-110	-107	dBc/Hz
Phase Noise @ 1 MHz			-133	-130	dBc/Hz
Phase Noise @ 10MHz			-150	-148	dBc/Hz
Phase Noise @ 20MHz			-152	-150	dBc/Hz
Phase Noise Floor @ 40 MHz			-153	-151	dBc/Hz
VCO A with divider by 4 (825MHz-975MHz) – Open Loop					
Phase Noise @ 1 KHz			-68	-65	dBc/Hz
Phase Noise @ 10 KHz			-95	-92	dBc/Hz
Phase Noise @ 100 KHz			-117	-114	dBc/Hz
Phase Noise @ 1 MHz			-139	-136	dBc/Hz
Phase Noise @ 10MHz			-151	-149	dBc/Hz
Phase Noise Floor @ 40 MHz			-153	-151	dBc/Hz
VCO B with divider by 4 (950MHz-1100MHz) – Open Loop					
Phase Noise @ 1 KHz			-67	-64	dBc/Hz
Phase Noise @ 10 KHz			-94	-91	dBc/Hz
Phase Noise @ 100 KHz			-116	-113	dBc/Hz
Phase Noise @ 1 MHz			-138	-135	dBc/Hz
Phase Noise @ 10MHz			-151	-149	dBc/Hz
Phase Noise Floor @ 40 MHz			-153	-151	dBc/Hz

Note 1: Phase Noise SSB.
VCO amplitude set to maximum value [11].
The phase noise is measured with the Agilent E5052A Signal Source Analyzer.
All the closed-loop performances are specified using a Reference Clock signal at 19.2 MHz with phase noise of -141dBc/Hz @1KHz offset and -146dBc/Hz @10KHz offset. All figures are guaranteed by design and characterization.

Note 2: Normalized PN = Measured PN - 20log(N) - 10log(f_{PFD}) where N is the VCO divider ratio (N=B*P+A) and f_{PFD} is the comparison frequency at the PFD input

5 Typical Performance Characteristics

The phase noise is measured with the Agilent E5052A Signal Source Analyzer. All the closed-loop measurements are done with f_{PFD} = 800 KHz and using a Reference Clock signal at 19.2 MHz with phase noise of -141dBc/Hz @1KHz offset and -146dBc/Hz @10KHz offset.

Figure 4. VCO A (Direct output) open loop phase noise

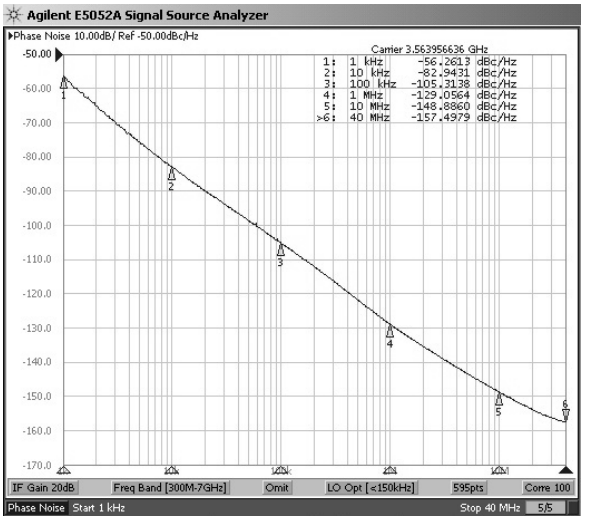


Figure 5. VCO A (Direct output) closed loop phase noise

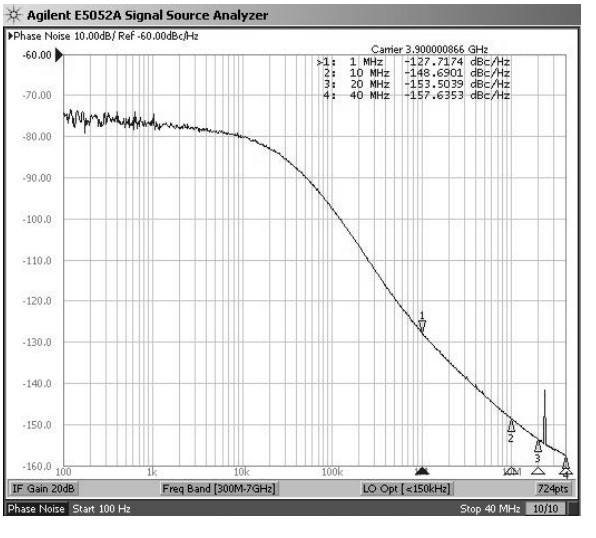


Figure 6. VCO B (Direct output) open loop phase noise

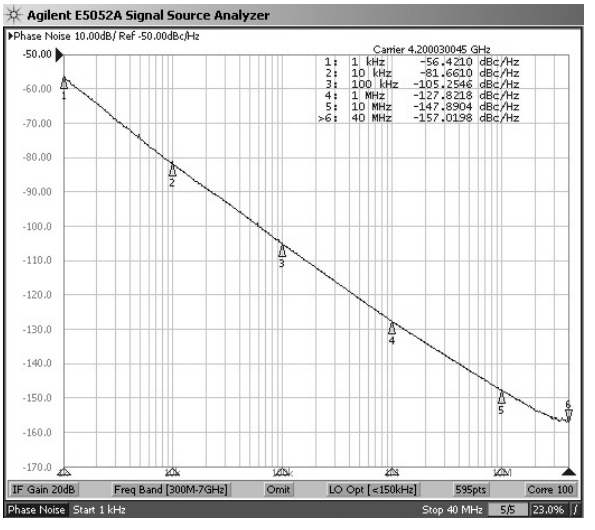


Figure 7. VCO B (Direct output) closed loop phase noise

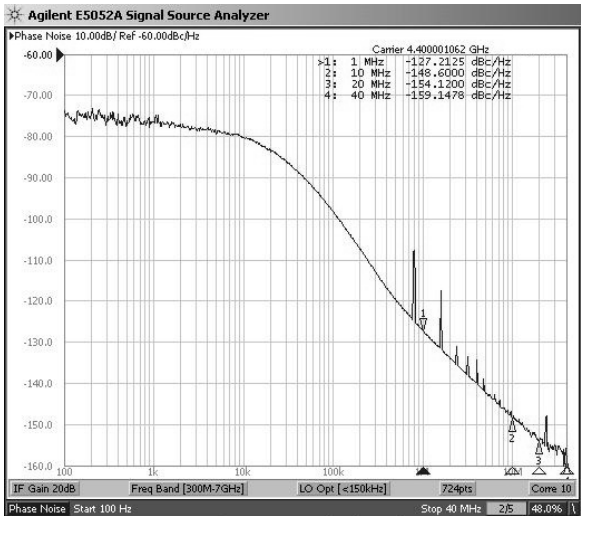


Figure 8. VCO A (Divider by 2 output) closed loop phase noise

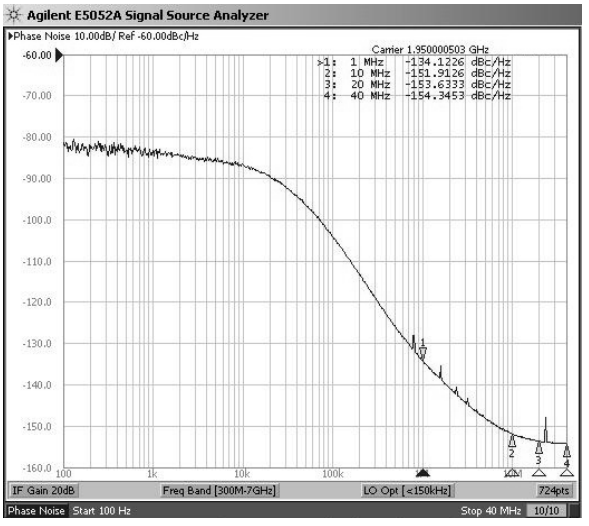


Figure 9. VCO A (Divider by 4 output) closed loop phase noise

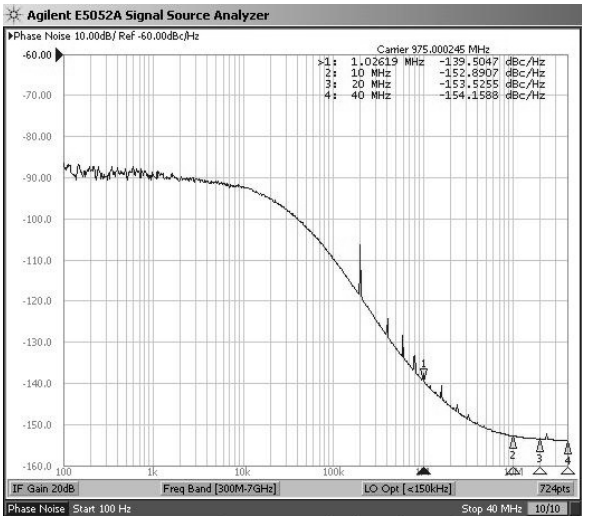


Figure 10. VCO B (Divider by 2 output) closed loop phase noise

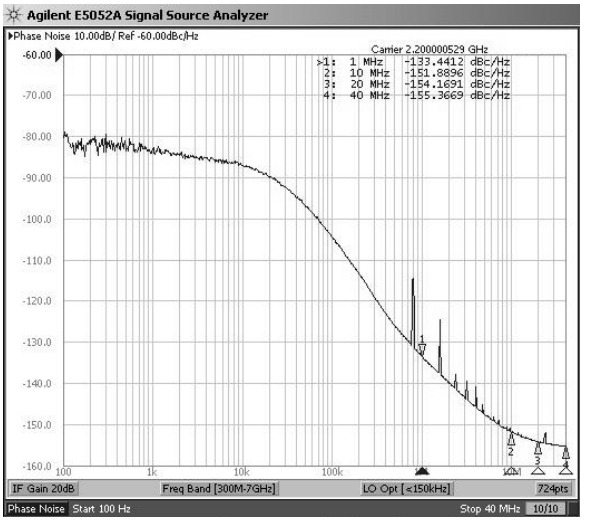
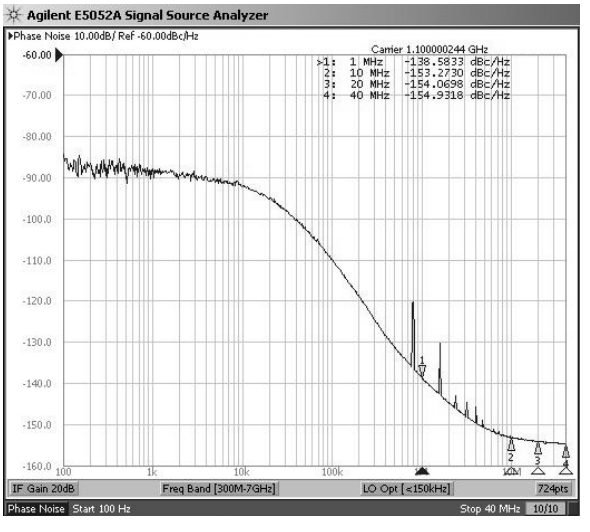


Figure 11. VCO B (Divider by 4 output) closed loop phase noise



6 General Description

The block diagram of *Figure 2* shows the different blocks, which have been integrated to achieve an integer-N PLL frequency synthesizer.

The STW81100 consists of 2 internal low-noise VCOs with buffer blocks, a divider by 2, a divider by 4, a low-noise PFD (Phase Frequency Detector), a precise charge pump, a 9-bit programmable reference divider, two programmable counters and a dual-modulus prescaler.

The A-counter (6 bits) and B counter (9 bits) counters, in conjunction with the dual modulus prescaler P/P+1 (64/65), implement an N integer divider, where N = B*P +A.

The division ratio of both reference and VCO dividers is controlled through an I^2C bus interface.

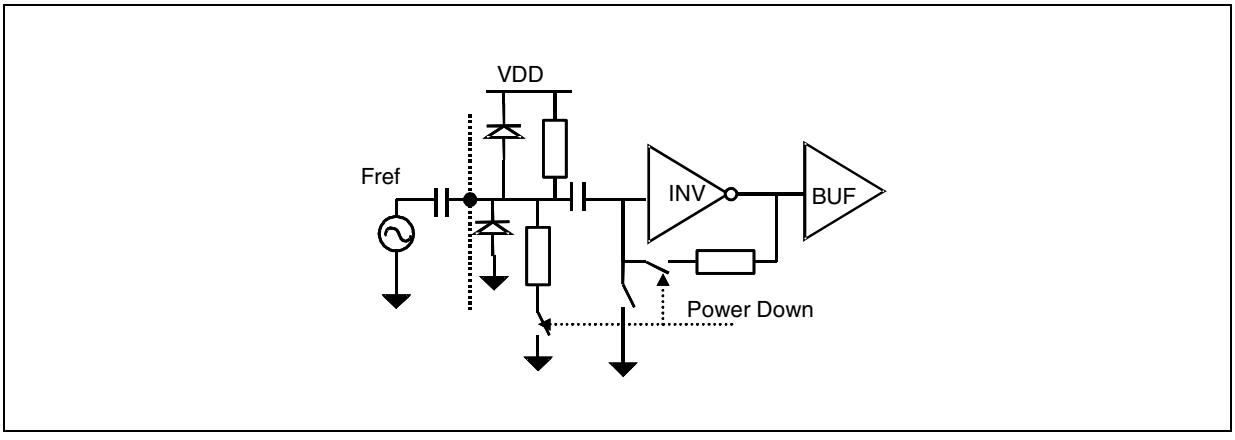
All devices operate with a power supply of 3.3 V and can be powered down when not in use.

7 Circuit Description

7.1 Reference input stage

The reference input stage is shown in *Figure 12*. The resistor network feeds a DC bias at the Fref input while the inverter used as the frequency reference buffer is AC coupled.

Figure 12. Reference Frequency Input Buffer



7.2 Reference Divider

The 9-bit programmable reference counter allows the input reference frequency to be divided to produce the input clock to the PFD. The division ratio is programmed through the I^2C bus interface.

7.3 Prescaler

The dual-modulus prescaler 64/65 takes the CML clock from the VCO buffer and divides it down to a manageable frequency for the CMOS A and B counters. It is based on a synchronous 4/5 core which division ratio depends on the state of the modulus input.

7.4 A and B Counters

The A (6 bits) and B (9 bits) counters, in conjunction with the dual modulus prescaler make it possible to generate output frequencies which are spaced only by the reference frequency divided by the reference division ratio. Thus, the division ratio and the VCO output frequency are given by these formulas:

$N = B \times P + A$

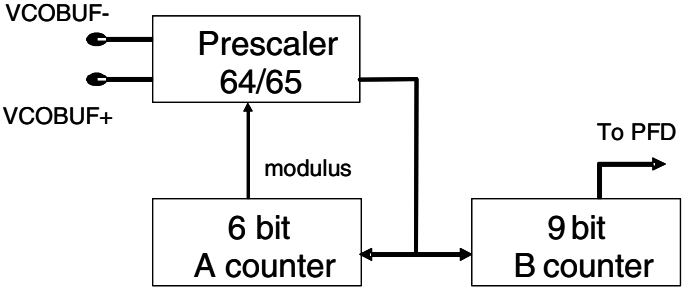
$$F_{VCO} = \frac{(B \cdot P + A) \cdot F_{ref}}{R}$$

where:

- FVCO: output frequency of VCO.
- P: modulus of dual modulus prescaler.
- B: division ratio of the main counter.
- A: division ratio of the swallow counter.
- Fref: input reference frequency.
- R: division ratio of reference counter.
- N: division ratio of PLL

For a correct work of the VCO divider, B must be strictly higher than A. A can take any value ranging from 0 to 63. The range of the N number can vary from 4096 to 32767.

Figure 13. VCO Divider Diagram

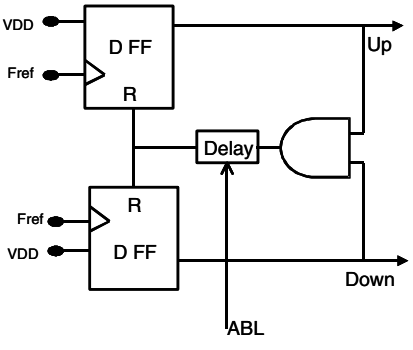


7.5 Phase frequency detector (PFD)

The PFD takes inputs from the reference and the VCO dividers and produces an output proportional to the phase error. The PFD includes a delay gate that controls the width of the anti-backlash pulse. This pulse ensures that there is no dead zone in the PFD transfer function.

Figure 14 is a simplified schematic of the PFD.

Figure 14. PFD Diagram



7.6 Lock Detect

This signal indicates that the difference between rising edges of both UP and DOWN PFD signals is found to be shorter than the fixed delay (roughly 5 ns). Lock Detect signal is high when the PLL is locked.

When Power Down is activated, Lock Detect is let to high level (Lock Detect consumes current only during PLL transients).

7.7 Charge Pump

This block drives two matched current sources, Iup and Idown, which are controlled respectively by UP and DOWN PFD outputs. The nominal value of the output current is controlled by an external resistor (to be connected to the REXT input pin) and a selection among 8 by a 3 bit word.

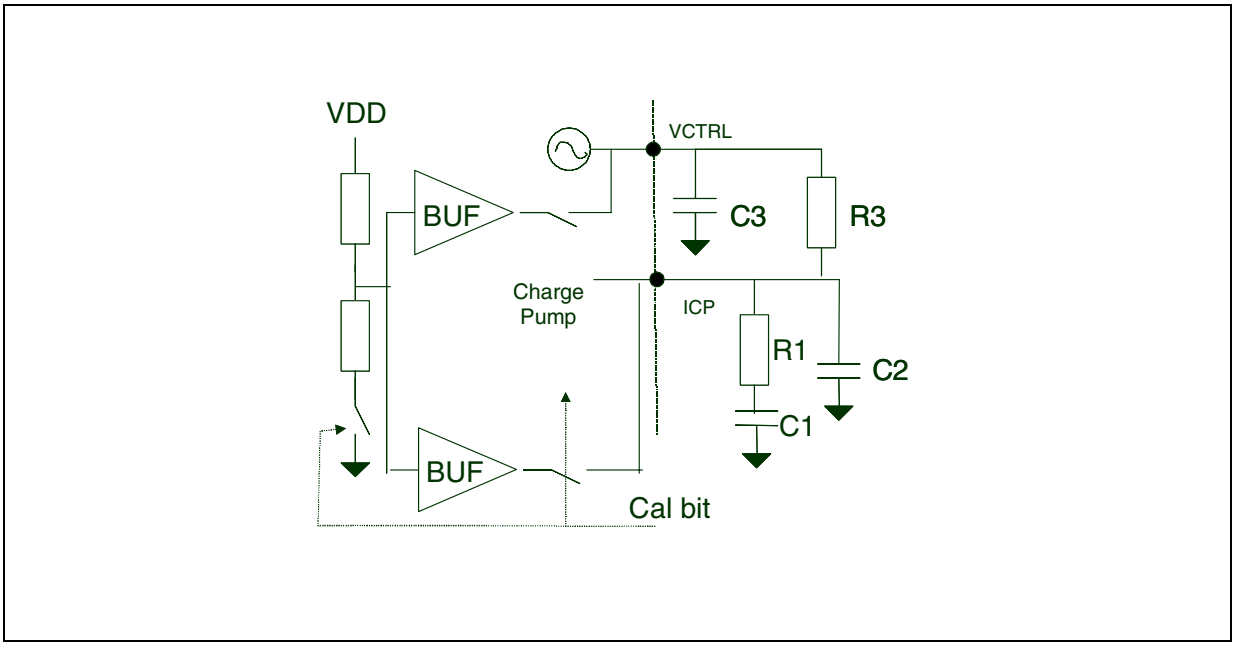
The minimum value of the output current is: I_{MIN} = 2*VBG/REXT (VBG~1.17 V)

Table 8. Current Value vs Selection

CPSEL2	CPSEL1	CPSEL0	Current	Value for REXT=9.1 KΩ
0	0	0	I_{MIN}	0.25 mA
0	0	1	$2*I_{MIN}$	0.50 mA
0	1	0	$3*I_{MIN}$	0.75 mA
0	1	1	$4*I_{MIN}$	1.00 mA
1	0	0	$5*I_{MIN}$	**1.25 mA**
1	0	1	$6*I_{MIN}$	1.50 mA
1	1	0	$7*I_{MIN}$	1.75 mA
1	1	1	$8*I_{MIN}$	2.00 mA

Note: The current is output on pin ICP. During the VCO auto calibration, ICP and VCTRL pins are forced to VDD/2.

Figure 15. Loop Filter Connection



7.8 Voltage Controlled Oscillators

7.8.1 VCO Selection

Within STW81100 two low-noise VCOs are integrated to cover a wide band from 3300MHz to 4400MHz (direct output), from 1650MHz to 2200MHz (selecting divider by 2) and from 825MHz to 1100MHz (selecting divider by 4).

VCO A frequency range 3300MHz-3900MHz

VCO B frequency range 3800MHz-4400MHz

7.8.2 VCO Frequency Calibration

Both VCOs can operate on 32 frequency ranges that are selected by adding or subtracting capacitors to the resonator. These frequency ranges are intended to cover the wide band of operation and compensate for process variation on the VCO center frequency.

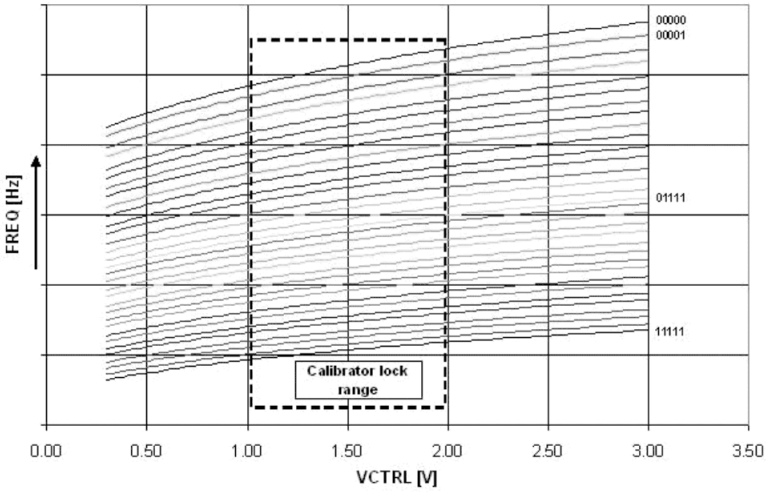
An automatic selection of the range is performed when the bit SERCAL rises from “0” to “1”. The charge pump is inhibited and the pins ICP & VCTRL are at VDD/2 volts.

Then the ranges are tested to select the one which with this VCO input voltage is the nearest to the desired output frequency (Fout = N*Fref/R). When this selection is achieved the signal ENDCALB (which means End of Calibration) falls to “0”, then the charge pump is enabled again and SERCAL should be reset to “0” before the next channel step.

The reference clock signal at the REF_IN input terminal must be running before starting the calibration.

The PLL has just to perform fine adjustment around VDD/2 on the loop filter to reach Fout, which enables a fast settle.

Figure 16. VCO Sub-Bands Frequency Characteristics



The SERCAL bit should be set to “1” at each division ratio change. It should be noted that in order to reset the autocalibrator State Machine after a power-up, and anyway before the first calibration, the INITCAL bit should be set to “1” and back to “0” (this operation is automatically performed by the Power On Reset circuitry). The calibration takes approximately 7 periods of the PFD Frequency.

The maximum allowed f_{PFD} to perform the calibration process is 1 MHz. Using an higher f_{PFD} the following procedure should be adopted:

1. Calibrate the VCO at the desired frequency with an f_{PFD} less than 1 MHz
2. Set the A, B and R dividers ratio for the desired f_{PFD}

7.8.3 VCO Voltage Amplitude Control

The bits A0 and A1 control the voltage swing of the VCO. The following table gives the voltage level expected on the resonator nodes.

Table 9.

Code A[1:0]	Differential output voltage (Vp)
00	1.1
01	1.3
10	1.9
11	2.1

8 I²C bus interface

Data transmission from microprocessor to the STW81100 takes place through the 2 wires (SDA and SCL) I²C-BUS interface. The STW81100 is always a slave device.

The I²C-bus protocol defines any device that sends data on to the bus as a transmitter and any device that reads the data as receiver. The device that controls the data transfer is known as the Master and the others as the slave. The master will always initiate the transfer and will provide the serial clock for synchronization.

8.1 General Features

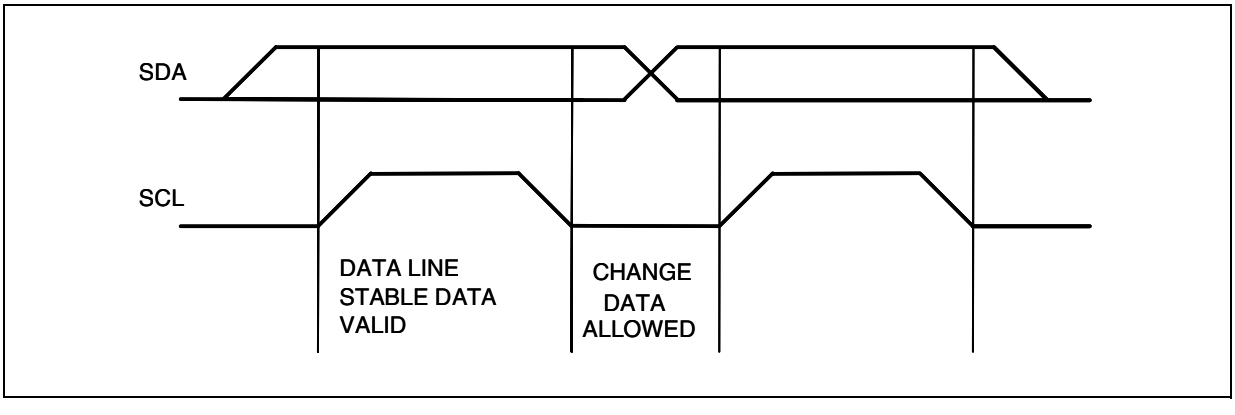
8.1.1 Power ON Reset

The device at Power ON is able to configure itself to a fixed configuration, with all programmable bits set to factory default setting.

8.1.2 Data Validity

Data changes on the SDA line must only occur when the SCL is LOW. SDA transitions while the clock is HIGH are used to identify START or STOP condition.

Figure 17.



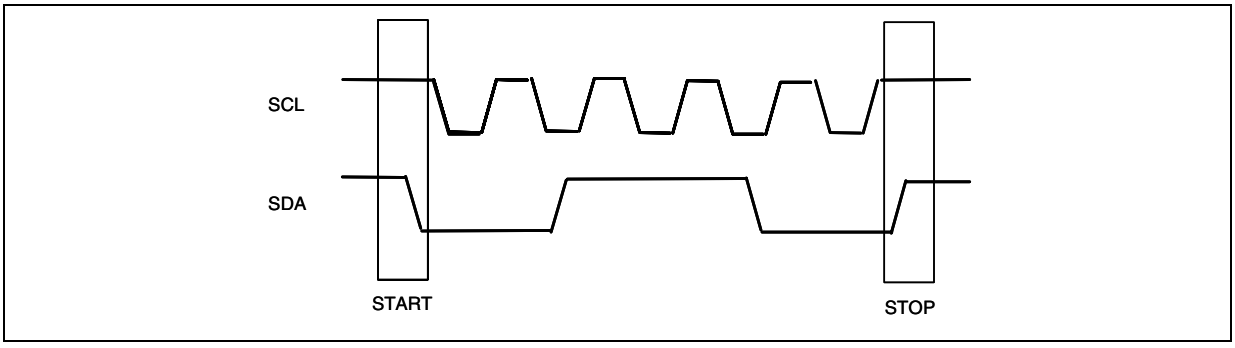
8.1.3 START condition

A Start condition is identified by a HIGH to LOW transition of the data bus SDA while the clock signal SCL is stable in the HIGH state. A Start condition must precede any command for data transfer.

8.1.4 STOP condition

A LOW to HIGH transition of the data bus SDA identifies start while the clock signal SCL is stable in the HIGH state. A STOP condition terminates communications between the STW81100 and the Bus Master.

Figure 18.

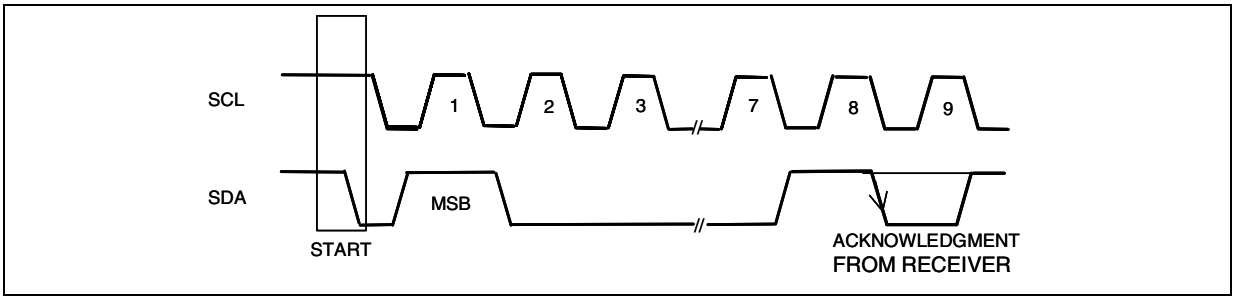


8.1.5 Byte format and acknowledge

Every byte transferred on the SDA line must contain bits. Each byte must be followed by an acknowledge bit. The MSB is transferred first.

An acknowledge bit is used to indicate a successful data transfer. The bus transmitter, either master or slave, will release the SDA bus after sending 8 bits of data. During the 9th clock pulse the receiver pulls the SDA low to acknowledge the receipt of 8 bits data.

Figure 19.



8.1.6 Device addressing

To start the communication between the Master and the STW81100, the master must initiate with a start condition. Following this, the master sends onto the SDA line 8 bits (MSB first) corresponding to the device select address and read or write mode.

The first 7 MSB's are the device address identifier, corresponding to the I^2C-Bus definition. For the STW81100 the address is set as "$1100A_2A_1A_0$", 3bits programmable. The 8th bit (LSB) is the read or write operation bit (RW; set to 1 in read mode and to 0 in write mode).

After a START condition the STW81100 identifies on the bus the device address and, if matched, it will acknowledge the identification on SDA bus during the 9th clock pulse.

8.1.7 Single-byte write mode

Following a START condition the master sends a device select code with the RW bit set to 0. The STW81100 gives an acknowledge and waits for the internal sub-address (1 byte). This byte provides access to any of the internal registers.

After the reception of the internal byte sub-address the STW81100 again responds with an acknowledge. A single byte write with sub-address 00H will change the "FUNCTIONAL MODE" register; therefore a "single byte write" operation with sub-address 04H will change the "CALIBRATION" register and so on.

Table 10.

S	$1100A_2A_1A_0$	0	ack	sub-address byte	ack	DATA IN	ack	P

8.1.8 Multi-byte write mode

The multi-byte write mode can start from any internal address. The master sends the data bytes and each one is acknowledged. The master terminates the transfer by generating a STOP condition.

The sub-address decides the starting byte. A Multi-byte with sub-address 01H and 2 DATA_IN bytes will change the “B_COUNTER” and “A_COUNTER” registers, so a Multi-byte with sub-address 00H and 6 DATA_IN bytes will change all the STW81100 registers.

Table 11.

S	$1100A_2A_1A_0$	0	ack	sub-address byte	ack	DATA IN	ack	....	DATA IN	ack	P

8.1.9 Current Byte Address Read

In the current byte address read mode, following a START condition, the master sends the device address with the rw bit set to 1 (No sub-address is needed as there is only 1 byte read register). The STW81100 acknowledges this and outputs the data byte. The master does not acknowledge the received byte, but terminates the transfer with a STOP condition.

Table 12.

S	1100 A_2 A_1 A_0	1	ack	DATA	No ack	P

8.2 Timing Specification

Figure 20. Data and clock

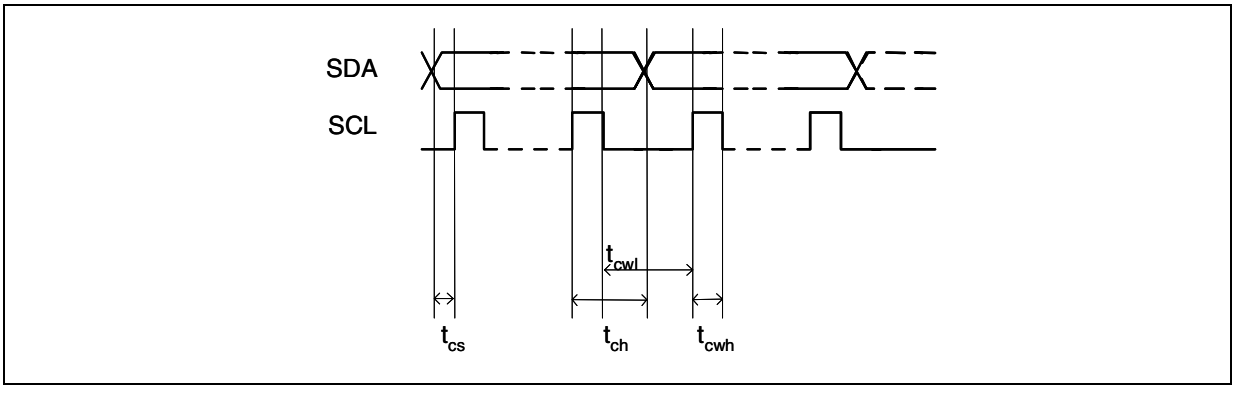


Table 13.

Symbol	Parameter	Minimum time (ns)
T_{cs}	Data to clock set up time	2
T_{ch}	Data to clock hold time	2
T_{cwh}	Clock pulse width high	10
T_{cwl}	Clock pulse width low	5

Figure 21. Start and Stop

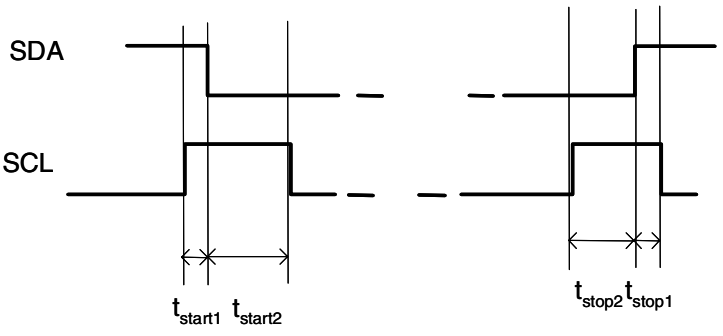


Table 14.

Symbol	Parameter	Minimum time (ns)
$T_{start1,2}$	Clock to data start time	2
$T_{stop1,2}$	Data to clock down stop time	2

Figure 22. Ack

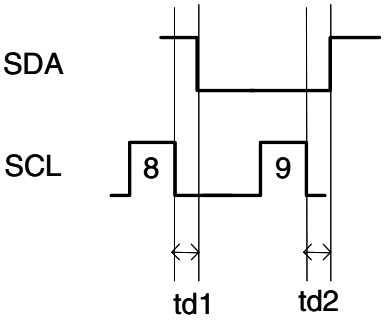


Table 15.

Symbol	Parameter	Maximum time (ns)
T_{d1}	Ack begin delay	2
T_{d2}	Ack end delay	2

8.3 I^2C Register

STW81100 has 6 write-only registers and 1 read-only register.

The following table gives a short description of the write-only registers list.

Table 16.

HEX CODE	DEC CODE	DESCRIPTION
0x00	0	FUNCTIONAL_MODE
0x01	1	B_COUNTER
0x02	2	A_COUNTER
0x03	3	REF_DIVIDER
0x04	4	CALIBRATION
0x05	5	CONTROL

Table 17. Functional_Mode

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0
PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

FUNCTIONAL_MODE register is used to select different functional mode for the STW81100 synthesizer according to the following table:

Table 18.

Decimal value	Description
0	Power down mode
1	Enable VCO A, output frequency divided by 2
2	Enable VCO B, output frequency divided by 2
3	Enable external VCO, output frequency divided by 2 (Test purpose only)
4	Enable VCO A, output frequency divided by 4
5	Enable VCO B, output frequency divided by 4
6	Enable external VCO, output frequency divided by 4 (Test purpose only)
7	Enable VCO A, direct output
8	Enable VCO B, direct output
9	Enable external VCO, direct output (Test purpose only)

Table 19. B_COUNTER

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0
B8	B7	B6	B5	B4	B3	B2	B1

B[8:1] Counter value (bit B0 in the next register)

Table 20. A_COUNTER

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0
B0	A5	A4	A3	A2	A1	A0	R8

Bit B0 for B Counter, A Counter value and bit R8 for Reference divider.

Table 21. REF_DIVIDER

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0
R7	R6	R5	R4	R3	R2	R1	R0

Reference Clock divider ratio R[7:0] (bit R8 in the previous register).

The LO output frequency is programmed by setting the proper value for A,B and R according to the following formula:

$$F_{OUT} = D_R \cdot (B \cdot 64 + A) \cdot \frac{F_{REF\_CLK}}{R}$$

where D_R equals
- 1 for Direct Output
- 0.5 for Output Divided by 2
- 0.25 for Output Divided by 4

Table 22. Calibration

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0
INIT CAL	SER CAL	SEL EXT CAL	CAL 0	CAL 1	CAL 2	CAL 3	CAL 4

This register controls VCO calibrator.

INITCAL: resets the auto-calibrator State Machine (writing to “1” and back to “0”)

SERCAL: at “1” starts the VCO auto-calibration (should be reset to “0” at the end of calibration)

SELEXTCAL: test purpose only; must be set to '0'

CAL[4:0]: test purpose only; must be set to '0'

Table 23. CONTROL

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0
PLL_A0	PLL_A1	CP SEL 0	CP SEL 1	CP SEL 2	NA	NA	NA

The CONTROL register is used to set the VCO output voltage amplitude and the Charge Pump Current.

PLL_A[1:0]: VCO amplitude

CPSEL[2:0]: Charge Pump output current

Table 24. READ-ONLY REGISTER

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0
ILLEGAL_SUBAD0	END CALB	LOCK_DET	INT CAL4	INT CAL3	INT CAL2	INT CAL1	INT CAL0

This register is automatically addressed in the 'current byte address read mode'.

ILLEGAL_SUBADD: gives "1" if the sub-address value is not correct

ENDCALB: at "0" means end of auto-calibration phase

LOCK_DET: "1" when PLL is locked

INTCAL[4:0]: internal value of the VCO control word

9 Application Information

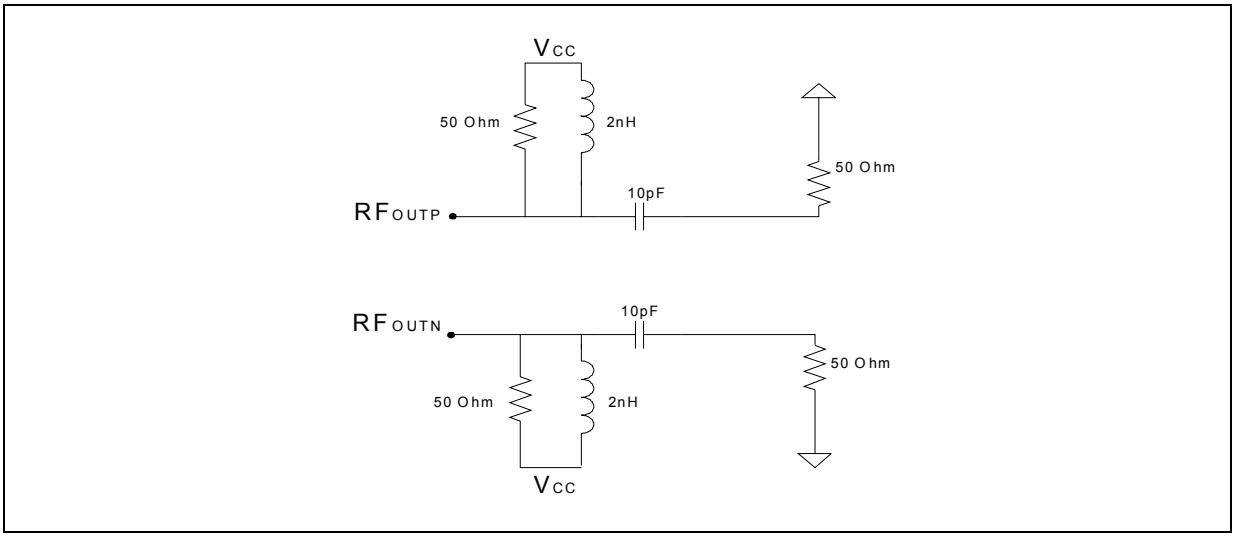
The STW81100 features three different alternatively selectable bands: direct output (3.3 to 4.4GHz), divided by 2 (1.65 to 2.2GHz) and divided by 4 (850 to 1100MHz). In order to achieve a suitable power level, a good matching network is needed to adapt the output stage to a 50Ω load. Moreover, since most of commercial RF components have single ended input and output terminations, a differential to single ended conversion could be required.

Below different matching configurations for the three bands are suggested as a guideline for the customer to design its own application board.

9.1 Direct output

If a differential to single conversion is not needed it is possible to match the output buffer of the STW81100 in the simple way shown in *Figure 23*.

Figure 23. Differential/single ended output network in the 3.3 - 4.4GHz range

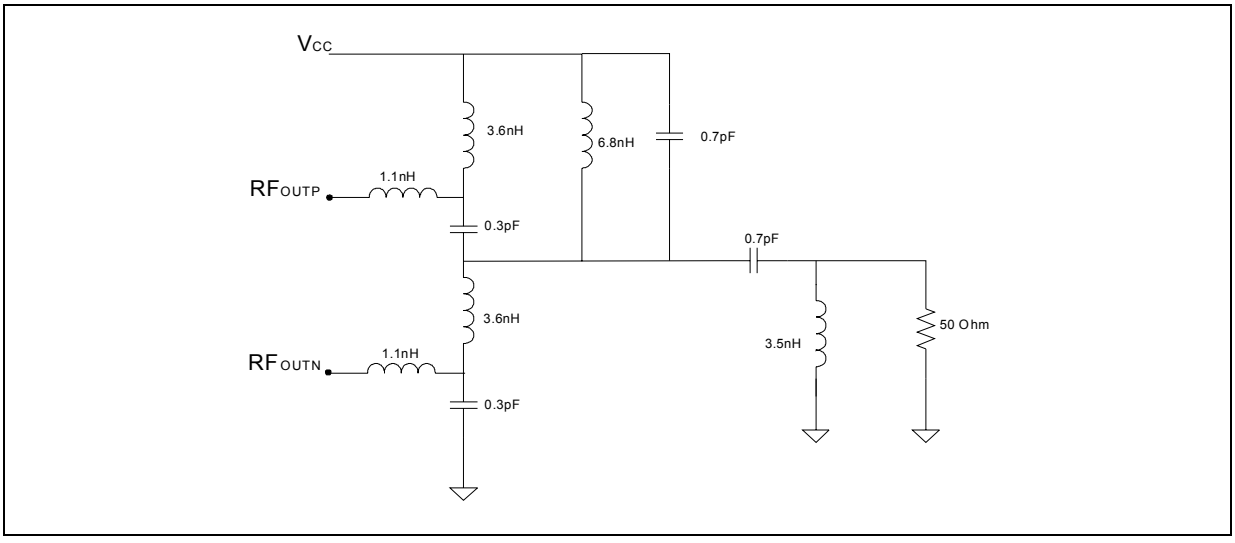


Since most of discrete components for microwave applications are single ended, the user can easily use one of the two outputs and terminate the other one to 50Ω with a 3dB power loss.

Alternatively it is possible to combine the 2 outputs in different ways. A first topology for the direct output (3.3GHz to 4.4GHz) is suggested in *Figure 24*. It basically consists of a simple LC balun and a matching network to adapt the output to a 50Ω load. The two LC networks shift output signal phase of -90° and +90° thus combining the 2 outputs. The LC balun is designed for a center frequency of 4GHz and exhibits ap-

proximately 2dBm output power over the whole band. This topology is intrinsically narrow band, since the LC balun is tuned at a single frequency. If the application requires a different sub-band, the LC combiner could be easily adjusted to be tuned at the frequency of interest.

Figure 24. LC lumped balun and matching network

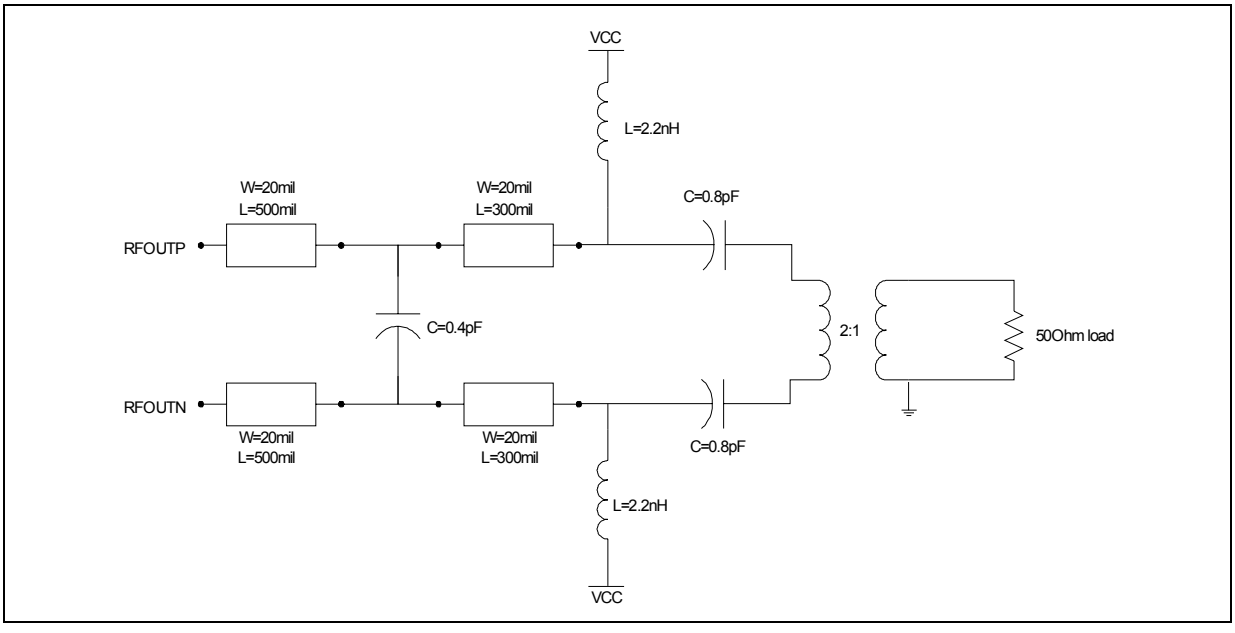


The 6.8nH shunt inductor works as a DC feed for one of the open collector terminals as well as a matching element along with the other components. The 1.1nH series inductors are used to resonate the parasitic capacitance of the chip.

For an optimum output matching it is recommended to use 0402 Murata or AVX capacitors and 0403 or 0604 HQ Coilcraft inductors. It is also advisable to use short interconnection paths to minimize losses and undesired impedance shift.

An alternative topology, which allows for a more broadband matching and balanced to unbalanced conversion, is shown in *Figure 25*.

Figure 25. Microstrip line and lumped matching network



By using this topology the STW81100 is capable to deliver approximately 0dBm to a 50Ω load with a return loss grater than 10dB over the whole frequency band (3.3 to 4.4GHz).

Those results have been achieved on an FR4 substrate with a thickness of 350um.

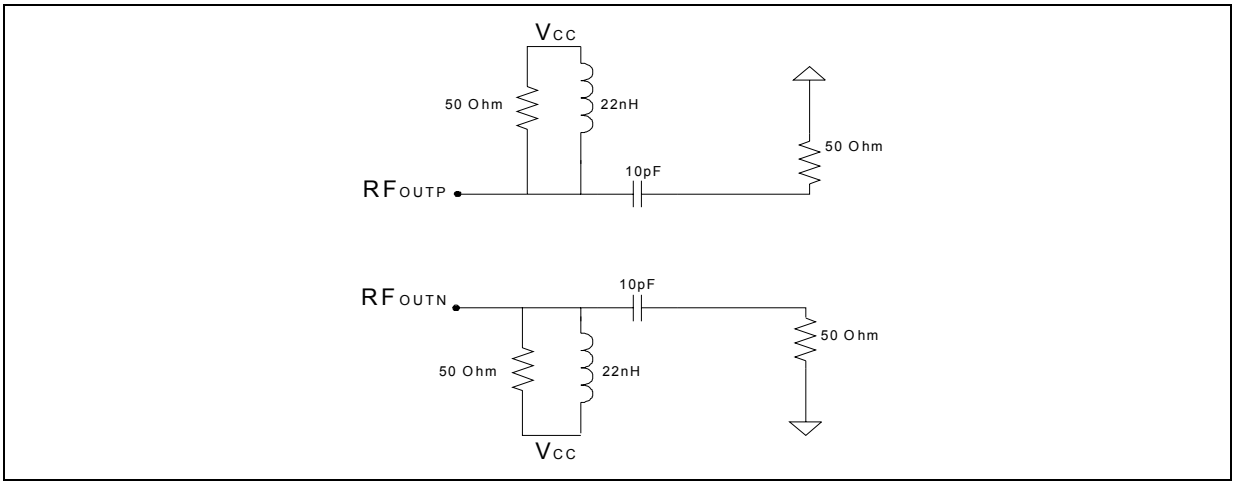
For the differential to single ended conversion the 50 to 100Ω - 3.3 to 4.4GHz - Johanson balun is recommended (3700BL15B100).

9.2 Divided by 2 output

If the user's application does not require a balanced to unbalanced conversion, the output matching reduces to the simple circuit shown below (*Figure 26*).

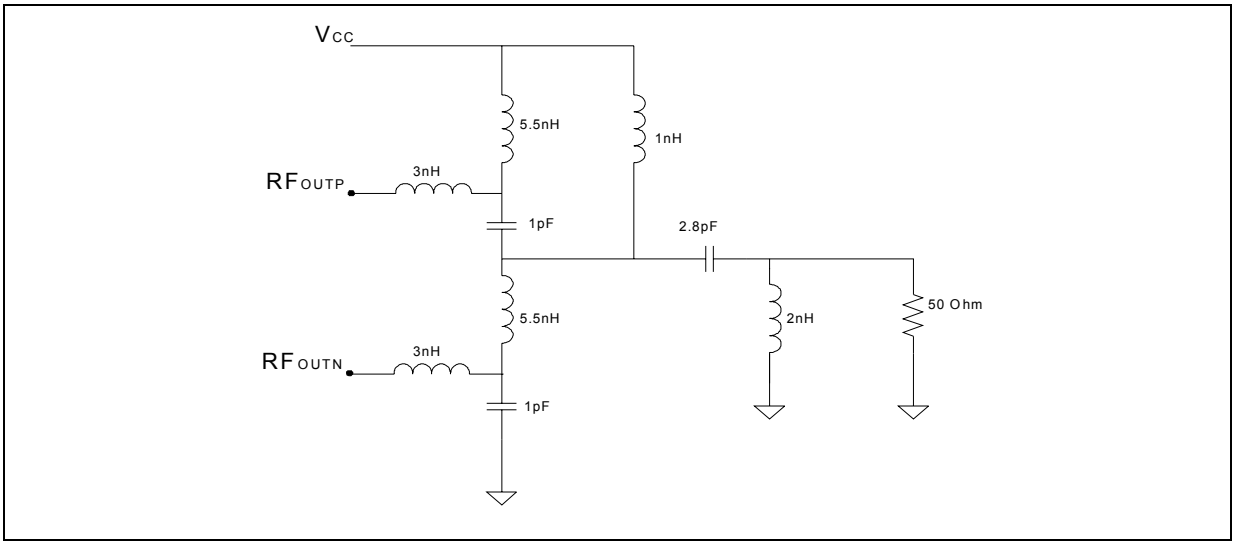
This solution can be easily used to provide one single ended output just terminating the other output at 50Ω with a 3dB power loss.

Figure 26. Differential/single ended output network in the 1.65 - 2.2GHz range



A first solution to combine the differential outputs is the lumped LC type balun tuned in the 2GHz band (*Figure 27*). An output power of approximately 2 dBm is delivered to a 50Ω load over the whole band (1.65GHz to 2.2GHz).

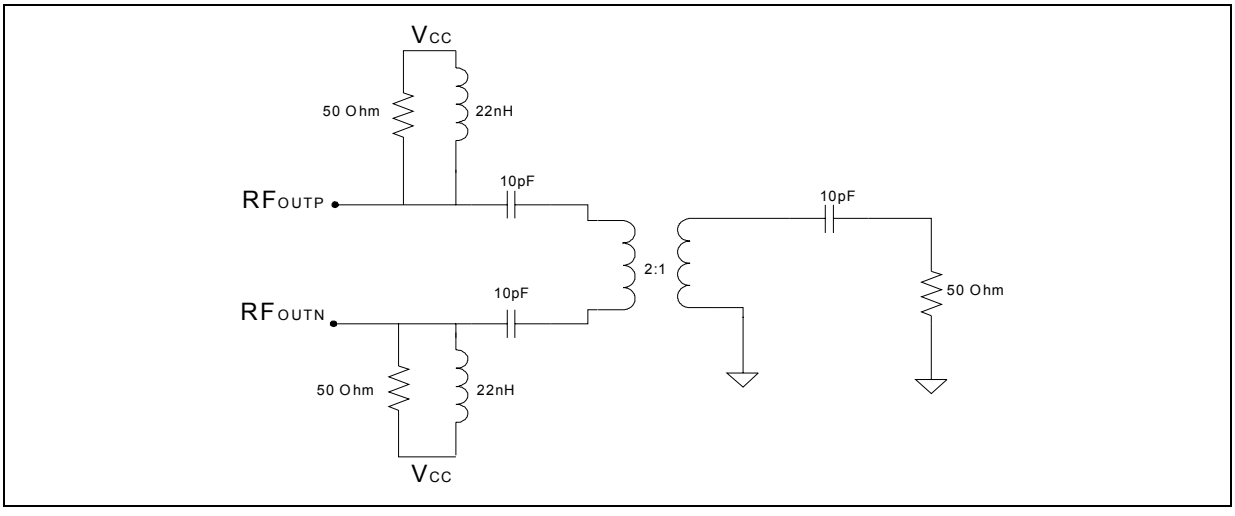
Figure 27. LC lumped balun for the divided by 2 output



The same recommendation for the SMD components applies also for the divided by 2 output.

Another topology suitable to combine the two outputs for the divided by 2 frequencies is represented in *Figure 28*.

Figure 28. Lumped output matching for the divided by 2 output



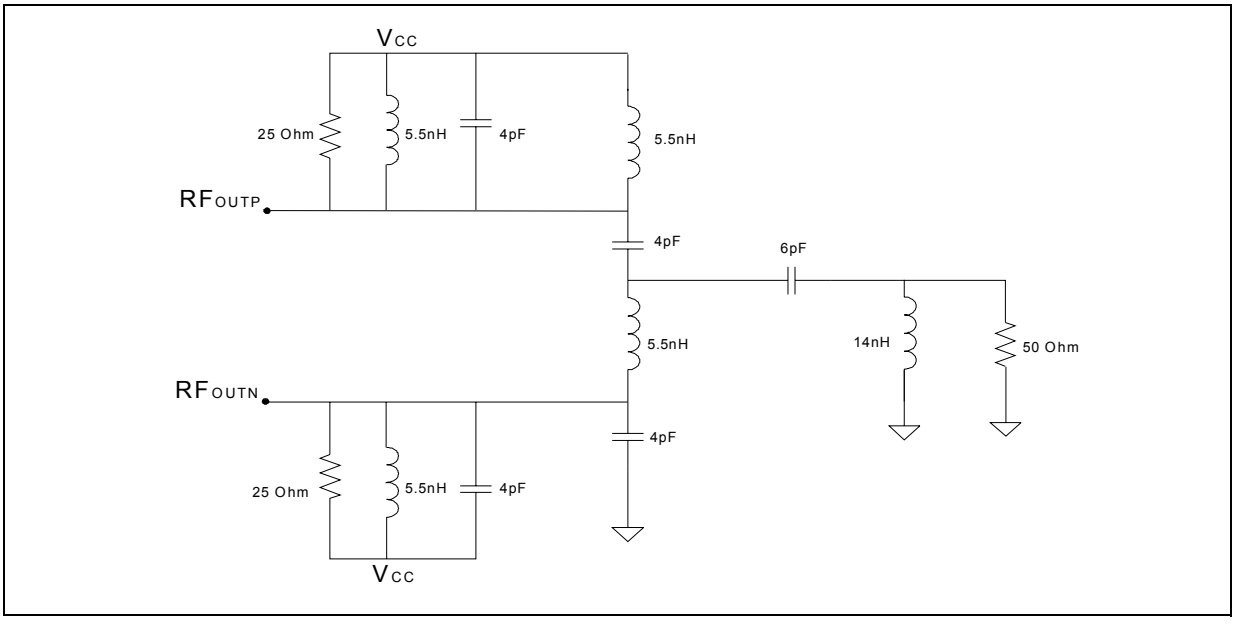
The balun used is the 50 to 100Ω - 1.65GHz to 2.2GHz Johanson balun (1850BL15B100).

9.3 Divided by 4 output

The same topology, components values and considerations of *Figure 26*, apply also for the divided by 4 output.

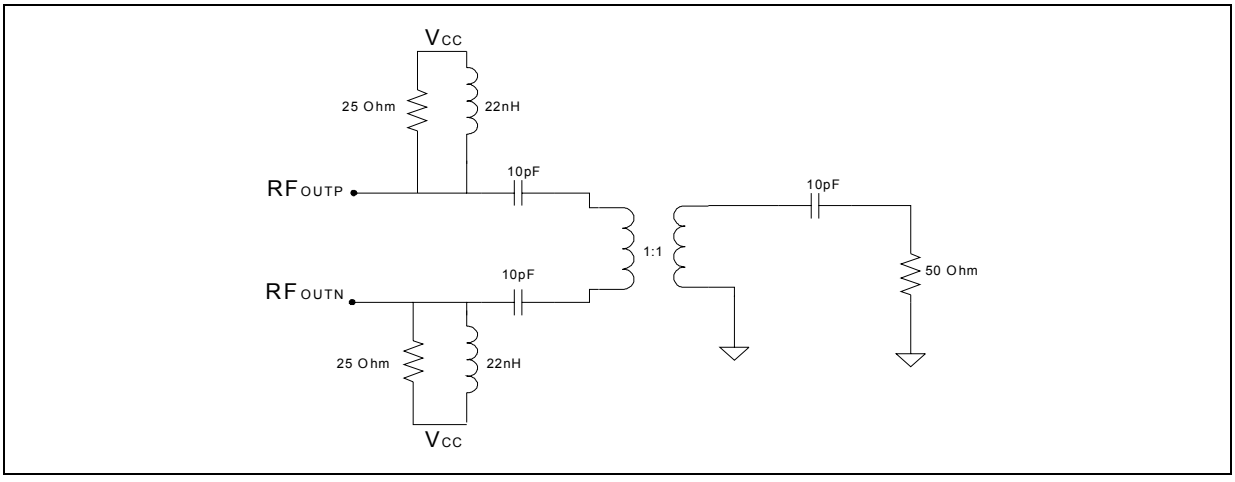
As for the previous sections, a solution to combine the differential outputs is the lumped LC type balun tuned in the 1GHz band (*Figure 29*). An output power of approximately 5 dBm is delivered to a 50Ω load over the whole band (825GHz to 1.1GHz).

Figure 29. LC lumped balun for the divided by 4 output



If the user prefers to use an RF balun it is possible to adopt the same topology depicted in *Figure 28*, just changing the balun and the resistor value (*Figure 30*). The suggested balun for the 0.8 - 1.1GHz frequency range is the 1:1 Johanson 900BL15B050.

Figure 30. Lumped output matching for the divided by 4 output



9.4 Evaluation Kit

It is available upon request an Evaluation Kit including:

- Evaluation Board
- GUI (Graphical User Interface) to program the device
- Measured S parameters of the RF output
- ADS2005 schematics providing guidelines for application board design
- STWPLLSim software for PLL loop filter design and noise simulation