Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

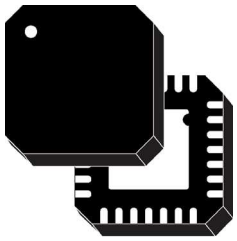
Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

STW81103

Multi-band RF frequency synthesizer with integrated VCOs

Features

- Integer-N frequency synthesizer
- Dual differential integrated VCOs with automatic center frequency calibration:
  - 2500 - 3050 MHz (direct output)
  - 4350 - 5000 MHz (direct output)
  - 1250 - 1525 MHz (internal divider by 2)
  - 2175 - 2500 MHz (internal divider by 2)
  - 625 - 762.5 MHz (internal divider by 4)
  - 1087.5 - 1250 MHz (internal divider by 4)
- Excellent integrated phase noise
- Fast lock time: 150µs
- Dual modulus programmable prescaler (16/17 or 19/20)
- 2 programmable counters to achieve a feedback division ratio from 256 to 65551 (prescaler 16/17) and from 361 to 77836 (prescaler 19/20).
- Programmable reference frequency divider (10 bits)
- Phase frequency comparator and charge pump
- Programmable charge pump current
- Digital lock detector
- Dual digital bus interface: SPI and I^2C bus (fast mode) with 3 bit programmable address ($1100A_2A_1A_0$)
- 3.3 V power supply
- Power down mode (hardware and software)
- Small size exposed pad VFQFPN28 package 5 mm x 5 mm x 1.0 mm
- Process: BICMOS 0.35 µm SiGe



VFQFPN28

Applications

- 2.5G and 3G Cellular infrastructure equipment
- CATV equipment
- Instrumentation and test equipment
- Other wireless communication systems

Description

The STMicroelectronics STW81103 is an integrated RF synthesizer with voltage controlled oscillators (VCOs). Showing high performance, high integration, low power, and multi-band performances, STW81103 is a low cost one chip alternative to discrete PLL and VCOs solutions.

STW81103 includes an Integer-N frequency synthesizer and two fully integrated VCOs featuring low phase noise performance and a noise floor of -155dBc/Hz. The combination of wide frequency range VCOs (thanks to center-frequency calibration over 32 sub-bands) and multiple output options (direct output, divided by 2 or divided by 4) allows to cover the 625 MHz-762.5 MHz, the 1087.5 MHz-1525 MHz, the 2175 MHz-3050 MHz and the 4350 MHz-5000 MHz bands.

The STW81103 is designed with STMicroelectronics advanced 0.35 µm SiGe process.

Contents

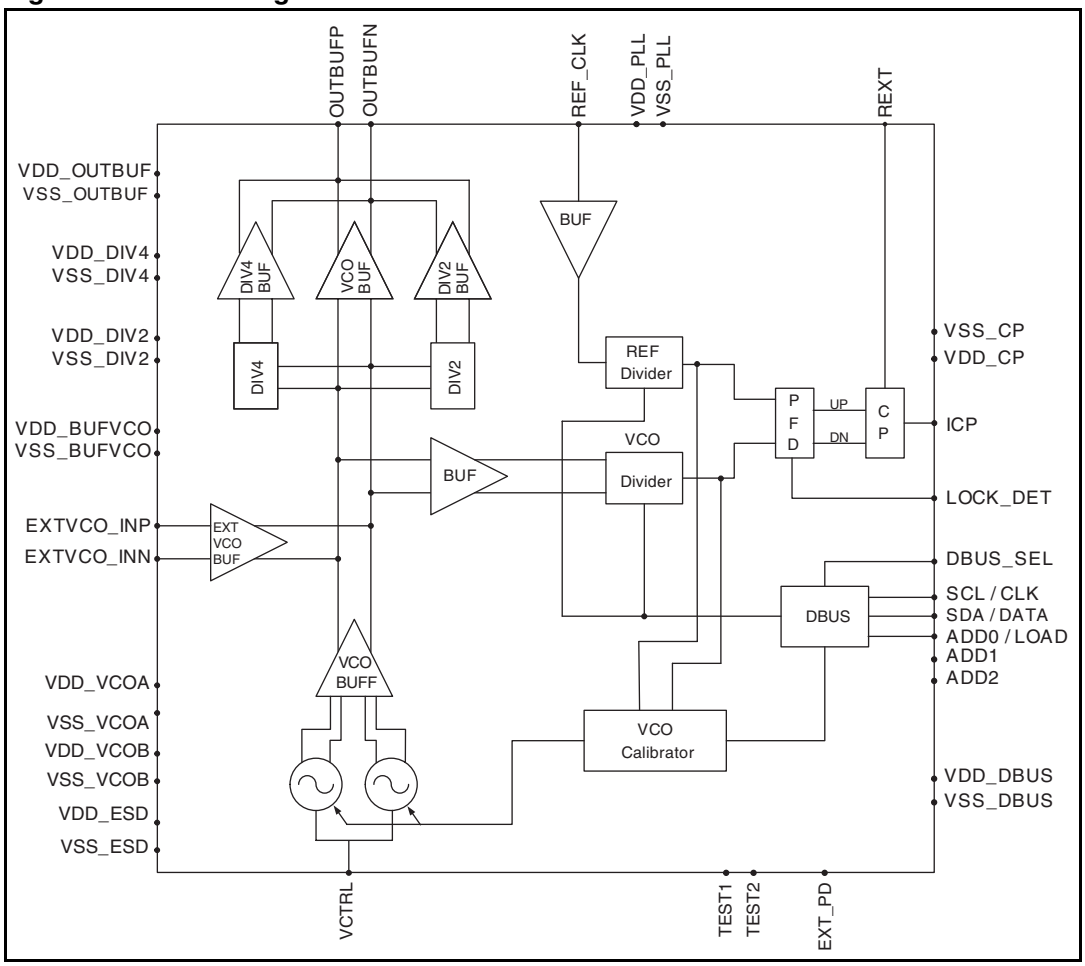
List of tables

List of figures

1 Block diagram and pin configuration

1.1 Block diagram

Figure 1. Block diagram



1.2 Pin configuration

Figure 2. Pin connection (top view)

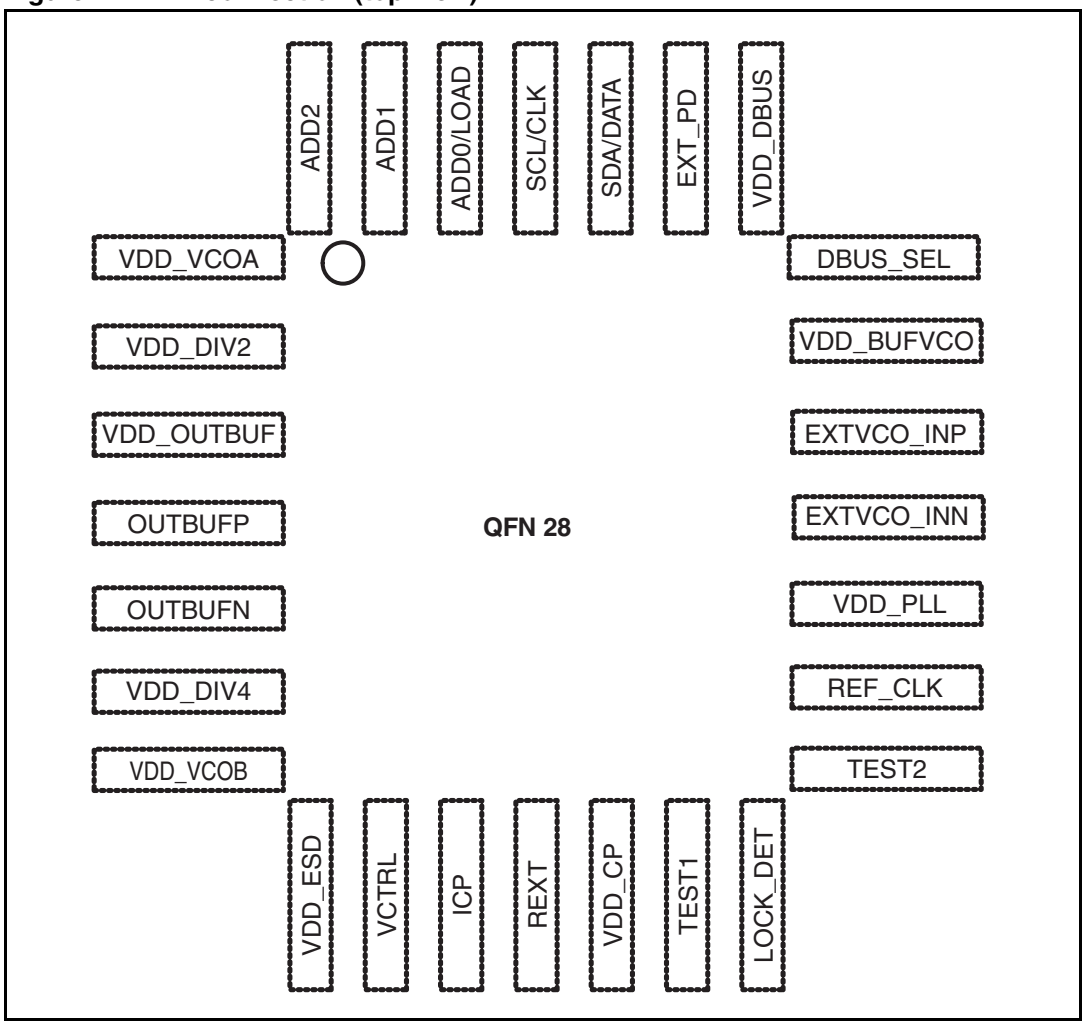


Table 1. Pin description

Pin No	Name	Description	Observation
1	VDD_VCOA	VCO A power supply	
2	VDD_DIV2	Divider by 2 power supply	
3	VDD_OUTBUF	Output buffer power supply	
4	OUTBUFP	LO buffer positive output	Open collector
5	OUTBUFN	LO buffer negative output	Open collector
6	VDD_DIV4	Divider by 4 power supply	
7	VDD_VCOB	VCO B power supply	
8	VDD_ESD	ESD positive rail power supply	
9	VCTRL	VCO control voltage	

Table 1. Pin description (continued)

Pin No	Name	Description	Observation
10	ICP	PLL charge pump output	
11	REXT	External resistance connection for PLL charge pump	
12	VDD_CP	Power supply for charge pump	
13	TEST1	Test input 1	For test purposes only; must be connected to GND
14	LOCK_DET	Lock detector	CMOS output (I_{OUT}=4mA)
15	TEST2	Test input 2	For test purposes only; must be connected to GND
16	REF_CLK	Reference clock input	
17	VDD_PLL	PLL digital power supply	
18	EXTVCO_INN	External VCO negative input	For test purposes only; must be connected to GND
19	EXTVCO_INP	External VCO positive input	For test purposes only; must be connected to GND
20	VDD_BUFVCO	VCO buffer power supply	
21	DBUS_SEL	Digital Bus Interface select	CMOS input
22	VDD_DBUS	SPI and I^2C bus power supply	
23	EXT_PD	Power down hardware ‘0’ device ON; ‘1’ device OFF	CMOS input
24	SDA/DATA	I2CBUS/SPI data line	CMOS Bidir Schmitt triggered (I_{OUT}=4mA)
25	SCL/CLK	I2CBUS/SPI clock line	CMOS input Schmitt triggered
26	ADD0/LOAD	I2CBUS address select pin/ SPI load line	CMOS input
27	ADD1	I2CBUS address select pin	CMOS input; must be connected to GND in SPI mode
28	ADD2	I2CBUS address select pin	CMOS input; must be connected to GND in SPI mode

2 Electrical specifications

2.1 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Values	Unit
AV_{CC}	Analog supply voltage	0 to 4.6	V
DV_{CC}	Digital supply voltage	0 to 4.6	V
T_{stg}	Storage temperature	+150	°C
ESD	Electrical static discharge - HBM(1) - CDM-JEDEC standard - MM	 4 1.5 0.2	kV

1. The maximum rating of the ESD protection circuitry on pin 4 and pin 5 is 800 V.

2.2 Operating conditions

Table 3. Operating conditions (1)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Units
AV_{CC}	Analog supply voltage		3.0	3.3	3.6	V
DV_{CC}	Digital supply voltage		3.0	3.3	3.6	V
I_{VDD1}	V_{DD1} current consumption			90		mA
I_{VDD2}	V_{DD2} current consumption			12		mA
T_{amb}	Operating ambient temperature		-40		85	°C
T_j	Maximum junction temperature				125	°C
$R_{th\ j\text{-}a}$	Junction to ambient package thermal resistance	Multilayer JEDEC board		44		°C/W
$R_{th\ j\text{-}b}$	Junction to board package thermal resistance	Multilayer JEDEC board		26.3		°C/W
$R_{th\ j\text{-}c}$	Junction to case package thermal resistance	Multilayer JEDEC board		6.3		°C/W

1. Refer to *Figure 36: Typical application diagram*.

2.3 Digital logic levels

Table 4. Digital logic levels

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Units
V_{il}	Low-level input voltage				0.2*Vdd	V
V_{ih}	High-level input voltage		0.8*Vdd			V
V_{hyst}	Schmitt trigger hysteresis		0.8			V
V_{ol}	Low-level output voltage				0.4	V
V_{oh}	High-level output voltage		0.85*Vdd			V

2.4 Electrical specifications

All electrical specifications are intended for a 3.3 V supply voltage.

Table 5. Electrical specifications

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Output frequency range						
F_{OUTA}	Output frequency range with VCOA	Direct output	2500		3050	MHz
		Divider by 2	1250		1525	MHz
		Divider by 4	625		762.5	MHz
F_{OUTB}	Output frequency range with VCOB	Direct output	4350		5000	MHz
		Divider by 2	2175		2500	MHz
		Divider by 4	1087.5		1250	MHz
VCO dividers						
N	VCO divider ratio	Prescaler 16/17	256		65551	
		Prescaler 19/20	361		77836	
Reference clock and phase frequency detector						
F_{ref}	Reference input frequency		10		200	MHz
	Reference input sensitivity(1)		0.35	1	1.5	Vpeak
R	Reference divider ratio		2		1023	
F_{PFD}	PFD input frequency				16	MHz
F_{STEP}	Frequency step(2)	Prescaler 16/17	F_{OUT}/ 65551		F_{OUT}/ 256	Hz
		Prescaler 19/20	F_{OUT}/ 77836		F_{OUT}/ 361	Hz

Table 5. Electrical specifications (continued)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Charge pump						
I_{CP}	ICP sink/source(3)	3-bit programmable			5	mA
V_{OCP}	Output voltage compliance range		0.4		V_{dd}-0.3	V
	Spurious(4)	Direct output (F_{PFD}=200 kHz)		-76		dBc
		Divider by 2 (F_{PFD}=400 kHz)		-82		dBc
		Divider by 4 (F_{PFD}=800 kHz)		-88		dBc
VCOs						
K_{VCOA}	VCOA sensitivity(5)	Lower frequency range	45	65	85	MHz/V
		Intermediate frequency range	60	80	105	MHz/V
		Higher frequency range	85	105	145	MHz/V
K_{VCOB}	VCOB sensitivity(5)	Lower frequency range	45	65	85	MHz/V
		Intermediate frequency range	60	80	100	MHz/V
		Higher frequency range	85	100	130	MHz/V
ΔT_{LK}	Maximum temperature variation for continuous lock(5) (6)	VCO A	125			°C
		VCO B	95			°C
	VCOA pushing(5)			4	7	MHz/V
	VCOB pushing(5)			15	21	MHz/V
V_{CTRL}	VCO control voltage(5)		0.4		3	V
	LO harmonic spurious(5)				-20	dBc
I_{VCOA}	VCOA current consumption	F_{VCO}=2.8 GHz; amplitude[11]		30		mA
		F_{VCO}=2.8 GHz; amplitude[00]		16		mA
I_{VCOB}	VCOB current consumption	F_{VCO}=4.7 GHz; amplitude[11]		24		mA
		F_{VCO}=4.7 GHz; amplitude[00]		13		mA
I_{VCOBUF}	VCO buffer consumption			15		mA
I_{DIV2}	Divider by 2 consumption			17		mA
I_{DIV4}	Divider by 4 consumption			14		mA
LO output buffer						
P_{LO}	Output level			0		dBm
R_L	Return loss	Matched to 50 ohms		15		dB
I_{OUTBUF}	Current consumption	DIV4 Buff		26		mA
		DIV2 Buff		23		mA
		Direct output		39		mA

Table 5. Electrical specifications (continued)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
External VCO						
	Frequency range		0.625		5.0	GHz
	Input level		-10		+6	dBm
	Current consumption	VCO internal buffer		28		mA
PLL miscellaneous						
I_{PLL}	Current consumption	Input buffer, prescaler, digital dividers, misc.		12		mA
t_{lock}	Lockup time(5) (7)	25 kHz PLL bandwidth; within 1 ppm of frequency error		150		µs

1. In order to achieve best phase noise performance 1 V peak level is suggested.
2. The frequency step is related to the PFD input frequency as follows:
   - $F_{step} = F_{PFD}$ for direct output
   - $F_{step} = F_{PFD}/2$ for divided by 2 output
   - $F_{step} = F_{PFD}/4$ for divided by 4 output
3. See relationship between ICP and REXT in *Section 5.7: Charge pump*.
4. The level of the spurs may change depending on PFD frequency, charge pump current, selected channel and PLL loop BW.
5. Guaranteed by design and specification.
6. When setting a specified output frequency, the VCO calibration procedure must be run in order to select the best sub-range for the VCO covering the desired frequency. Once programmed at the initial temperature T_0 inside the operating temperature range (-40 °C to +85 °C), the synthesizer is able to maintain the lock status only if the temperature drift (in either direction) is within the limit specified by ΔT_{LK}, provided that the final temperature T_1 is still inside the nominal range. If higher ΔT are required the **"VCO calibration auto-restart"** feature can be enabled, thus allowing to re-start the VCO calibration procedure automatically when the part loose the lock condition (trigger on lock detector signal).
7. Frequency jump from 2250 to 2400 MHz; it includes the time required by the VCO calibration procedure (7 F_{PFD} cycles with F_{PFD}=400 kHz).

2.5 Phase noise specification

Table 6. Phase noise specification (1)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
In-band phase noise floor – closed loop(2)					
Normalized inband phase noise floor	ICP=4 mA, PLL BW=50 kHz; including reference clock contribution		-222		dBc/Hz
Inband phase noise floor direct output			-222+20log(N)+10log(F_{PFD})		dBc/Hz
Inband phase noise floor divider by 2			-228+20log(N)+10log(F_{PFD})		dBc/Hz
Inband phase noise floor divider by 4			-234+20log(N)+10log(F_{PFD})		dBc/Hz
PLL integrated phase noise – direct output					
Integrated phase noise 100 Hz to 40 MHz	F_{OUT}=4.675 GHz, F_{PFD}=200 kHz, F_{STEP}=200 kHz, PLL BW = 15 kHz, ICP=3 mA		-34.6		dBc
			1.5		° rms
PLL integrated phase noise – divider by 2					
Integrated phase noise 100 Hz to 40 MHz	F_{OUT}=2.3376 GHz, F_{PFD}=400 kHz, F_{STEP}=200 kHz, PLL BW=25 kHz, ICP=2 mA		-42.6		dBc
			0.6		° rms
PLL integrated phase noise – divider by 4					
Integrated phase noise 100 Hz to 40 MHz	F_{OUT}=1.1688 GHz, F_{PFD}=800 kHz, F_{STEP}=200 kHz, PLL BW=35 kHz, ICP=1.5 mA		-49.5		dBc
			0.27		° rms
VCO A direct (2500 MHz-3050 MHz) – open loop(3)					
Phase noise @ 1 kHz			-59		dBc/Hz
Phase noise @ 10 kHz			-87		dBc/Hz
Phase noise @ 100 kHz			-109		dBc/Hz
Phase noise @ 1 MHz			-131		dBc/Hz
Phase noise @ 10 MHz			-151		dBc/Hz
Phase noise @ 40 MHz			-161		dBc/Hz
VCO B direct (4350 MHz-5000 MHz) – open loop(3)					
Phase noise @ 1 kHz			-54		dBc/Hz
Phase noise @ 10 kHz			-82		dBc/Hz
Phase noise @ 100 kHz			-105		dBc/Hz
Phase noise @ 1 MHz			-127		dBc/Hz
Phase noise @ 10 MHz			-147		dBc/Hz
Phase noise @ 40 MHz			-157		dBc/Hz

Table 6. Phase noise specification (1) (continued)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
VCO A with divider by 2 (1250 MHz-1525 MHz) – open loop(3)					
Phase noise @ 1 kHz			-65		dBc/Hz
Phase noise @ 10 kHz			-93		dBc/Hz
Phase noise @ 100 kHz			-115		dBc/Hz
Phase noise @ 1 MHz			-137		dBc/Hz
Phase noise @ 10 MHz			-153		dBc/Hz
Phase noise floor @ 40 MHz			-155		dBc/Hz
VCO B with divider by 2 (2175 MHz-2500 MHz) – open loop(3)					
Phase noise @ 1 kHz			-60		dBc/Hz
Phase noise @ 10 kHz			-88		dBc/Hz
Phase noise @ 100 kHz			-111		dBc/Hz
Phase noise @ 1 MHz			-132		dBc/Hz
Phase noise @ 10 MHz			-150		dBc/Hz
Phase noise floor @ 40 MHz			-154		dBc/Hz
VCO A with divider by 4 (625 MHz-762.5 MHz) – open loop(3)					
Phase noise @ 1 kHz			-71		dBc/Hz
Phase noise @ 10 kHz			-99		dBc/Hz
Phase noise @ 100 kHz			-121		dBc/Hz
Phase noise @ 1 MHz			-142		dBc/Hz
Phase noise @ 10 MHz			-154		dBc/Hz
Phase noise floor @ 40 MHz			-155		dBc/Hz
VCO B with divider by 4 (1087.5 MHz-1250 MHz) – open loop(3)					
Phase noise @ 1 kHz			-66		dBc/Hz
Phase noise @ 10 kHz			-94		dBc/Hz
Phase noise @ 100 kHz			-117		dBc/Hz
Phase noise @ 1 MHz			-138		dBc/Hz
Phase noise @ 10 MHz			-153		dBc/Hz
Phase noise floor @ 40 MHz			-154		dBc/Hz

1. Phase Noise SSB. VCO amplitude setting to value [11]. All closed-loop performances are specified using a reference clock signal at 76.8 MHz with a phase noise of -135 dBc/Hz @1 kHz offset, -145dBc/Hz @10kHz offset and -149.5 dBc/Hz of noise floor.
2. Normalized PN = Measured PN – 20log(N) – 10log(F_{PFD}), where N is the VCO divider ratio (N=B*P+A) and F_{PFD} is the comparison frequency at the PFD input.
3. Typical phase noise at centre band frequency.

An evaluation kit is available upon request, including a powerful simulation tool (STWPLLSim) that allows a very accurate estimation of the device's phase noise according to the desired project parameters (VCO frequency, selected output stage, reference clock, frequency step, and so on); refer to *Section 8: Application information* for more details.

3 Typical performance characteristics

Phase noise is measured with the Agilent E5052A Signal Source Analyzer. All closed-loop measurements are done with F_{STEP}=200 kHz, with the F_{PFD} and charge pump current properly set. The loop filter configuration is depicted in *Figure 36: Typical application diagram*, and the reference clock signal is at 76.8 MHz with a phase noise of -135 dBc/Hz @1 kHz offset, -145 dBc/Hz @10 kHz offset and -149.5 dBc/Hz of noise floor.

Figure 3. VCO A (direct output) open loop phase noise

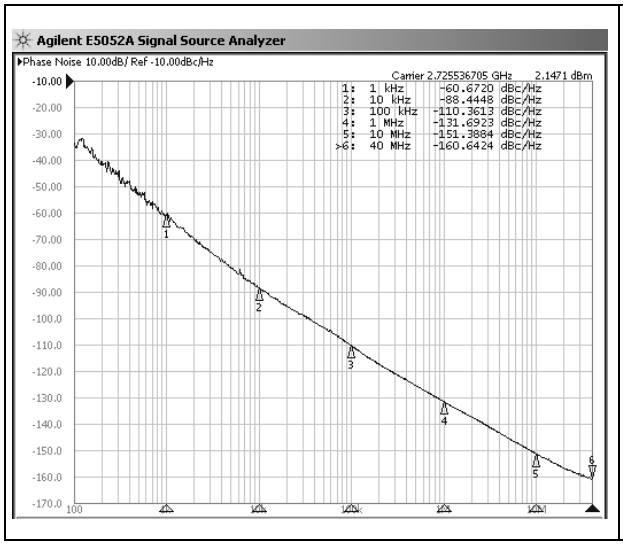


Figure 4. VCO B (direct output) open loop phase noise

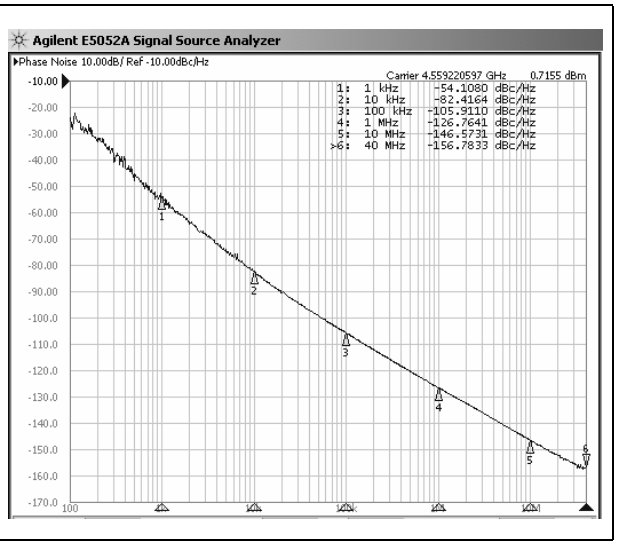


Figure 5. VCO A (direct output) closed loop phase noise at 2.775 GHz (F_{STEP}=200 kHz; F_{PFD}=200 kHz; I_{CP}=2 mA)

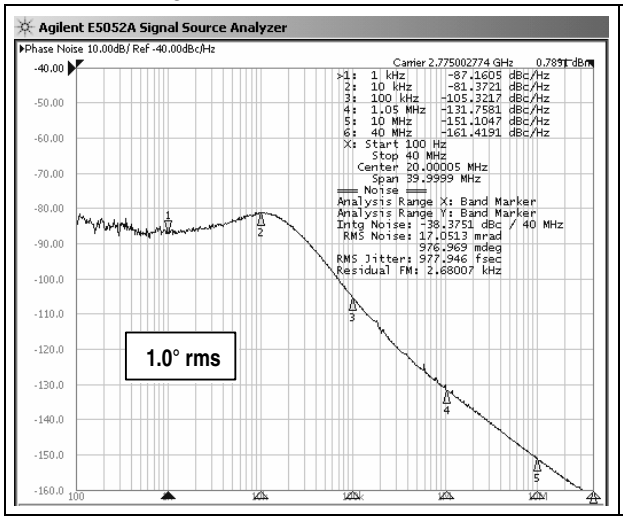


Figure 6. VCO B (direct output) closed loop phase noise at 4.675 GHz (F_{STEP}=200 kHz; F_{PFD}=200 kHz; I_{CP}=3 mA)

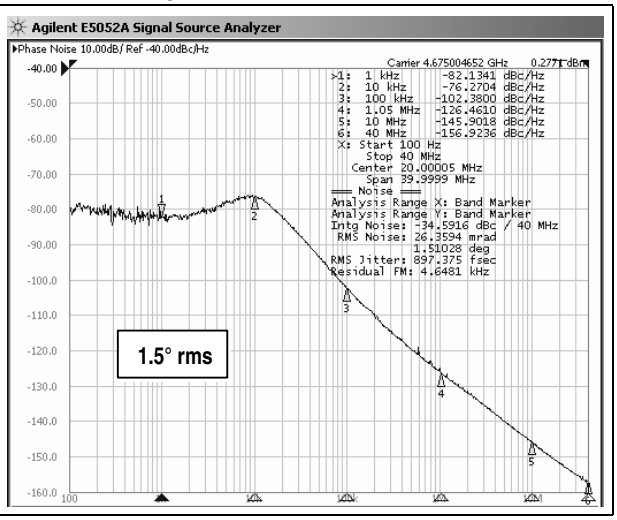


Figure 7. VCO A (div. by 2 output) closed loop phase noise at 1.3876 GHz (F_{STEP}=200 kHz; F_{PFD}=400 kHz; I_{CP}=1.5 mA)

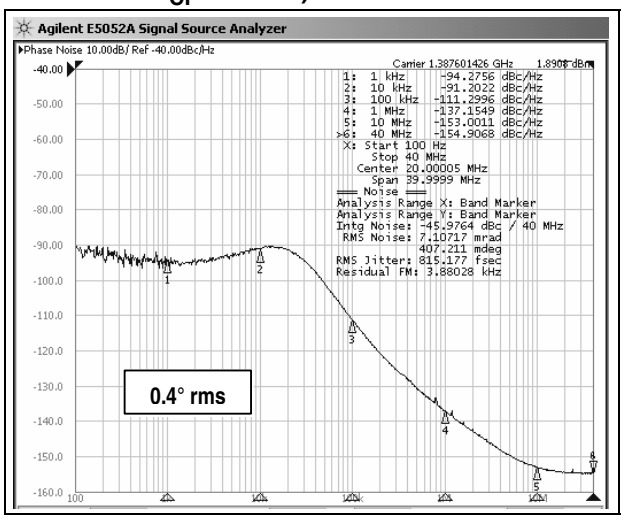


Figure 8. VCO B (div. by 2 output) closed loop phase noise at 2.3376 GHz (F_{STEP}=200 kHz; F_{PFD}=400 kHz; I_{CP}=2 mA)

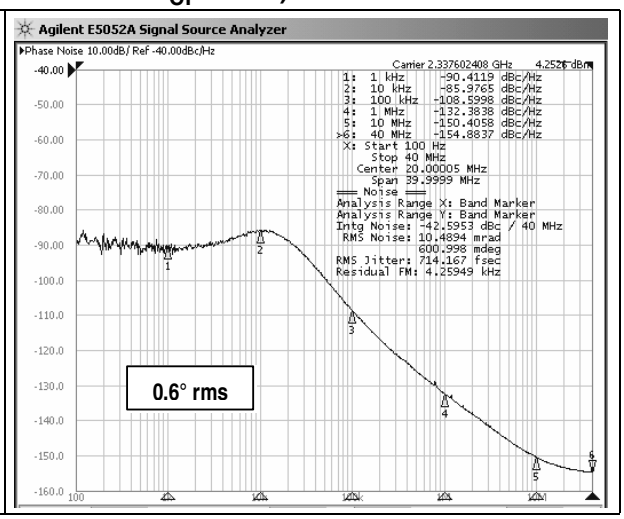


Figure 9. VCO A (div. by 4 output) closed loop phase noise at 693.8 MHz (F_{STEP}=200 kHz; F_{PFD}=800 kHz; I_{CP}=1 mA)

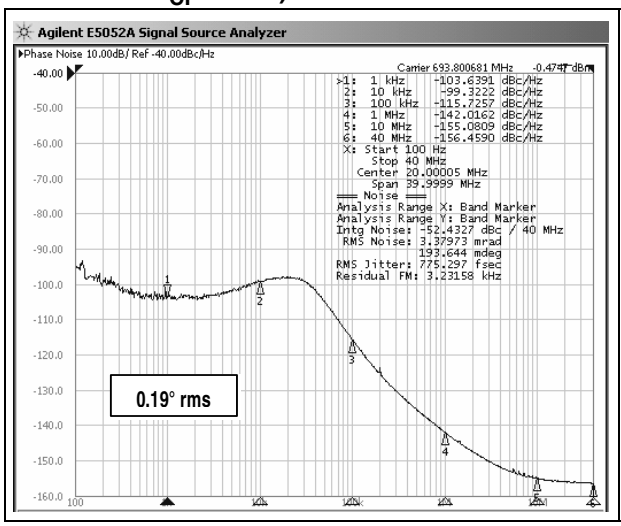


Figure 10. VCO B (div. by 4 output) closed loop phase noise at 1168.8 MHz (F_{STEP}=200 kHz; F_{PFD}=800 kHz; I_{CP}=1.5 mA)

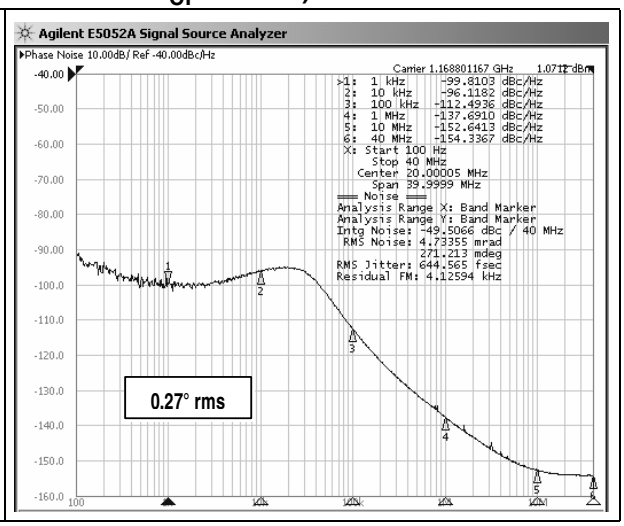


Figure 11. PFD frequency spurs (direct output; F_{PFD}=200 kHz)

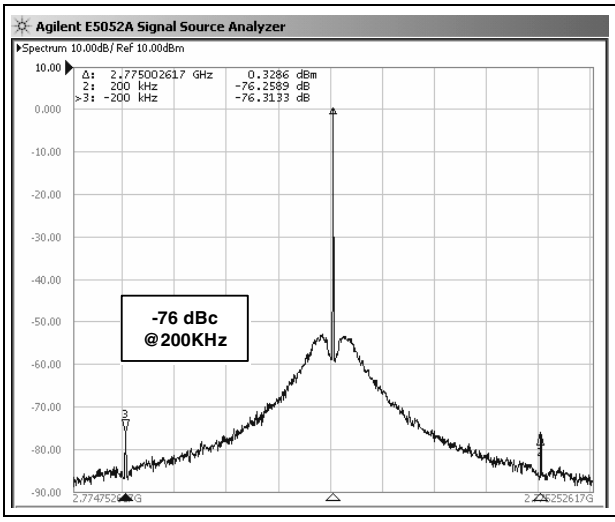


Figure 12. PFD frequency spurs (div. by 2 output; F_{PFD}=400 kHz)

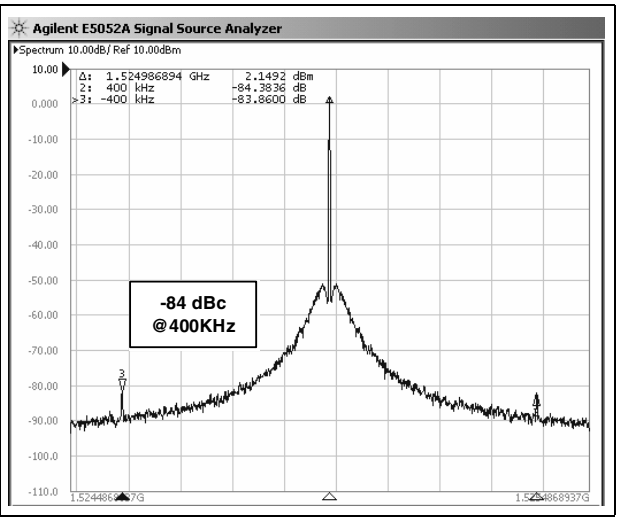


Figure 13. PFD frequency spurs (div. by 4 output; F_{PFD}=800 kHz)

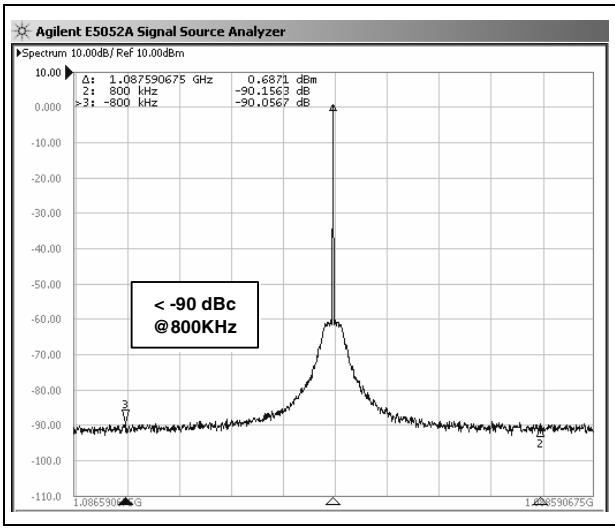
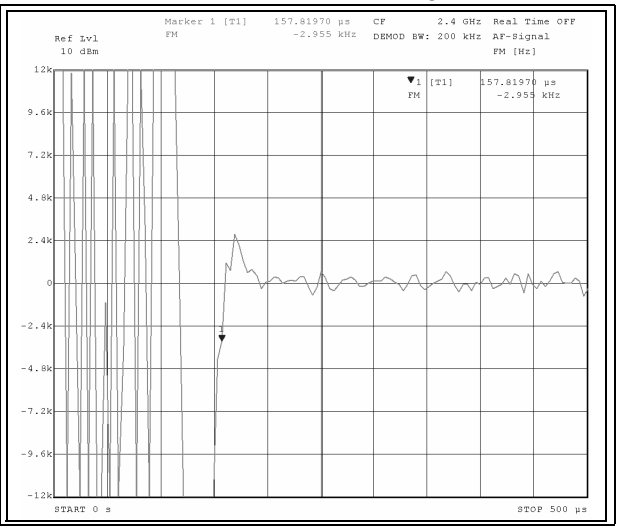


Figure 14. Settling time (final frequency=2.4 GHz; F_{PFD}=400 kHz; I_{CP}=2.5 mA)



4 General description

Figure 1: Block diagram shows the separate blocks that, when integrated, form an Integer-N PLL frequency synthesizer.

The STW81103 consists of two internal low-noise VCOs with buffer blocks, a divider by 2, a divider by 4, a low-noise PFD (phase frequency detector), a precise charge pump, a 10-bit programmable reference divider, two programmable counters and a programmable dual-modulus prescaler. The 5-bit A-counter and 12-bit B-counter, in conjunction with the dual-modulus prescaler P/P+1 (16/17 or 19/20), implement an N integer divider, where N = B*P +A. The division ratio of both reference and VCO dividers is controlled through the selected digital interface (I^2C bus or SPI).

The digital interface type is selected through the proper hardware connection of pin DBUS_SEL (0 V for I^2C bus, 3.3 V for SPI).

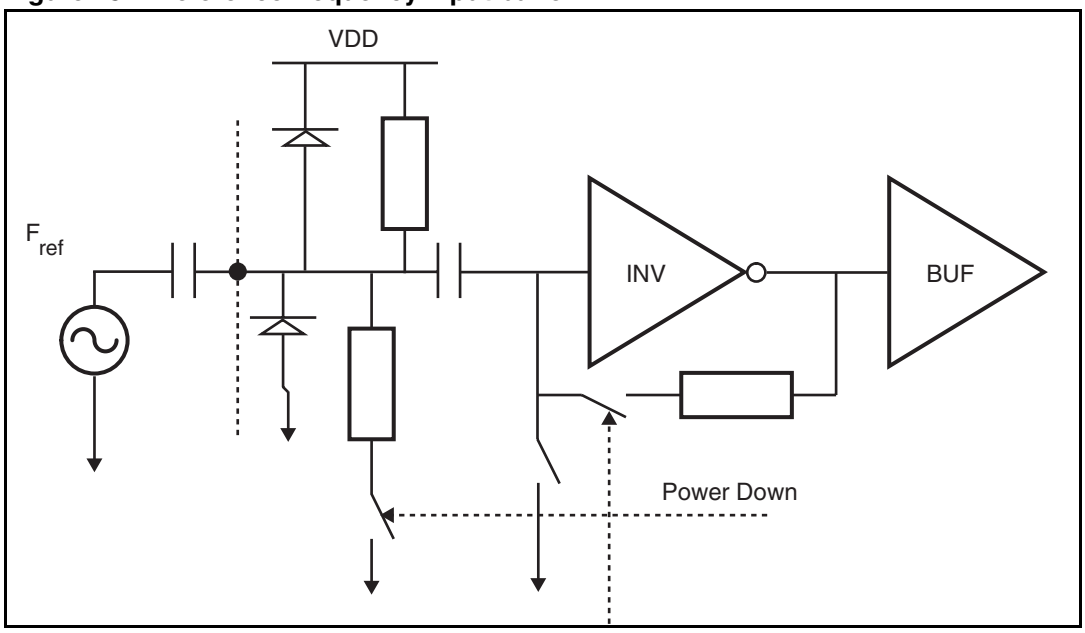
All devices operate with a power supply of 3.3 V, and can be powered down when not in use.

5 Circuit description

5.1 Reference input stage

The reference input stage is shown in *Figure 15*. The resistor network feeds a DC bias at the F_{ref} input, while the inverter used as the frequency reference buffer is AC coupled.

Figure 15. Reference frequency input buffer



5.2 Reference divider

The 10-bit programmable reference counter allows division of the input reference frequency to produce the input clock to the PFD. The division ratio is programmed through the digital interface.

5.3 Prescaler

The dual-modulus prescaler P/P+1 takes the CML clock from the VCO buffer and divides it down to a manageable frequency for the CMOS A and B counters. The modulus P is programmable and can be set to 16 or 19. The prescaler is based on a synchronous 4/5 core whose division ratio depends on the state of the modulus input.

5.4 A and B counters

The 5-bit A-counter and 12-bit B-counter, in conjunction with the selected dual modulus (16/17 or 19/20) prescaler, allow the generation of output frequencies that are spaced only by the reference frequency divided by the reference division ratio. The division ratio and the VCO output frequency are given by the following formulas:

$N = B \times P + A$

$$F_{VCO} = \frac{(B \times P + A)}{R} \times F_{ref}$$

where

F_{VCO}: output frequency of VCO

P: modulus of dual modulus prescaler (16 or 19 selected through the digital interface)

B: division ratio of the main counter

A: division ratio of the swallow counter

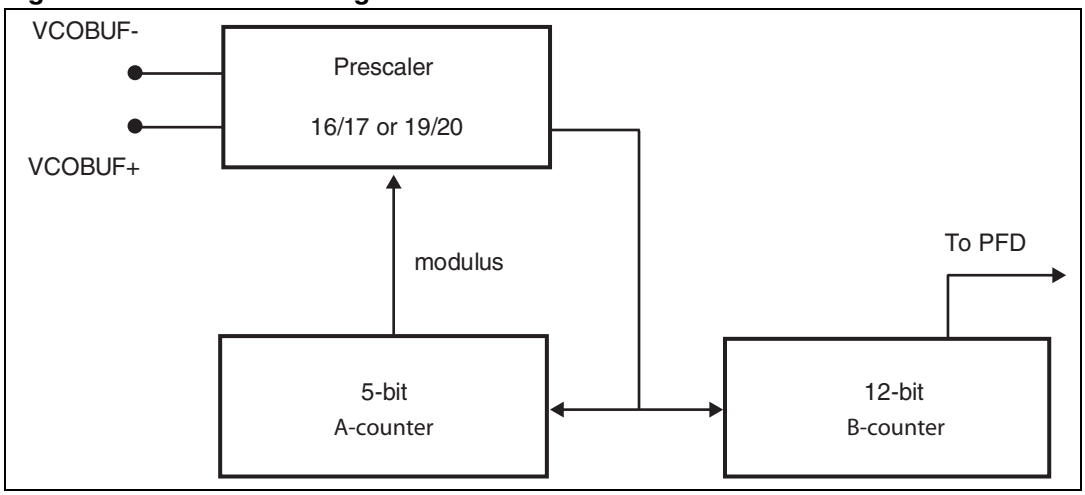
F_{ref}: input reference frequency

R: division ratio of the reference counter

N: division ratio of the PLL

For the VCO divider to work correctly, B absolutely must be greater than A, which can take any value ranging from 0 to 31. The value range of N is either from 256 to 65551 (if P=16) or from 361 to 77836 (P=19).

Figure 16. VCO divider diagram

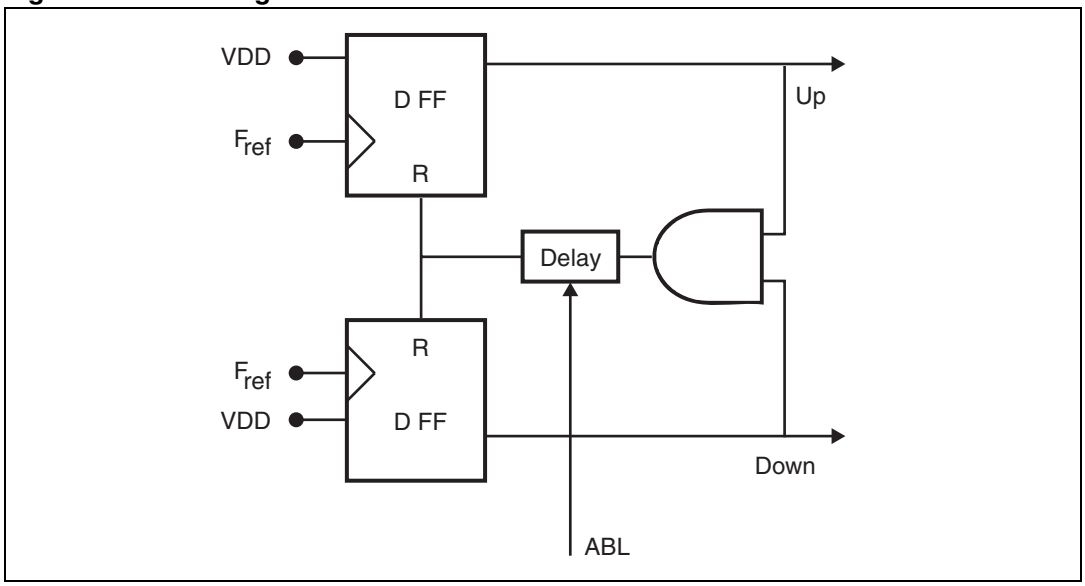


5.5 Phase frequency detector (PFD)

The PFD takes inputs from the reference and the VCO dividers and produces an output proportional to the phase error. The PFD includes a delay gate that controls the width of the anti-backlash pulse. This pulse ensures that there is no dead zone in the PFD transfer function.

Figure 17 is a simplified schematic of the PFD.

Figure 17. PFD diagram



5.6 Lock detect

This signal indicates that the difference between rising edges of both UP and DOWN PFD signals is found to be shorter than the fixed delay (roughly 5 ns). The Lock Detect signal is high when the PLL is locked and low when the PLL is unlocked. Lock Detect consumes current only during PLL transients.

5.7 Charge pump

This block drives two matched current sources, I_{UP} and I_{DOWN}, which are controlled respectively by UP and DOWN PFD outputs. The nominal value of the output current is controlled by an external resistor (connected to the REXT input pin) and a 3-bit word that allows selection among 8 different values.

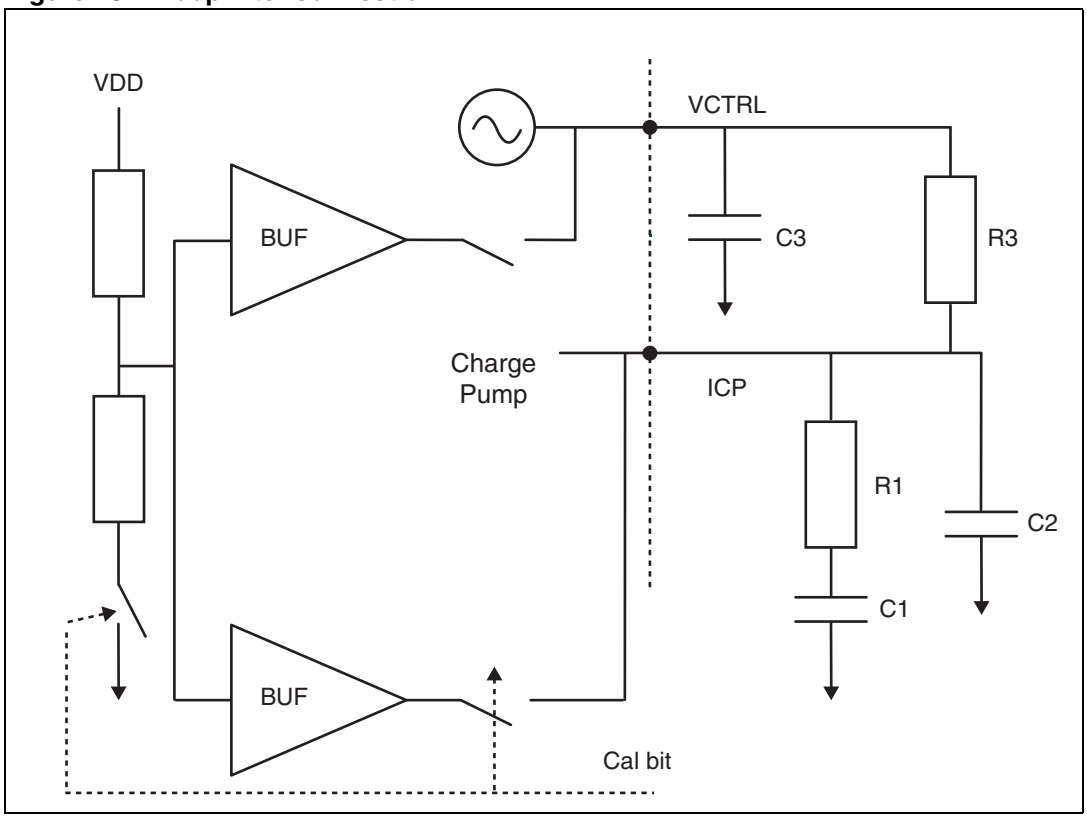
The minimum value of the output current is: I_{MIN} = 2*VBG/REXT (VBG~1.17 V)

Table 7. Current value vs. selection

CPSEL2	CPSEL1	CPSEL0	Current	Value for REXT=4.7 KΩ
0	0	0	I_{MIN}	0.5 mA
0	0	1	$2*I_{MIN}$	1.0 mA
0	1	0	$3*I_{MIN}$	1.5 mA
0	1	1	$4*I_{MIN}$	2.0 mA
1	0	0	$5*I_{MIN}$	2.5 mA
1	0	1	$6*I_{MIN}$	3.0 mA
1	1	0	$7*I_{MIN}$	3.5 mA
1	1	1	$8*I_{MIN}$	4.0 mA

Note: The current is output on pin ICP. During VCO auto-calibration, the ICP and VCTRL pins are forced to VDD/2.

Figure 18. Loop filter connection



5.8 Voltage controlled oscillators

5.8.1 VCO selection

The STW81103 integrates two low-noise VCOs to cover a wide band from:

- 2500 MHz to 3050 MHz and from 4350 MHz to 5000 MHz (direct output)
- 1250 MHz to 1525 MHz and from 2175 MHz to 2500 MHz (selecting divider by 2)
- 625 MHz to 762.5 MHz and from 1087.5 MHz to 1250 MHz (selecting divider by 4)

The frequency range is 2500 MHz-3050 MHz for VCO A, and 4350 MHz-5000 MHz for VCO B.

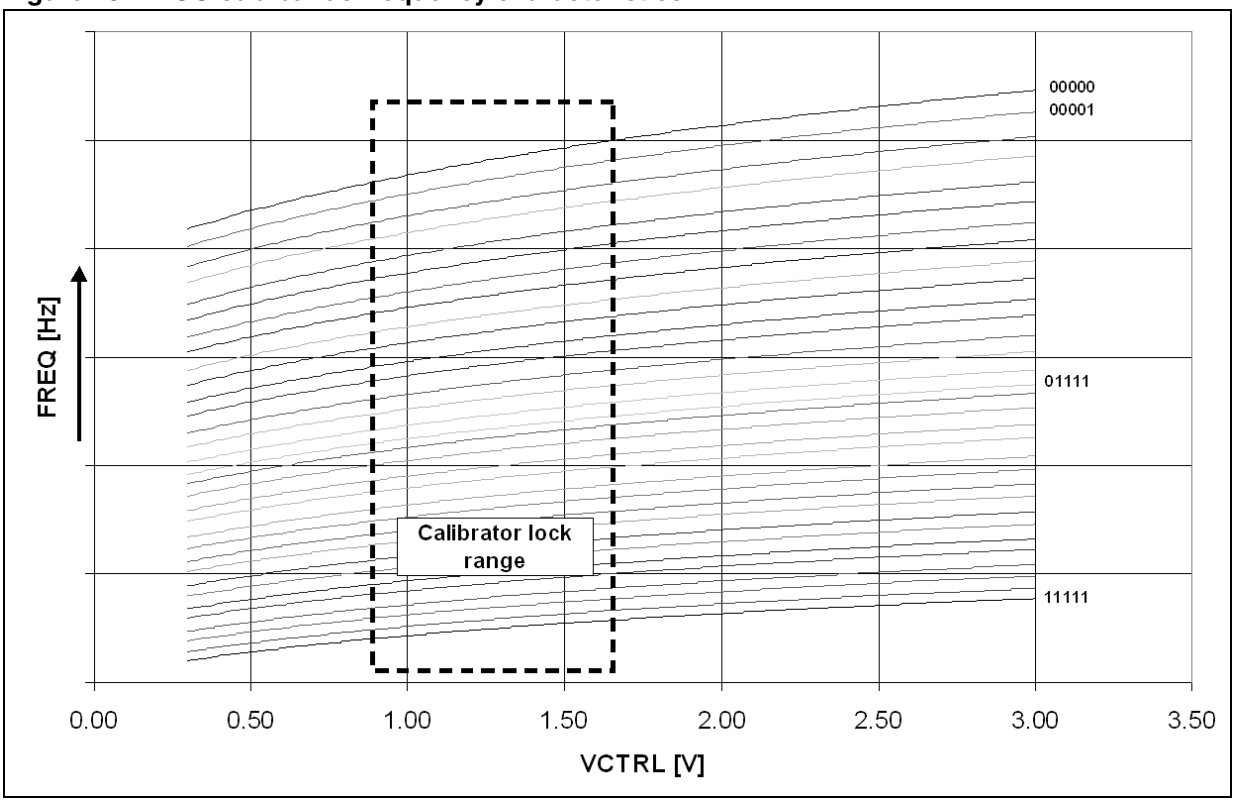
5.8.2 VCO frequency calibration

Both VCOs can operate on 32 frequency ranges that are selected by adding or subtracting capacitors from the resonator. These frequency ranges are intended to cover the wide band of operation and compensate for process variation on the VCO center frequency.

The range is automatically selected when the SERCAL bit is set to 1. The charge pump is inhibited, and the ICP and VCTRL pins are at VDD/2 volts. The ranges are then tested with this VCO input voltage to select the one nearest to the desired output frequency ($F_{OUT} = N*F_{ref}/R$).

After this selection, the SERCAL bit is automatically reset to 0 and the charge pump is once again enabled. To enable a fast settle, the PLL needs only to perform fine adjustments around VDD/2 on the loop filter to reach F_{OUT}.

Figure 19. VCO sub-bands frequency characteristics



The SERCAL bit should be set to “1” at each division ratio change. The VCO calibration procedure takes approximately 7 periods of the PFD frequency.

The maximum allowed F_{PFD} to perform the calibration process is 1 MHz. When using a higher F_{PFD}, follow the steps below:

1. Calibrate the VCO at the desired frequency with an F_{PFD} less than 1 MHz.
2. Set the ratio of the A, B and R dividers for the desired F_{PFD}.

VCO calibration auto-restart feature

The VCO calibration auto-restart feature, once activated, allows to restart the calibration procedure when the lock detector reports that the PLL has moved to an unlock condition (trigger on ‘1’ to ‘0’ transition of lock detector signal).

This situation could happen if the device experiences a significant temperature variation. Once programmed at the initial temperature T_0 inside the operating temperature range (-40 °C to +85 °C), the synthesizer is able to maintain the lock status only if the temperature drift (in either direction) is within the limit specified by the ΔT_{LK} parameter, provided that the final temperature T_1 is still inside the nominal range.

Each VCO featured by STW81103 has its specific ΔT_{LK} parameter reported in *Table 5*, that is typically lower than the maximum allowable drift (ΔT_{MAX}=125; from -40 °C to +85 °C and vice versa).

By enabling the VCO calibration auto-restart feature (through the CAL_AUTOSTART_EN bit), the part will be able to select again the proper VCO frequency sub-range if the temperature drift exceeds the ΔT_{LK} limit, without any external user command.

5.8.3 VCO voltage amplitude control

The voltage swing of the VCOs can be adjusted over four levels by means of two dedicated programming bits (PLL_A1 and PLL_A0). Higher amplitudes provide best phase noise, whereas lower amplitudes save power.

Table 8 gives the voltage swing level expected on the resonator nodes, the current consumption, and the phase noise at 1 MHz.

Table 8. VCO A performances versus amplitude setting (Freq = 2.8 GHz)

PLL_A[1:0]	Differential voltage swing (Vp)	Current consumption (mA)	PN @1 MHz (dBc/Hz)
00	1.1	16	-126
01	1.3	19	-127
10	1.9	27	-130
11	2.1	30	-131

Table 9. VCO B performances vs. amplitude setting (Freq = 4.7 GHz)

PLL_A[1:0]	Differential voltage swing (Vp)	Current consumption (mA)	PN at 1 MHz (dBc/Hz)
00	1.1	13	-121
01	1.3	15	-122
10	1.9	22	-126
11	2.1	24	-127

5.9 Output stage

The differential output signal of the synthesizer can be selected by software among three different signal paths (direct, divider by 2 and divider by 4) providing multi-band capability.

The selection of the output stage is done by programming properly the PD[4:0] bits.

The output stage is an open-collector structure which is able to meet different requirements over the desired output frequency range by proper connections on the PCB. Refer to *Section 8: Application information* for more details on PCB connections.

5.9.1 Output buffer control mode

This control mode allows to enable/disable the output stage by a hardware control pin (EXT_PD, pin#23) while the PLL stays locked at the desired frequency; in such a way a very fast switching time is achieved.

This feature can be useful in designing a ping-pong architecture saving the cost of an external RF switch.

The function of pin#23 (EXT_PD) is set with the OUTBUF_CTRL_EN bit as shown in *Table 10.*

Table 10. EXT_PD pin function setting

OUTBUF_CTRL_EN	Function of the EXT_PD pin	EXT_PD pin settings
0	Device hardware power down	EXT_PD = 0 V ➔ Device ON
		EXT_PD = 3.3 V ➔ Device OFF
1	Output Buffer control	EXT_PD = 0 V ➔ Output Stage ON
		EXT_PD = 3.3 V ➔ Output Stage OFF