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STW81200

Wideband RF PLL fractional/integer frequency synthesizer with integrated VCOs and LDOs

Datasheet - production data

VFQFPN36

Features

- Output frequency range: 46.875 to 6000 MHz
- Very Low Noise
  - Normalized in band phase noise floor: -227 dBc/Hz
  - VCO phase noise: -135 dBc/Hz @ 1 MHz offset, 4.0 GHz carrier
  - Noise floor: -160 dBc/Hz
- Dual architecture frequency synthesizer: Fractional-N and Integer-N
- Integrated VCOs with automatic center frequency calibration
- Programmable RF output dividers by 1/2/4/8/16/32/64
- Dual RF Output broadband matched with programmable power level and mute function
- External VCO option with 5 V charge pump
- Integrated low noise LDO voltage regulators
- Maximum phase detector frequency: 100 MHz
- Exact frequency mode
- Fast lock and cycle slip reduction
- Differential reference clock input (LVDS and LVECPL compliant) supporting up to 800 MHz
- 13-bit programmable reference frequency divider
- Programmable charge pump current
- Digital lock detector
- Integrated reference crystal oscillator core
- R/W SPI interface
- Logic compatibility/tolerance 1.8 V/3.3 V
- Low Power Functional mode
- Supply Voltage: 3.0 V to 5.4 V
- Small size exposed pad VFQFPN36 package 6 x 6 x 1.0 mm
- Process: BICMOS 0.25 µm SiGe

Applications

- Cellular/4G infrastructure equipment
- Instrumentation and test equipment
- Cable TV
- Other wireless communication systems

Table 1. Device summary

Order Code	Package	Packing
STW81200T	VFQFPN36	Tray
STW81200TR	VFQFPN36	Tape and reel

Description

The STW81200 is a dual architecture frequency synthesizer (Fractional-N and Integer-N), that features three low phase-noise VCOs with a fundamental frequency range of 3.0 GHz to 6.0 GHz and a programmable dual RF output divider stage which allows coverage from 46.875 MHz to 6 GHz.

The STW81200 optimizes size and cost of the final application thanks to the integration of low-noise LDO voltage regulators and internally-matched broadband RF outputs.

The STW81200 is compatible with a wide range of supply voltages (from 3.0 V to 5.4 V) providing to the end user a very high level of flexibility which trades off excellent performance with power dissipation requirements. A low-power functional mode (software controlled) gives an extra power saving.

Additional features include crystal oscillator core, external VCO mode and output-mute function.

Contents

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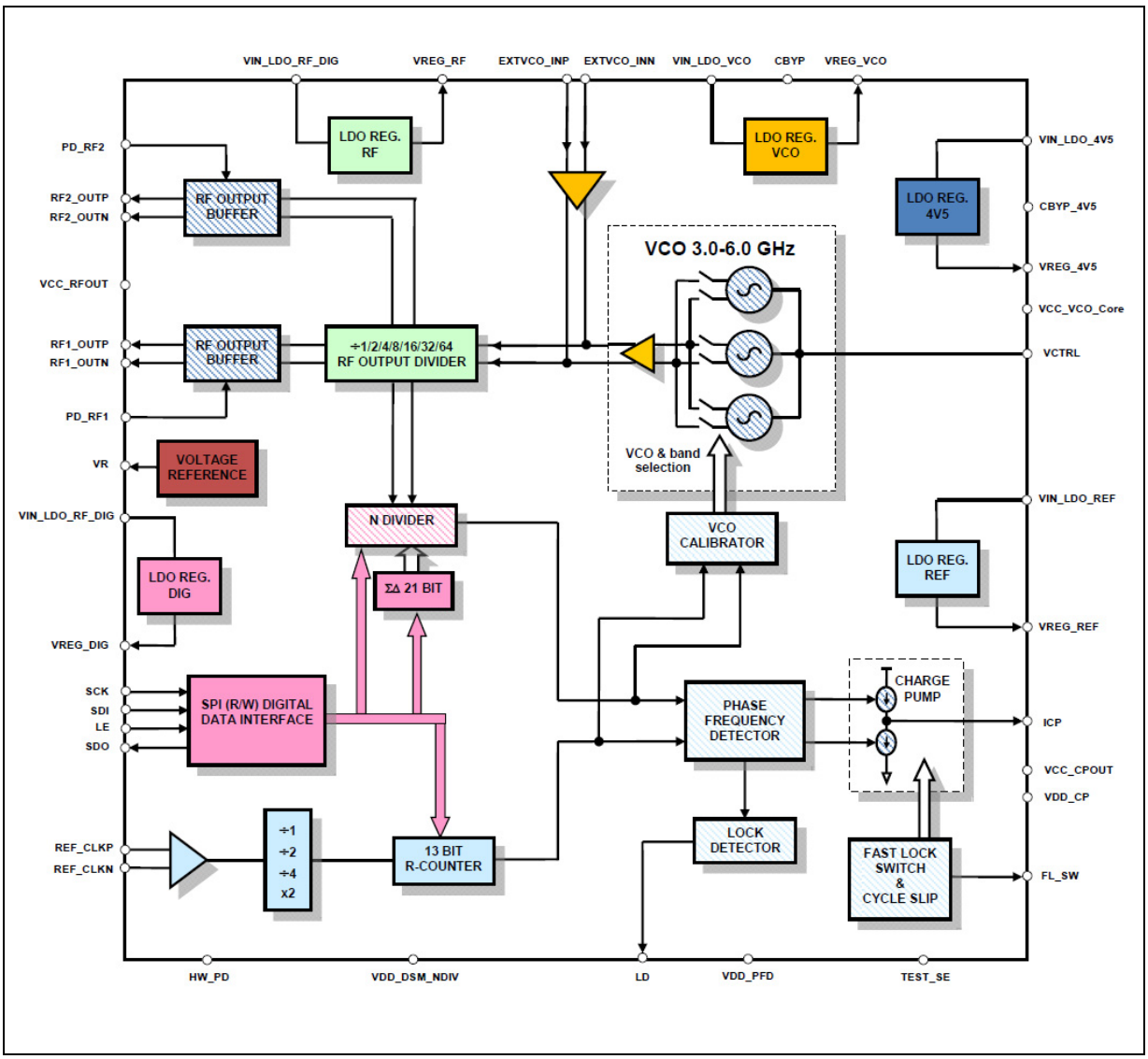
1 Functional block diagram

Figure 1. Functional block diagram



2 Pin definitions

Figure 2. Top view

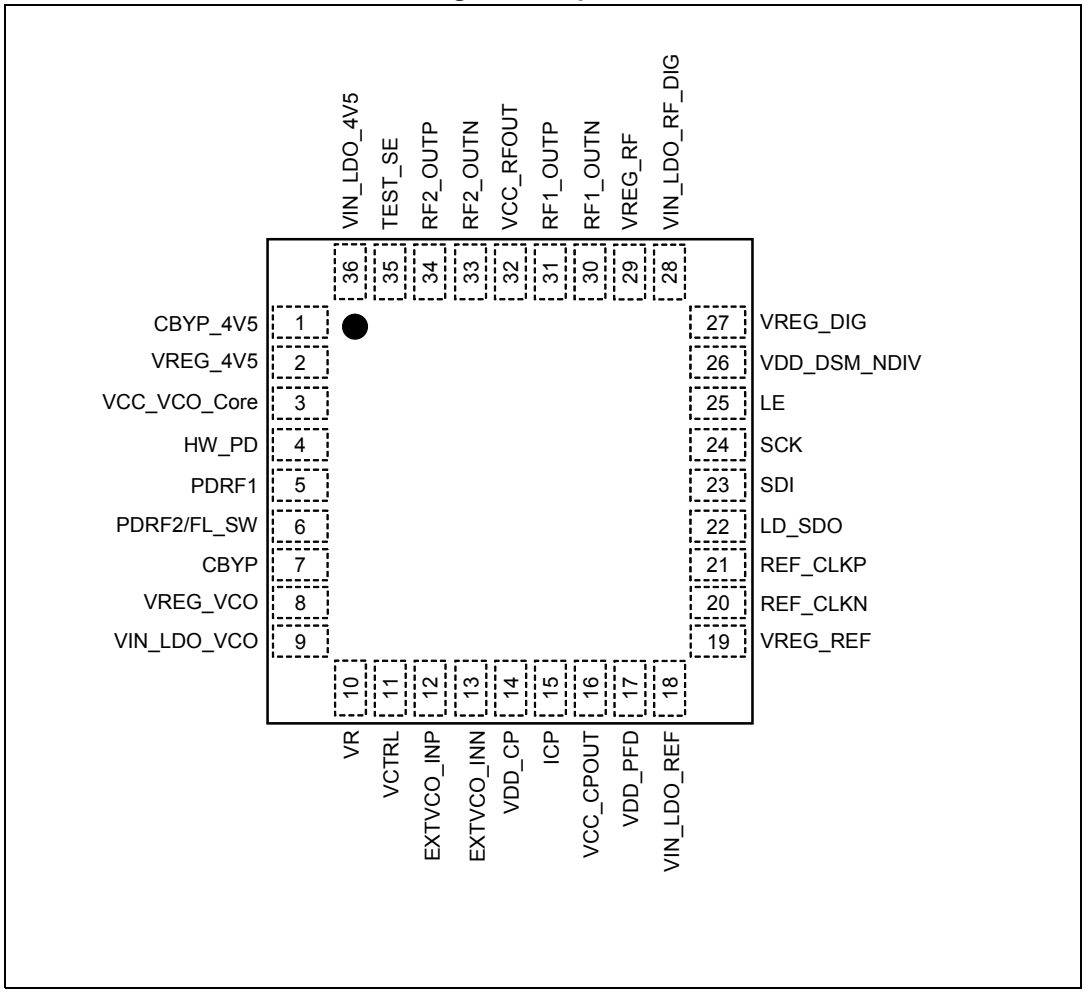


Table 2. Pin description

Pin No	Name	Description	Observation
1	CBYP_4V5	Connection for 4.5 V regulator bypass capacitor	-
2	VREG_4V5	Regulated output voltage for 4.5V regulator	Adjustable output voltage: 5.0 V, 4.5 V, 2.6 V, 3.3 V
3	VCC_VCO_Core	Supply voltage for VCO Core	Must be connected to VREG_4V5 or VREG_VCO
4	HW_PD	HW Power Down	CMOS Schmitt Triggered Input, 1.8 V compatible, 3.3 V tolerant
5	PD_RF1	RF1 output stage Power Down control	CMOS Schmitt Triggered Input, 1.8 V compatible, 3.3 V tolerant
6	PD_RF2/FL_SW	RF2 output stage Power Down Control / Fast Lock switch	CMOS Schmitt Triggered Input, 1.8 V compatible, 3.3V tolerant (with Fast lock feature disabled); High impedance/ GND shorted output (with Fast Lock feature enabled)
7	CBYP	Connection for VCO circuitry regulator bypass capacitor	-
8	VREG_VCO	Regulated output voltage for VCO circuitry regulator	-
9	VIN_LDO_VCO	Supply voltage for VCO circuitry regulator	-
10	VR	Connection for reference voltage filtering capacitor	-
11	VCTRL	VCO control voltage	-
12	EXTVCO_INP	External VCO positive input	This pin must be connected to ground if external VCO is not used
13	EXTVCO_INN	External VCO negative input	This pin must be connected to ground if external VCO is not used
14	VDD_CP	Supply voltage for Charge Pump bias	This pin must be connected to VREG_VCO
15	ICP	PLL charge pump output	-
16	VCC_CPOUT	Supply voltage for Charge Pump output stage	This pin must be connected to VREG_4V5 or VREG_VCO
17	VDD_PFD	Supply voltage for PFD	This pin must be connected to VREG_REF
18	VIN_LDO_REF	Supply voltage for PLL regulator	-
19	VREG_REF	Regulated output voltage for Reference Clock regulator	-
20	REF_CLKN	Reference clock negative input	-
21	REF_CLKP	Reference clock positive input	-

Table 2. Pin description (continued)

Pin No	Name	Description	Observation
22	LD_SDO	Lock Detector/SPI Data output	CMOS push-pull Output 2.5V with slew rate control or open drain (1.8V to 3.3V tolerant)
23	SDI	SPI Data input	CMOS Schmitt triggered Input, 1.8 V compatible, 3.3 V tolerant
24	SCK	SPI clock	CMOS Schmitt triggered Input, 1.8 V compatible, 3.3 V tolerant
25	LE	SPI load enable	CMOS Schmitt triggered Input, 1.8 V compatible, 3.3 V tolerant
26	VDD_DSM_NDIV	Supply voltage for DSM and N divider	This pin must be connected to VREG_DIG
27	VREG_DIG	Regulated output voltage for digital circuitry regulator	-
28	VIN_LDO_RF_DIG	Supply voltage for RF Output divider stage and digital regulators	-
29	VREG_RF	Regulated output voltage for RF Output Divider stage regulator	-
30	RF1_OUTN	Main RF negative output	50 Ω output impedance
31	RF1_OUTP	Main RF positive output	50 Ω output impedance
32	VCC_RFOUT	Supply voltage for RF Output stages	Connected to VREG_DIV, VREG_4V5 or external 5V
33	RF2_OUTN	Auxiliary RF negative output	50 Ω output impedance
34	RF2_OUTP	Auxiliary RF positive output	50 Ω output impedance
35	TEST_SE	Test pin	This pin must be connected to ground
36	VIN_LDO_4V5	Supply voltage for 4.5 V regulator	-

3 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
VCC	Supply voltage pins #14, #17, #26	-0.3 to 2.7	V
	Supply voltage LDOs pins #9, #18, #28, #36	-0.3 to 5.4	V
	Supply voltage pins #3	-0.3 to 5	V
	Supply voltage pins #16, #32	-0.3 to 5.4	V
Tstg	Storage temperature	+150	°C
ESD	Electrical Static Discharge HBM(1) CDM-JEDEC Standard MM	 2 0.5 0.2	kV

1. The maximum rating of the ESD protection circuitry on pin 21 (REF_CLKP) is 1.5 kV.

4 Operating conditions

Table 4. Operating conditions

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{CC}	Supply voltage pins #14, #17, #26	-	2.5	-	2.7	V
	Supply voltage (LDOs inputs) pins #9, #18, #28, #36	-	3.0	-	5.4	V
	Supply voltage pin #3, #16, #32	-	2.5	-	5	V
I_{CC}	Current Consumption Pin #3, #16 and #32 supplied at 4.5 V	DIV2 ON, Main Output only, 4 GHz VCO, max. performance	-	84	-	mA
	Current Consumption Pin #3, #16 and #32 supplied at 2.6 V		-	50	-	mA
	Current consumption other blocks an supplies at 2.6 V		-	110	-	mA
T_A	Operating ambient temperature	-	-40	-	85	°C
T_J	Maximum junction temperature	-	-	-	125	°C
Θ_{JA}	Junction to ambient package thermal resistance(1)	Multilayer JEDEC board	-	33	-	°C/W
Θ_{JB}	Junction to board package thermal resistance(1)	Multilayer JEDEC board	-	18	-	°C/W
Θ_{JC}	Junction to case package thermal resistance(1)	Multilayer JEDEC board	-	3	-	°C/W
Ψ_{JB}	Thermal characterization parameter junction to board(1)	Multilayer JEDEC board	-	17	-	°C/W
Ψ_{JT}	Thermal characterization parameter junction to top case(1)	Multilayer JEDEC board	-	0.3	-	°C/W

1. Refer to JEDEC standard JESD 51-12 for a detailed description of the thermal resistances and thermal parameters. Data here presented are referring to a Multilayer board according to JEDEC standard.
$T_J = T_A + \Theta J_A * P_{diss}$ (in order to estimate T_J if ambient temperature T_A and dissipated power P_{diss} are known)
$TJ = T_B + \Psi_{JB} * P_{diss}$ (in order to estimate T_J if ambient temperature T_B and dissipated power P_{diss} are known)
$T_J = T_T + \Psi_{JT} * P_{diss}$ (in order to estimate T_J if ambient temperature T_T and dissipated power P_{diss} are known)

Table 5. Digital logic levels

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
Vdd	Internal Supply for digital circuits	-	-	2.6	-	V
Vil	Low level input voltage	Schmitt input	0	-	0.6	V
Vih	High level input voltage	Schmitt input	1.2	-	3.6	V
Vol	Low level output voltage	I_{OL} = 4 mA	-	-	0.2	V
Voh	High level output voltage	I_{OH} = 4 mA	Vdd-0.2	-	-	V

5 Electrical specifications

All electrical specifications are given at 25°C T_{AMB} and in a full-current mode, unless otherwise stated.

Table 6. Electrical specifications

Symbol	Parameter	Condition	Min	Typ	Max	Units
Output frequency range						
F_{OUT}	Output Frequency	Direct output	3000	-	6000	MHz
		Divider by 2 output	1500	-	3000	MHz
		…	…	-	…	MHz
		Divider by 64 output	46.875	-	93.75	MHz
VCO dividers						
N	VCO Divider Ratio	Integer Mode	24	-	131071	-
		Fractional mode (DSM 1st Order)	24	-	510	-
		Fractional mode (DSM 2nd Order)	25	-	509	-
		Fractional mode (DSM 3rd Order)	27	-	507	-
		Fractional mode (DSM 4st Order)	31	-	503	-
Xtal oscillator						
F_{XTAL}	XTAL frequency range	-	10	-	50	MHz
ESR_{XTAL}	XTAL ESR	-	-	-	50	Ω
P_{XTAL}	XTAL Power Dissipation	-	-	-	5	mW
CIN_{XTAL}	XTAL Oscillator Input capacitance	Single ended	0.6	-	-	pF
PN_{XTAL}	XTAL Oscillator Phase Noise Floor	50 MHz XTAL	-	-162	-	dBc/Hz
TOL_{XTAL}	XTAL Oscillator accuracy	@12 MHz, 25 ºC	-	-	10	ppm
Reference clock and phase frequency detector						
F_{ref}	Reference input frequency(1)	-	10	-	800	MHz
	Reference input sensitivity	Differential Mode	0.2	1	1.25	Vp
		Single Ended Mode	0.35	1	1.25	Vp
PN_{REFIN}	Reference Input Buffer Phase Noise Floor	Single Ended Mode @100 MHz, sinusoidal signal 1.25 Vp	-	-163	-	dBc/Hz
		LVDS signal @100 MHz 400 mVp	-	-159	-	dBc/Hz

Table 6. Electrical specifications (continued)

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{REF}	Current consumption(2)	Differential Mode	-	10	-	mA
		Single Ended Mode	-	3	-	
		XTAL oscillator Mode	-	5	-	
R	Reference Divider Ratio	-	1	-	8191	
F_{PFD}	PFD input frequency(3)	-	-	-	100	MHz
F_{STEP}	Frequency step(3)	LO direct output	-	47.5	-	Hz
		LO with divider by 2	-	23.75	-	Hz
		…	-	…	-	Hz
		LO with divider by 64	-	0.7422	-	Hz
Charge pump						
VCC_{CPOUT}	CP Supply	Pin # 16 (VCC_CPOUT)	2.5	-	5	V
I_{CP}	ICP sink/source	5-bit programmable	-	-	4.9	mA
V_{ICP}	Output voltage range on ICP pin (pin#14)	-	0.4	-	VCC_{CPOUT} -0.4	V
-	Comparison frequency Spurs (4)	-	-	-85	-	dBc
-	In-Band Fractional Spurs (5)	-	-	-50	-	
VCOs						
$VCC_{VCOCore}$	VCO Core Supply	Pin # 3 (VCC_VCO_Core)	2.5	-	5	V
$I_{VCOCore}$	Oscillator Core current consumption	@ 4 GHz and 4.5 V supply	-	52	-	mA
		@ 4 GHz and 3.3 V supply	-	35	-	
		@ 4 GHz and 2.6 V supply	-	30	-	
I_{VCOBUF}	VCO buffer consumption	Pin # 3 (VCC_VCO_Core)	-	35	-	mA
K_{VCO}	VCO gain	-	-	35-95	-	MHz/V
ΔT_{LK}	Maximum temperature variation for continuous lock(6)(7)	Pin #16 @4.5/5 V	-125	-	125	°C
		Pin #16 @3.3 V	-125	-	125	°C
		Pin #16 @2.6 V	-125	-	115	°C
RF output stage						
VCC_{RFOUT}	RF Output supply	Pin # 35 (VCC_RFOUT)	2.5	-	5	V
P_{OUT}	Output level	Differential 3.3 V to 5 V supply	-1	-	+7	dBm
	-	Differential 2.6 V supply	-1	-	+1	
Z_{OUT}	Output impedance	Differential	-	100	-	Ω
		Single Ended	-	50	-	Ω
R_L	Return Loss	Matched to 50-ohm Single Ended	-	15	-	dB

Table 6. Electrical specifications (continued)

Symbol	Parameter	Condition	Min	Typ	Max	Units
H_2	LO 2nd Harmonic	Direct output (single/differential)	-	-30/-40	-	dBc
		Divided output (single/differential)	-	-30/-35	-	dBc
H_3	LO 3rd Harmonic	Direct output (single/differential)	-	-15/-15	-	dBc
		Divided output (single/differential)	-	-15/-15	-	dBc
P_{MUTE}	Level of Signal with RF Mute Enabled	Direct output @4 GHz (single/diff)	-	-45/-60	-	dBm
		Divided output @2 GHz (single/diff)	-	-45/-60	-	dBm
P_{ISO}	Main/aux port isolation	Direct output @4 GHz (single/diff)	-	-35/-40	-	dBc
		Divided output @2 GHz (single/diff)	-	-40/-45	-	dBc
I_{DIV}	RF Divider Current Consumption(8)	Direct output (1 differential output)	-	28	-	mA
		DIV2 buff (1 differential output)	-	47	-	
		DIV4 buff (1 differential output)	-	56	-	
		DIV8 buff (1 differential output)	-	65	-	
		DIV16 buff (1 differential output)	-	75	-	
		DIV32 buff (1 differential output)	-	83		
		DIV64 buff (1 differential output)	-	92	-	
		Auxiliary path enabled	-	19	-	
$I_{RFOUTBUF}$	RF Output Buffer Current Consumption(8)	3.3 V to 5 V supply (1 differential output; P_{OUT} = +7 dBm)	-	25	-	mA
		3.3 V to 5 V Auxiliary path enabled	-	25	-	
		2.6 V supply (1 differential output; P_{OUT} = +1 dBm)	-	12	-	
		2.6 V Auxiliary path enabled	-	12	-	

Table 6. Electrical specifications (continued)

Symbol	Parameter	Condition	Min	Typ	Max	Units
PLL miscellaneous						
I_{PLL}	PLL current Consumption(8)	Prescaler, digital dividers, misc.	-	20	-	mA
I_{DSM}	ΔΣ Modulator current consumption(8)	-	-	3.5	-	mA

1. The maximum frequency of the Reference Divider is 200 MHz; when using higher reference clock frequency (up to the max. value of 800 MHz) the internal divider by 2 or divider by 4 must be enabled.
   The fractional mode is allowed in the full frequency range only with reference clock frequency >11.93 MHz
   With reference clock frequency in the range 10 MHz to 11.93 MHz, due to the limits of N value in fractional mode, the full VCO frequencies would not be addressed in fractional mode; in this case the frequency doubler in the reference path can be enabled.
2. Reference clock signal @ 100 MHz, R=2
3. The minimum frequency step is obtained as F_{PFD} / (2^21); these typical values are obtained considering F_{PFD} = 100 MHz.
4. PFD frequency leakage.
5. This is the level inside the PLL loop bandwidth due to the contribution of the ΔΣ Modulator. In order to obtain the fractional spurs level for a specific frequency offset, the attenuation provided by the loop filter at such offset should be subtracted.
6. Once a VCO is programmed at the initial temperature T_0 inside the operating temperature range (-40 °C to +85 °C), the synthesizer is able to maintain the lock status only if the temperature drift (in either direction) is within the limit specified by ΔT_{LK}, provided that the final temperature T_f is still inside the nominal range.
7. In order to guarantee the performance of ΔT_{LK} the bit CAL_TEMP_COMP in register ST6 must be set to ‘1’.
8. Current consumption measured with PLL locked in following conditions: Reference clock signal @ 100 MHz; PFD @50 MHz (R=2); VCO @ 4005 MHz

Table 7. Phase noise specifications

Parameter	Min	Typ	Max	Units
Normalized In-Band Phase Noise(1) Floor(2)	-	-227	-	dBc/Hz
VCO Open Loop Phase Noise(1) at F_{OUT} @ 4 GHz – VIN=5.0 V, VREG=4.5 V				
Phase Noise @ 1 kHz	-	-64	-	dBc/Hz
Phase Noise @ 10 kHz	-	-91	-	dBc/Hz
Phase Noise @ 100 kHz	-	-114	-	dBc/Hz
Phase Noise @ 1 MHz	-	-135	-	dBc/Hz
Phase Noise @ 10 MHz	-	-154	-	dBc/Hz
Phase Noise @ 100 MHz	-	-160	-	dBc/Hz
VCO Open Loop Phase Noise(1) at F_{OUT} @ 4 GHz/2 = 2GHz – VIN=5.0 V, VREG=4.5 V				
Phase Noise @ 1 kHz	-	-70	-	dBc/Hz
Phase Noise @ 10 kHz	-	-97	-	dBc/Hz
Phase Noise @ 100 kHz	-	-120	-	dBc/Hz
Phase Noise @ 1 MHz	-	-141	-	dBc/Hz
Phase Noise @ 10 MHz	-	-156	-	dBc/Hz
Phase Noise @ 40 MHz	-	-159	-	dBc/Hz
VCO Open Loop Phase Noise(1) at F_{OUT} @ 4 GHz/4 = 1 GHz – VIN=5.0 V, VREG=4.5 V				
Phase Noise @ 1 kHz	-	-76	-	dBc/Hz
Phase Noise @ 10 kHz	-	-103	-	dBc/Hz
Phase Noise @ 100 kHz	-	-126	-	dBc/Hz
Phase Noise @ 1 MHz	-	-146	-	dBc/Hz
Phase Noise @ 10 MHz	-	-159	-	dBc/Hz
Phase Noise Floor	-	-160	-	dBc/Hz
VCO Open Loop Phase Noise(1) at F_{OUT} @ 4 GHz/32 = 125 MHz – VIN=5.0 V, VREG=4.5 V				
Phase Noise @ 1 kHz	-	-92	-	dBc/Hz
Phase Noise @ 10 kHz	-	-121	-	dBc/Hz
Phase Noise @ 100 kHz	-	-144	-	dBc/Hz
Phase Noise @ 1 MHz	-	-161	-	dBc/Hz
Phase Noise @ 10 MHz	-	-163	-	dBc/Hz
Phase Noise Floor	-	-164	-	dBc/Hz

Table 7. Phase noise specifications

Parameter	Min	Typ	Max	Units
VCO Open Loop Phase Noise(1) at F_{OUT} @ 4 GHz – VIN=3.6V , VREG=3.3 V				
Phase Noise @ 1 kHz	-	-62	-	dBc/Hz
Phase Noise @ 10 kHz	-	-89	-	dBc/Hz
Phase Noise @ 100 kHz	-	-113.2	-	dBc/Hz
Phase Noise @ 1 MHz	-	-133.6	-	dBc/Hz
Phase Noise @ 10 MHz	-	-152.4	-	dBc/Hz
Phase Noise @ 100 MHz	-	-158.5	-	dBc/Hz
VCO Open Loop Phase Noise(1) at F_{OUT} @ 4 GHz – VIN=3.0 V, VREG=2.6 V				
Phase Noise @ 1 kHz	-	-60.5	-	dBc/Hz
Phase Noise @ 10 kHz	-	-88	-	dBc/Hz
Phase Noise @ 100 kHz	-	-110.3	-	dBc/Hz
Phase Noise @ 1 MHz	-	-131	-	dBc/Hz
Phase Noise @ 10 MHz	-	-150	-	dBc/Hz
Phase Noise @ 100 MHz	-	-157	-	dBc/Hz

1. Phase Noise SSB unless otherwise specified. The VCO Open loop figures are specified at 4.5/5 V on VCC_VCO_Core (pin #3).
2. Normalized PN = Measured PN – 20log(N) – 10log(F_{PFD}) where N is the VCO divider ratio and F_{PFD} is the comparison frequency at the PFD input.

6 Typical Performance Characteristics

Figure 3. VCO open-loop phase noise (5 V supply)

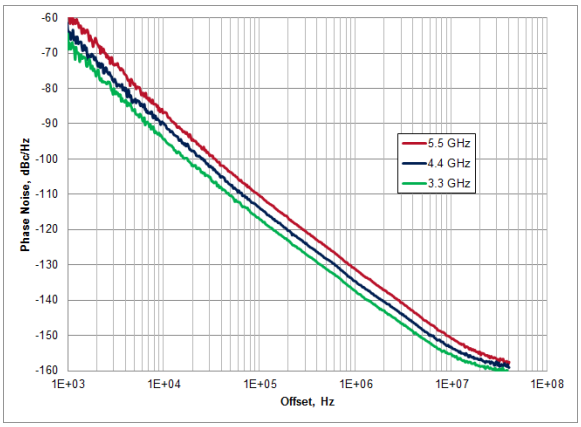


Figure 4. Closed-loop phase noise at 4.8 GHz, divided by 1 to 64 (5 V supply)

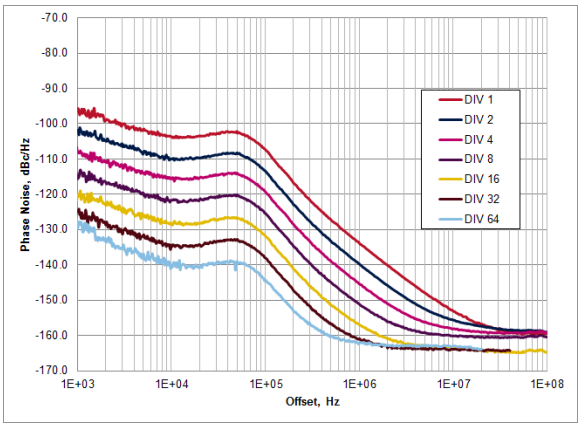


Figure 5. VCO open-loop phase noise at 4.4 GHz vs. supply

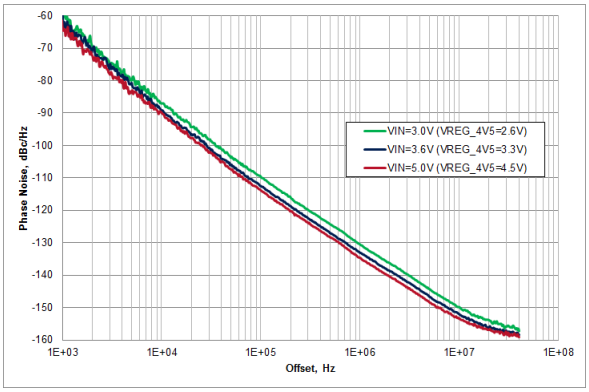


Figure 6. VCO open-loop phase noise over frequency vs. supply

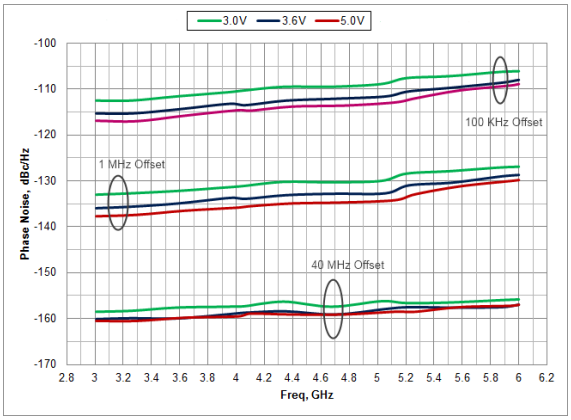


Figure 7. Single sideband integrated phase noise vs. frequency and supply (F_{PFD}= 50 MHz)

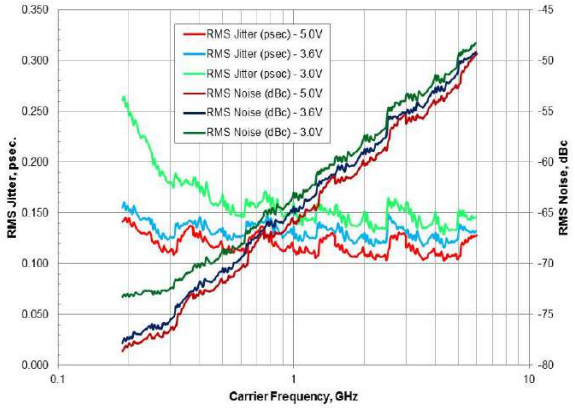


Figure 8. Figure of merit

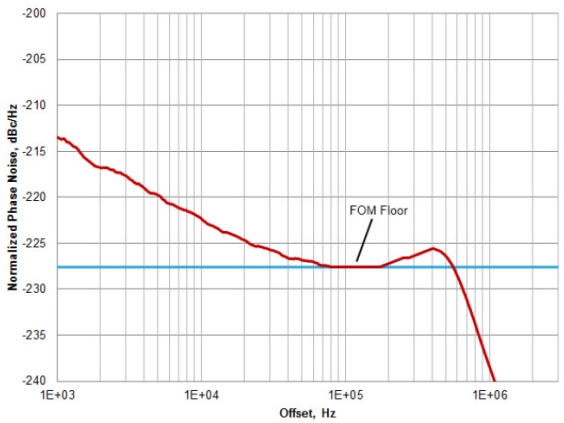


Figure 9. Phase noise and fractional spurs at 2646.96 MHz vs. supply (F_{PFD} = 61.44 MHz)

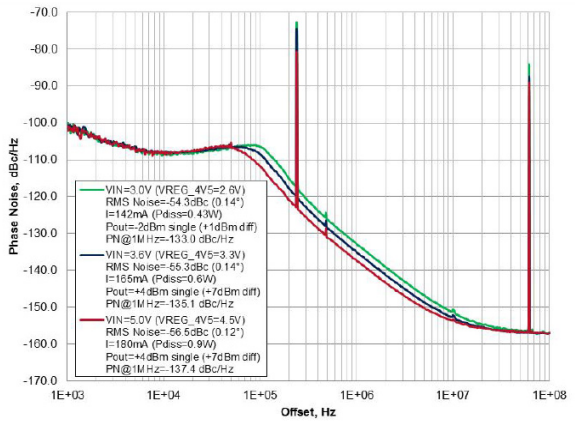


Figure 10. Phase noise and fractional spurs at 2118.24 MHz vs. supply (F_{PFD} = 61.44 MHz)

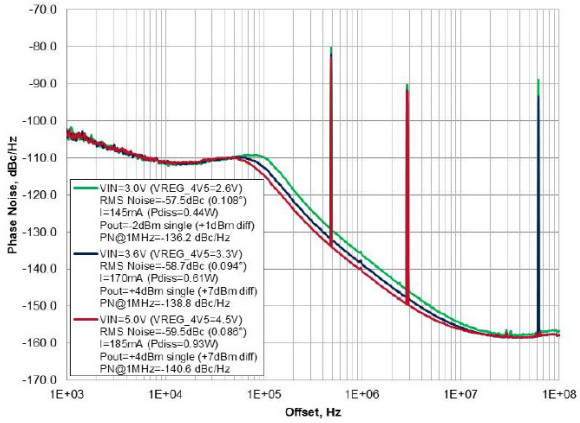


Figure 11. Phase noise and fractional spurs at 2118.24 MHz at 5.0 V supply (F_{PFD} = 61.44 MHz)

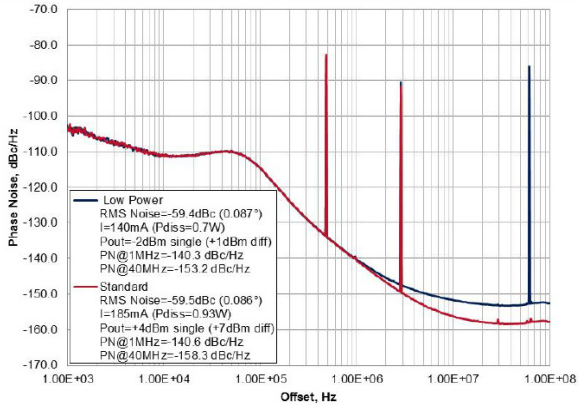


Figure 12. Phase noise and fractional spurs at 2118.24 MHz at 3.6 V supply (F_{PFD} = 61.44 MHz)

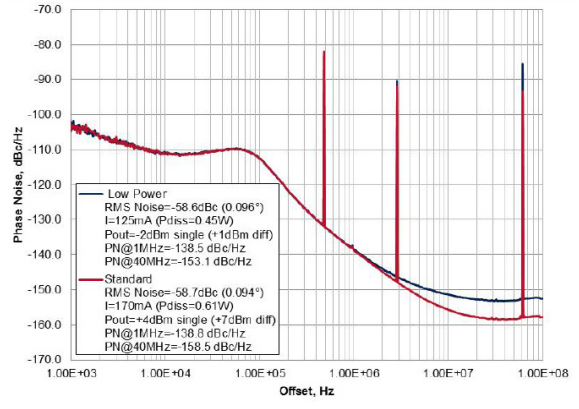


Figure 13. Phase noise and fractional spurs at 2118.24 MHz at 3.0 V supply (F_{PFD} = 61.44 MHz)

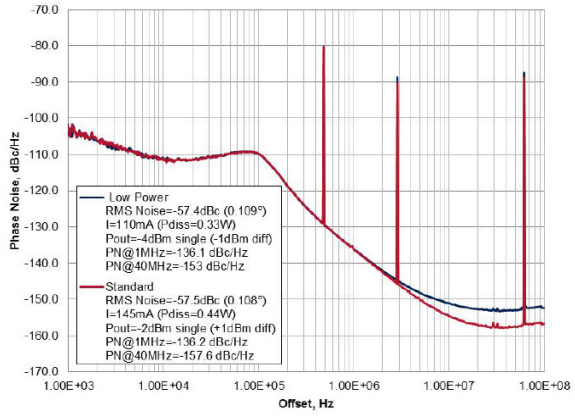


Figure 14. Phase noise at 5.625 GHz and 4.6 GHz (F_{PFD} = 50 MHz)

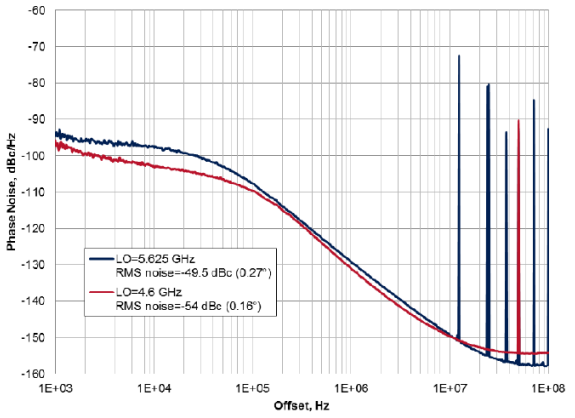


Figure 15. Typical VCO control voltage after VCO calibration (3.6 V supply)

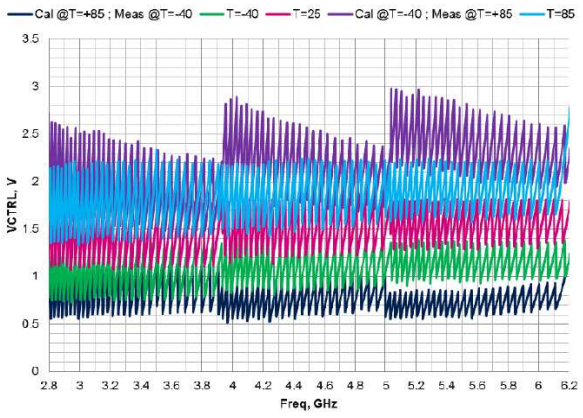


Figure 16. Average K_{VCO} over VCO frequency and supply

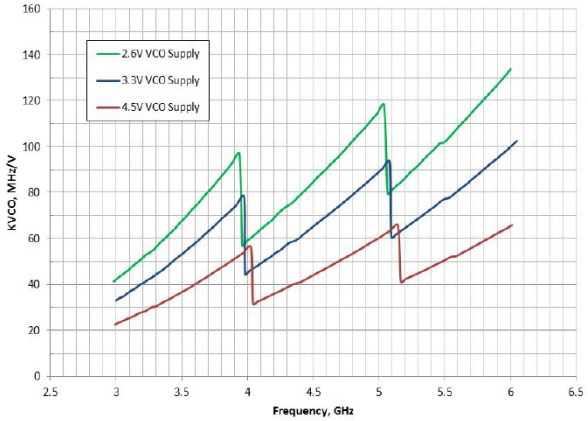


Figure 17. Output power level vs. temperature - single ended (RF_OUT_PWR=7)

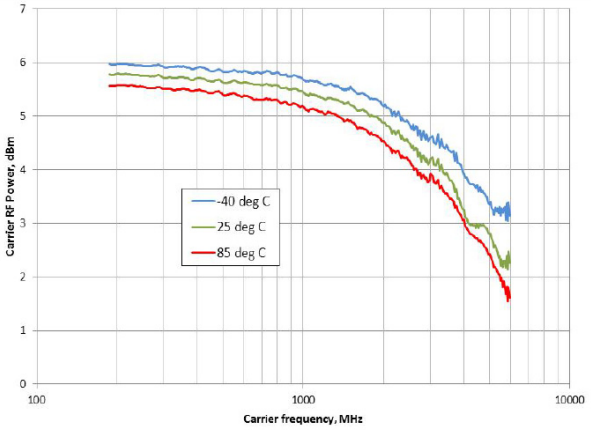


Figure 18. Output power level – single ended (3 dB more for differential)

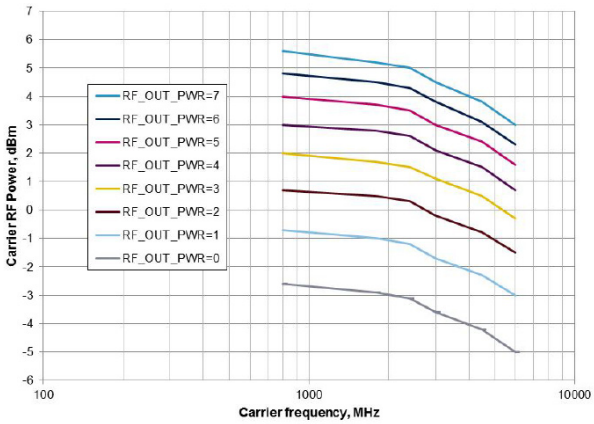


Figure 19. Typical spur level at PFD offset over carrier frequency (5.0 V supply)

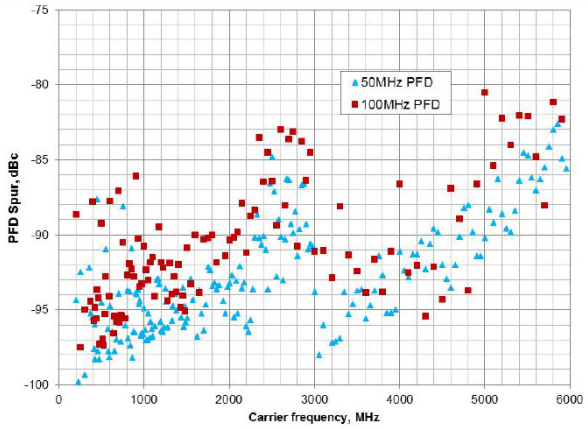


Figure 20. Typical spur level vs. offset from 4.5 GHz (5.0 V supply, F_{PFD}=50MHz)

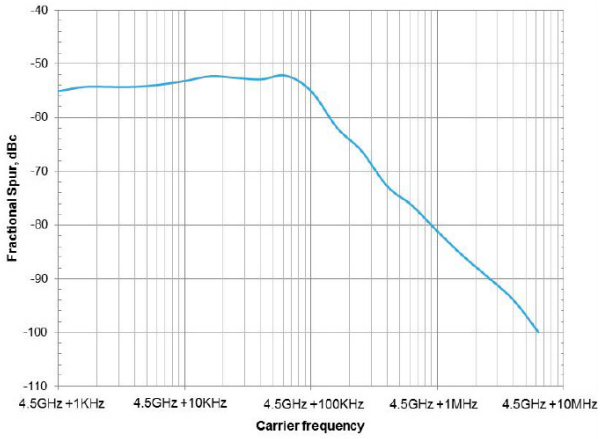


Figure 21. 10 kHz fractional spur (integer boundary) vs. temperature (5.0 V supply, F_{PFD} = 50 MHz)

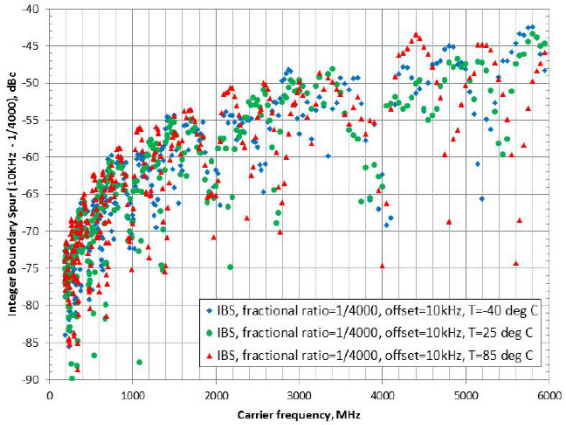


Figure 22. 800 kHz fractional spur (integer boundary) vs. temperature (5.0 V supply, F_{PFD} = 50 MHz)

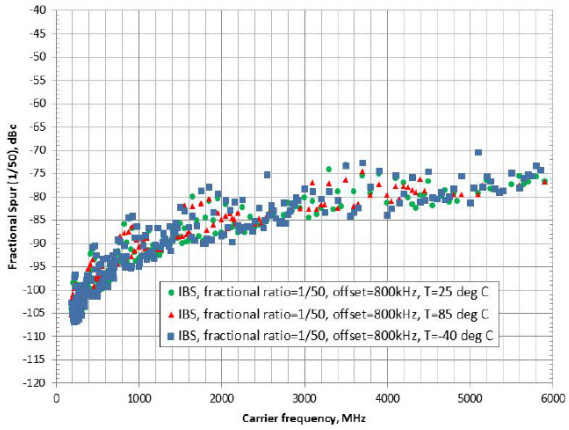


Figure 23. Frequency settling with VCO calibration – wideband view

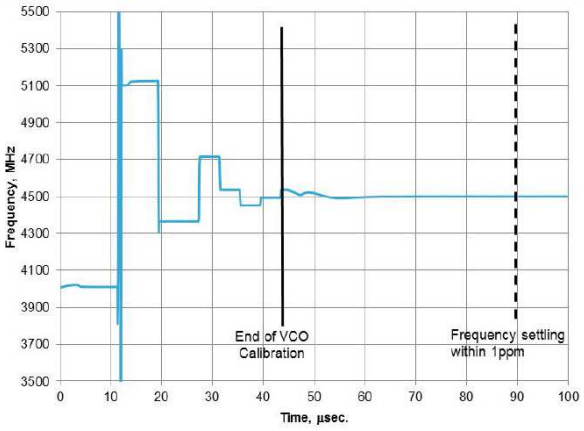


Figure 24. Frequency settling with VCO calibration – narrowband view

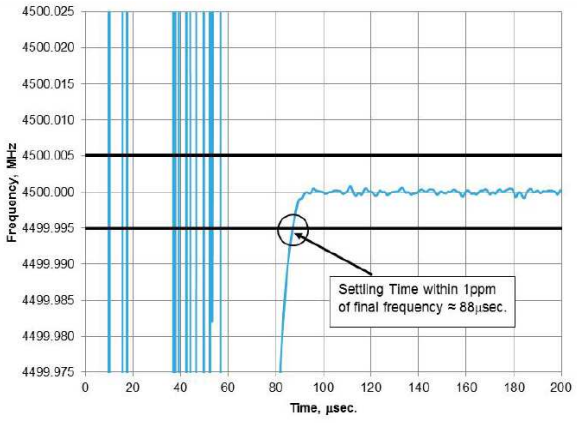


Figure 25. Overall current consumption vs. temperature (5.0 V supply, F_{PFD} = 50 MHz)

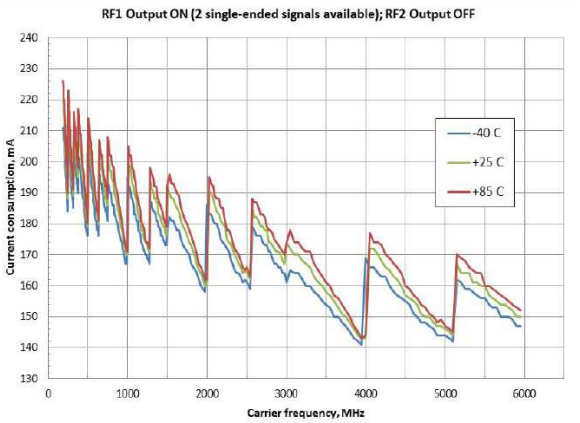


Figure 26. Current consumption – standard vs. low power (5.0 V supply, F_{PFD} = 50 MHz)

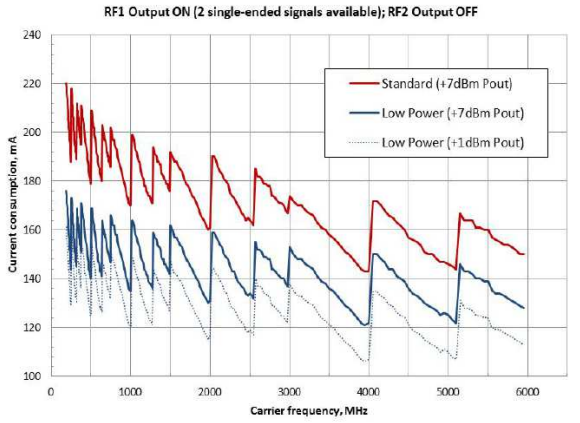


Figure 27. Current consumption – standard vs. low power (3.6 V supply, F_{PFD} = 50 MHz)

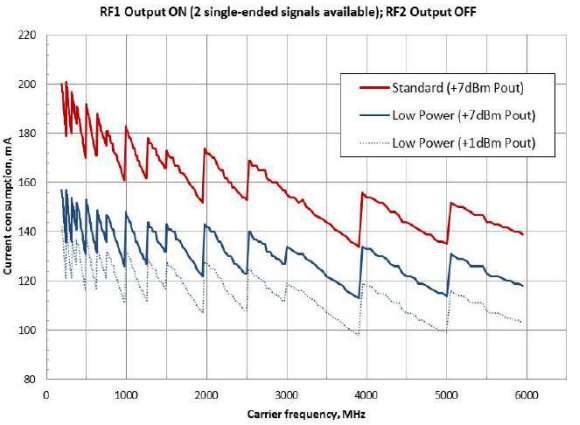
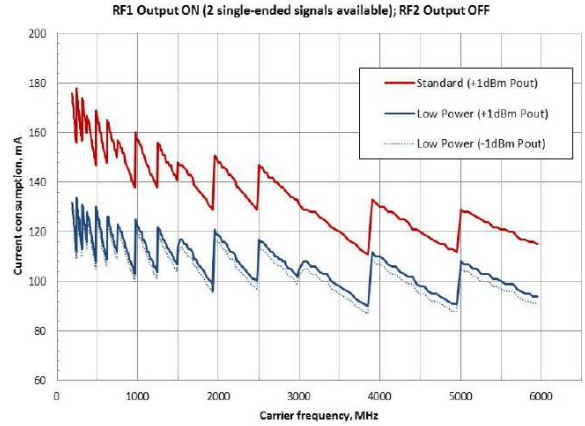


Figure 28. Current consumption – standard vs. low power (3.0 V supply, F_{PFD} = 50 MHz)



7 Circuit description

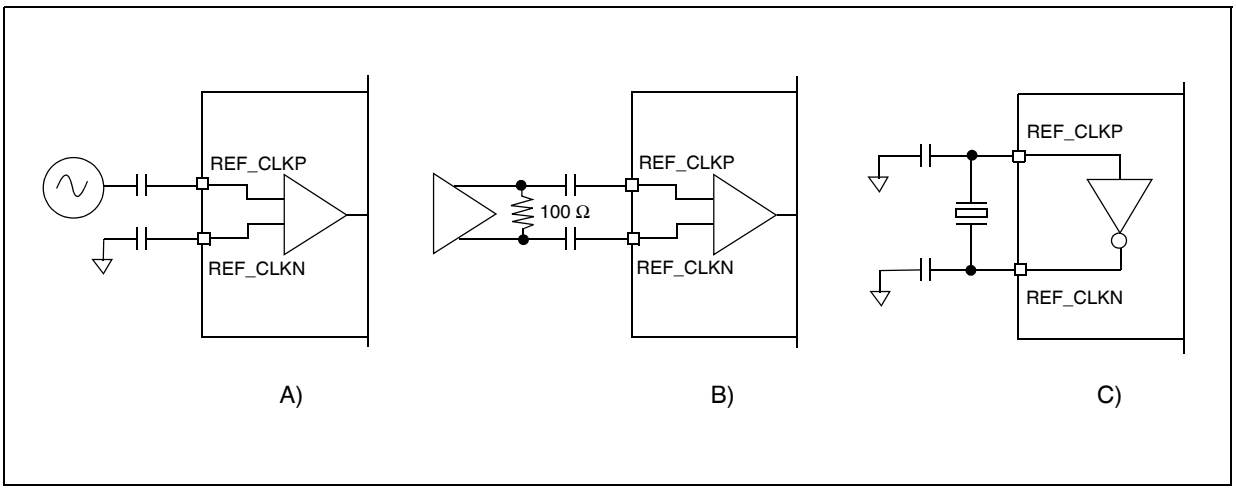
7.1 Reference input stage

The reference input stage provides different modes for the reference clock signal.

Both single-ended and differential modes (LVDS, LVECPL) are supported; a crystal mode is also provided in order to build a Pierce type crystal oscillator. *Figure 29* shows the connections required for the different configurations supported.

In single-ended and differential modes the inputs must be AC coupled as the REF_CLKP and REF_CLKN pins are internally biased to an optimal DC operating point. The input resistance is 100 ohms differential and the best performance for phase noise is obtained for signals with a higher slew rate, such as a square wave.

Figure 29. Reference clock buffer configurations: single-ended (A), differential (B), crystal mode (C)



7.2 Reference divider

The 13-bit programmable reference counter is used to divide the input reference frequency to the desired PFD frequency. The division ratio is programmable from 1 to 8191.

The maximum allowed input frequency of the R-Counter is 200 MHz.

The reference clock can be extended up to 400 MHz enabling the divide-by-2 stage or up to 800 MHz enabling the divide-by-4 stage.

A frequency doubler is provided in order to double low reference frequencies and increase the PFD operating frequency thus allowing an easier filtering of the out-of-band noise of the Delta-Sigma Modulator; the doubler is introducing a noise degradation in the in-band PLL noise thus this feature should be carefully used.

When the doubler is enabled, the maximum reference frequency is limited to 25 MHz.

7.3 PLL N divider

The N divider sets the division ratio in the PLL feedback path.

Both Integer-N and Fractional-N PLL architectures are implemented in order to ensure the best overall performance of the synthesizer.

The Fractional-N division is achieved combining the integer divider section with a Delta-Sigma modulator (DSM) which sets the fractional part of the overall division ratio.

The DSM is implemented as a MASH structure with programmable order (2 bit; 1^{st}, 2^{nd}, 3^{rd} and 4^{th} order), programmable MODULUS (21 bit).

It includes also a DITHERING function (1 bit) which can be used to reduce fractional spur tones by spreading the DSM sequence and consequently the energy of the spurs over a wider bandwidth.

The overall division ratio N is given by:

$$N = N_{INT} + N_{FRAC}$$

The integer part N_{INT} is 17-bit programmable and can range from 24 to 131071 in Integer Mode. For $N_{INT} \geq 512$ the fractional mode is not allowed and the setting used for DSM does not have any effect.

Based upon the selected order of the Delta-Sigma Modulator the allowed range of N_{INT} values changes as follows:

- 24 to 510 - 1st Order DSM
- 25 to 509 - 2nd Order DSM
- 27 to 507 - 3rd Order DSM
- 31 to 503 - 4th Order DSM

The fractional part N_{FRAC} of the division ratio is controlled by setting the values FRAC and MOD (21 bits each) and it depends also on the value of DITHERING (1 bit):

$$N_{FRAC} = \frac{FRAC}{MOD} + \frac{DITHERING}{2 \cdot MOD}$$

The MOD value can range from 2 to 2097151, while the range of FRAC is from 0 to MOD-1. If the DITHERING function is not used (DITHERING=0) the fractional part of N is simply achieved as ratio of FRAC over MOD.