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STW82102B

RF down converter with embedded integer-N synthesizer

Datasheet –production data

Features

- High linearity:
  - IIP3: +25.5 dBm
  - 2FRF-2FLO spurious rejection: 85 dBc
- Noise figure:
  - NF: 10.5 dB
- Conversion gain
  - CG: 8 dB
- RF range: 1425 MHz to 1910 MHz
- Wide IF amplifier frequency range: 70 MHz to 400 MHz
- Integrated RF balun with internal matching
- Dual differential integrated VCOs with automatic center frequency calibration:
  - LOA: 1500 to 1800 MHz
  - LOB: 1900 to 2200 MHz
- Embedded integer-N synthesizer
  - Dual modulus programmable prescaler (16/17 or 19/20)
  - Programmable reference frequency divider (10 bits)
  - Adjustable charge pump current
  - Digital lock detector
  - Excellent integrated phase noise
  - Fast lock time: 150 µs
- Integrated DAC with dual current output
- Supply: 3.3 V and 5 V analog, 3.3 V Digital
- Dual digital bus interface: SPI and I^2C bus (fast mode) with 3 bit programmable address ($1101A_2A_1A_0$)
- Process: 0.35 µm BICMOS SiGe
- Operating temperature range -40 to +85°C
- 44-lead exposed pad VFQFPN package 7x7x1.0 mm

VFQFPN-44

Applications

- Cellular infrastructure equipment:
  - IF sampling receivers
  - Digital PA linearization loops
- Other wireless communication systems.

Table 1. Device summary

Part number	Package	Packaging
STW82102B	VFQFPN-44	Tray
STW82102BTR	VFQFPN-44	Tape and reel

Description

The STMicroelectronics STW82102B is an integrated down converter providing 8 dB of gain, 10.5 dB NF, and a very high input linearity by means of its passive mixer.

Embedding two wide band auto calibrating VCOs and an integer-N synthesizer, the STW82102B is suitable for both Rx and Tx requirements for cellular infrastructure equipment.

The integrated RF balun and internal matching permit direct 50 ohm single-ended interface to RF port. The IF output is suitable for driving 200-ohm impedance filters.

By embedding a DAC with dual current output to drive an external PIN diode attenuator, the STW82102B replaces several costly discrete components and offers a significant footprint reduction.

The STW82102B device is designed with STMicroelectronics advanced 0.35 µm SiGe process. Its performance is specified over a -40 °C to +85 °C temperature range.

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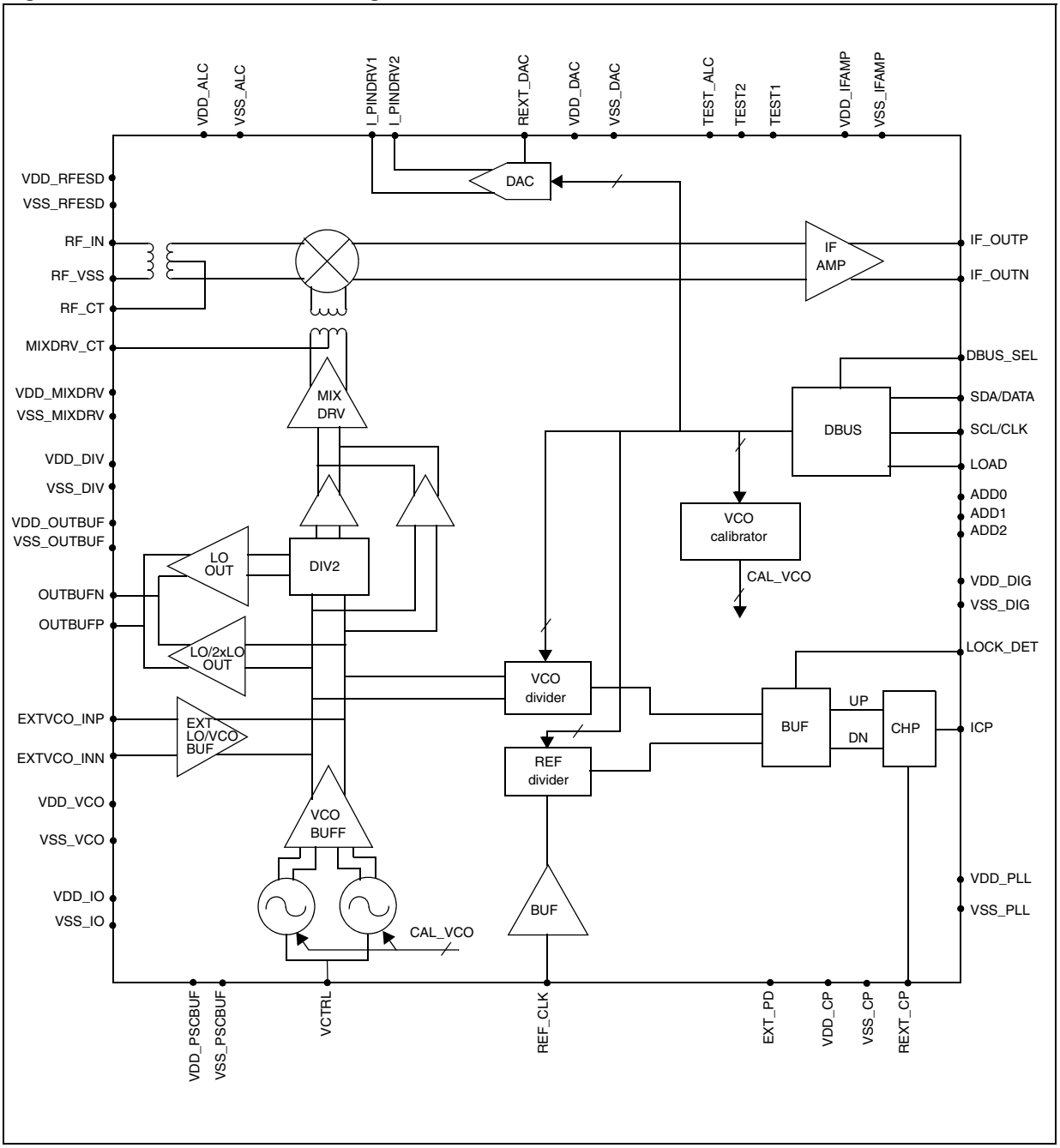
1 Block diagram

Figure 1. STW82102B block diagram



2 Pin description

Figure 2. STW82102B pin configuration

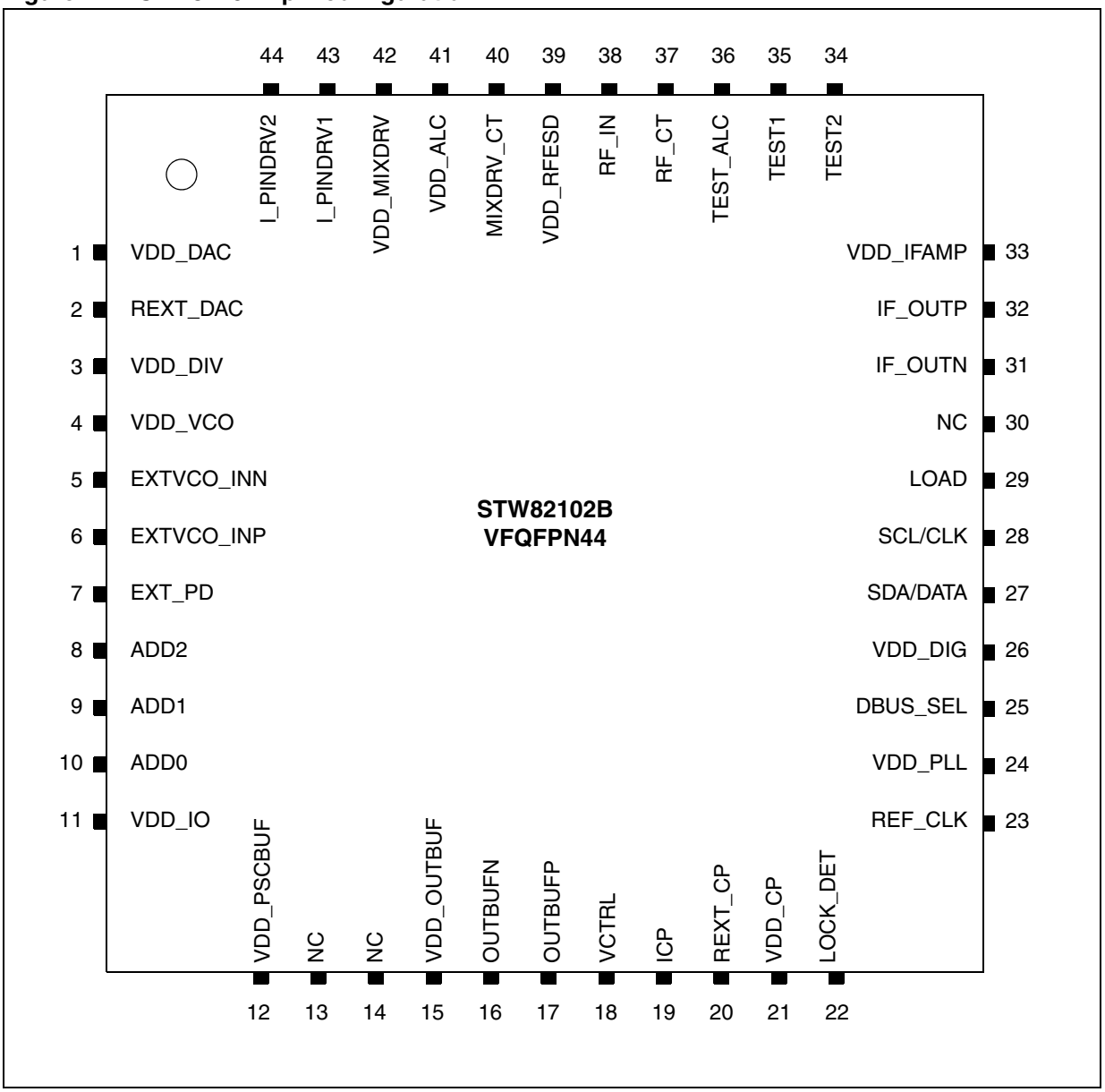


Table 2. Pin list

Pin No	Name	Description	Observation
1	VDD_DAC	DAC power supply	Vsupply analog1= 3.3 V
2	REXT_DAC	External resistance connection for DAC	-
3	VDD_DIV	Divider by 2 power supply	Vsupply analog1= 3.3 V
4	VDD_VCO	VCOs and External VCO Buffer power supply	Vsupply analog1= 3.3 V
5	EXTVCO_INN	External VCO (LO) negative input	Diversity Slave Mode and External VCO Modes; otherwise it must be connected to GND
6	EXTVCO_INP	External VCO (LO) positive input	Diversity Slave Mode and External VCO Modes; otherwise it must be connected to GND
7	EXT_PD	Hardware power down: '0' device ON; '1' device OFF	CMOS Input
8	ADD2	I^2CBUS address select pin	CMOS Input
9	ADD1	I^2CBUS address select pin	CMOS Input
10	ADD0	I^2CBUS address select pin	CMOS Input
11	VDD_IO	Digital IO power supply	Vsupply digital = 3.3 V
12	VDD_PSCBUF	Prescaler input buffer power supply	Vsupply analog1= 3.3 V
13	NC	Not connected	-
14	NC	Not connected	-
15	VDD_OUTBUF	Power supply for LO buffer	Vsupply analog1=3.3 V
16	OUTBUFN	LO Output buffer negative output	Open collector @3.3 V
17	OUTBUFP	LO Output buffer positive output	Open collector @ 3.3 V
18	VCTRL	Control voltage for VCOs	-
19	ICP	PLL charge pump output	-
20	REXT_CP	External resistance connection for PLL charge pump current	-
21	VDD_CP	Power supply for charge pump	Vsupply analog1= 3.3 V
22	LOCK_DET	Lock detector	CMOS Output
23	REF_CLK	Reference frequency input	-
24	VDD_PLL	PLL digital power supply	Vsupply analog1= 3.3 V
25	DBUS_SEL	Digital Bus Interface select	CMOS Input
26	VDD_DIG	Power supply for digital bus interface	Vsupply digital = 3.3 V
27	SDA/DATA	I^2CBUS /SPI data line	CMOS Bidir Schmitt triggered
28	SCL/CLK	I^2CBUS /SPI clock line	CMOS Input Schmitt triggered
29	LOAD	SPI load line	CMOS Input Schmitt triggered
30	NC	Not connected	-
31	IF_OUTN	IF amplifier negative output	Open collector @ 5 V(1)

Table 2. Pin list (continued)

Pin No	Name	Description	Observation
32	IF_OUTP	IF Amplifier positive output	Open collector @ 5 V(1)
33	VDD_IFAMP	IF Amplifier power supply	Vsupply analog1 = 3.3 V
34	TEST2	Test input 2	Test purpose only; it must be connected to GND
35	TEST1	Test input 1	Test purpose only; it must be connected to GND
36	TEST_ALC	Test output	Test purpose only; it must be connected to GND
37	RF_CT	RF balun central tap	-
38	RF_IN	RF input	-
39	VDD_RFESD	RF ESD positive rail power supply	Vsupply analog1 = 3.3 V
40	MIXDRV_CT	Mixer driver balun central tap	Vsupply analog2 = 5 V(1)
41	VDD_ALC	ALC power supply	Vsupply analog1 = 3.3 V
42	VDD_MIXDRV	Mixer driver power supply	Vsupply analog1 = 3.3 V
43	I_PINDRV1	DAC current output for external PIN Diode attenuator	PMOS Open drain
44	I_PINDRV2	DAC current output for external PIN Diode attenuator	PMOS Open drain

1. Supply voltage @ 3.3 V in low-current mode operation

3 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Values	Unit
AVCC1	Analog Supply voltage	0 to 4.6	V
AVCC2	Analog Supply voltage	0 to 6	V
DVCC	Digital Supply voltage	0 to 4.6	V
Tstg	Storage temperature	+150	°C
ESD (Electro-static discharge)	HBM on pins 16, 17, 31, 32	0.8	kV
	HBM on pin 37, 38, 40	1	
	HBM on all remaining pins	2	
	CDM-JEDEC Standard on pin 38	0.25	
	CDM-JEDEC Standard on all remaining pins	0.5	
	MM on pins 16,17	0.15	
	MM on all remaining pins	0.2	

4 Operating conditions

Table 4. Operating conditions

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
AVCC1	Analog Supply voltage	-	3.15	3.3	3.45	V
AVCC2	Analog Supply voltage	-	4.75	5	5.25	V
DVCC	Digital Supply voltage	-	3.15	3.3	3.45	V
$I_{CC3.3V}$	Current Consumption at 3.3 V	Standard mode	-	130	150	mA
		External VCO standard mode	-	110	130	mA
		Diversity slave mode	-	105	120	mA
		Diversity master mode	-	155	180	mA
		External VCO diversity master mode	-	140	160	mA
I_{CC5V}	Current Consumption	High current mode at 5 V	-	160	185	mA
		Low current mode at 3.3 V	-	95	110	mA
T_A	Operating ambient temperature	-	-40		85	°C
T_J	Maximum junction temperature	-	-		125	°C
Θ_{JA}	Junction to ambient package thermal resistance(1)	Multi-layer JEDEC board	-	33	-	°C/W
Θ_{JB}	Junction to board package thermal resistance(1)	Multi-layer JEDEC board	-	19	-	°C/W
Θ_{JC}	Junction to case package thermal resistance(1)	Multi-layer JEDEC board	-	3	-	°C/W
Ψ_{JB}	Thermal characterization parameter junction to board(1)	Multi-layer JEDEC board	-	18	-	°C/W
Ψ_{JT}	Thermal characterization parameter junction to top case(1)	Multi-layer JEDEC board	-	0.3	-	°C/W

1. Refer to JEDEC standard JESD 51-12 for a detailed description of the thermal resistances and thermal parameters. Data here presented are referring to a Multi-layer board according to JEDEC standard.
$T_J = T_A + \Theta_{JA} * Pdiss$ (in order to estimate T_J if ambient temperature T_A and dissipated power Pdiss are known)
$T_J = T_B + \Psi J_B * Pdiss$ (in order to estimate T_J if board temperature T_B and dissipated power Pdiss are known)
$T_J = T_T + \Psi J_T * Pdiss$ (in order to estimate T_J if top case temperature T_T and dissipated power Pdiss are known)

Table 5. Digital logic levels

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
Vil	Low level input voltage	-	-	-	0.2*Vdd	V
Vih	High level input voltage	-	0.8*Vdd	-	-	V
Vhyst	Schmitt trigger hysteresis	-	0.8	-	-	V
Vol	Low level output voltage	-	-	-	0.4	V
Voh	High level output voltage	-	0.85*Vdd	-	-	V

5 Test conditions

Unless otherwise specified the following test conditions are applied:

- Vsupply digital = 3.3 V
- Vsupply analog1 = 3.3 V
- Vsupply analog2 = 5 V
- F_{IF} = 150 MHz
- MIX = 0111
- T ambient = 27 °C

Refer also to *Section 11: Application information*.

6 Electrical characteristics

*Note: Vsupply digital = 3.3 V, Vsupply analog1 = 3.3 V, Vsupply analog2 = 5 V, F_{RF} = 1700 MHz, F_{LO} = 1550 MHz, T_A = +25*C, RF power = 0 dBm, unless otherwise specified.*

Table 6. Down converter mixer and IF amplifier electrical characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{RF}	RF Frequency	-	1425	-	1910	MHz
F_{LO}	LO Frequency	VCOA divided by 2	1500	-	1800	MHz
		VCOB divided by 2	1900	-	2200	MHz
F_{IF}	IF Center Frequency(2)	F_{IF} = ABS(F_{LO}-F_{RF})	70	-	400	MHz
CG	Power Conversion Gain	Rin = 50 ohm, Rout = 200 ohm RFin = 0 dBm	7.5	8	8.5	dB
$CG_{\Delta T}$	Power Conversion Gain over Temperature(3)	T= -40 to +85 °C	-	±0.6	-	dB
IP_{1dB}	Input P1dB	High current Mode	-	13.5	-	dBm
		Low current Mode	-	8	-	
IIP3	Third-order input intercept point(4)	High current Mode	25	25.5	-	dBm
		Low current Mode	19	19.5	-	
$IIP3_{\Delta T}$	IIP3 variation over temperature(3)	T= -40 to +85 °C	-	±0.5	-	dB
nF_{RF}-nF_{LO}	Spurious rejection at IF(3)	$2F_{RF}$-$2F_{LO}$ F_{RFin} = -5 dBm, F_{IF} = 150 MHz	-	85	-	dBc
		$3F_{RF}$-$3F_{LO}$ F_{RFin} = -5 dBm, F_{IF} = 150 MHz	-	76	-	dBc
NF_{SSB}	Noise figure	High-current mode, MIX = 0011	-	10.5	11	dB
		Low-current mode, MIX = 0011	-	10.5	11	dB
-	LO to IF Leakage	1xLO	-	-35	-	dBm
		2xLO		-34		
-	LO to RF Leakage	-	-	-27	-	dBm
-	RF to IF Isolation	-	-	45	-	dB
RF_{RL}	RF Return Loss	Matched to 50 ohm	-	20	-	dB
IF_{RL}	IF Return Loss	Matched to 200 ohm	-	25	-	dB
-	Gain Flatness for TX observation path(5)	Maximum deviation from F_c over ±10 MHz. For any F_c within each TX observation path band.	-0.05	-	+0.05	dB
		Maximum deviation from F_c over ±30 MHz. For any F_c within each TX observation path band.	-0.10	-	+0.10	dB

Table 6. Down converter mixer and IF amplifier electrical characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
-	Phase Flatness for TX observation path(5)	Maximum deviation from linear phase at F_c over ±10 MHz. For any F_c within each TX observation path band.	-0.3	-	+0.3	deg
		Maximum deviation from linear phase at F_c over ±30 MHz. For any F_c within each TX observation path band.	-0.7	-	+0.7	deg
-	Gain Flatness for RX path(5)	Maximum ripple over a 4 MHz band. For any F_c within each RX path band.	-	-	0.1	dB pk-pk
-	Phase Flatness for RX path(5)	Maximum ripple over a 4 MHz band. For any F_c within each RX path band.	-	-	0.6	deg pk-pk
ICC_{MD}	Mixer Driver Current Consumption	3.3 V Supply (pin 41, 42)	-	48	-	mA
		5 V Supply (pin 40)	-	50	-	mA
	Mixer Driver Current Consumption (Low Current Mode)	3.3 V Supply (pin 41, 42)	-	20	-	mA
		3.3 V Supply (pin 40)	-	35	-	mA
ICC_{IFAM}	IFAMP Current Consumption	3.3 V Supply (pin 33)	-	10	-	mA
		5 V Supply (pin 31, 32)	-	107	-	mA
	IFAMP Current Consumption (Low Current Mode)	3.3 V Supply (pin 33)	-	6	-	mA
		3.3 V Supply (pin 31, 32)	-	55	-	mA

1. All linearity and NF performances are intended at maximum LO amplitude (LO_A[1:0]=[11]), tuning capacitors (CAP[2:0]) programmed according to the selected frequency, mixer bias (MIX[3:0]) set to maximize performance and the device operated in high current mode. The performances of conversion gain, NF and linearity are intended at the SMA connectors of a typical application board.
2. The IF frequency range supported by the IF Amplifier is from 70 to 400 MHz. The exact IF frequency range supported for a specific RF frequency can be calculated as $F_{IF} = ABS(F_{LO}-F_{RF})$ where F_{LO} is inside the specified LO frequency range.
3. Guaranteed by design and characterization
4. RFin = 0 dBm/tone, RF tone spacing = 5 MHz
5. Guaranteed by design

Table 7. Pin diode attenuator driver (dual output current DAC) electrical characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
R	Resolution	-	-	10	-	Bit
DNL	Differential non linearity	-	-0.05	-	0.05	LSB
INL	Integral non linearity	-	-0.45	-	0.45	LSB
I_{FS}	Full Scale current (1)	-	0.28	-	2.8	mA
-	Current Mismatch	-	-	-	2	%
-	Output voltage compliance range	-	0	-	3	V
VR_{EXT_DAC}	Voltage Reference	-	-	1.19		V
R_{EXT_DAC}	REXT DAC Range	-	10	-	100	kΩ
Icc_{static}	Static current consumption	(Iout = 0 mA; pin 1)	-	2.5	-	mA

1. See relationship between IDAC and R_{EXT_DAC} in the Circuit Description section (Dual Output Current DAC)

Table 8. Integer-N synthesizer electrical characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VCO dividers						
N	VCO Divider Ratio (N)	Prescaler 16/17	256	-	65551	-
		Prescaler 19/20	361	-	77836	-
Reference clock and phase frequency detector						
F_{ref}	Reference input frequency	-	10	19.2	200	MHz
-	Reference input sensitivity	-	0.35	1	1.5	Vpeak
R	Reference Divider Ratio	-	2	-	1023	
F_{PFD}	PFD input frequency	-	-	-	16	MHz
F_{STEP}	Frequency step (1)	Prescaler 16/17	F_{LO}/ 65551	-	F_{LO}/ 256	Hz
		Prescaler 19/20	F_{LO}/ 77836	-	F_{LO}/ 361	Hz
Charge pump						
I_{CP}	ICP sink/source (2)	3bit programmable	-	-	5	mA
V_{OCP}	Output voltage compliance range	-	0.4	-	V_{dd}-0.3	V
-	Spurious(3)	-	-	-70	-	dBc
VCOs						
K_{VCOA}	VCOA sensitivity	Higher frequency range	-	100	-	MHz/V
		Intermediate frequency range	-	85	-	MHz/V
		Lower frequency range	-	70	-	MHz/V
K_{VCOB}	VCOB sensitivity	Higher frequency range	-	85	-	MHz/V
		Intermediate frequency range	-	70	-	MHz/V
		Lower frequency range	-	60	-	MHz/V
ΔT_{LKA}	VCOA maximum temperature variation for continuous lock(4)	CALTYPE [0]	-	-	125	°C
		CALTYPE [1]	-	-	125	°C
ΔT_{LKB}	VCOB maximum temperature variation for continuous lock (4))	CALTYPE [0]	-	-	115	°C
		CALTYPE [1]	-	-	125	°C
-	VCO A Pushing	-	-	8	-	MHz/V
	VCO B Pushing	-	-	14	-	MHz/V
V_{CTRL}	VCO control voltage	-	0.4		V_{dd}-0.3	V
-	LO Harmonic Spurious	-	-		-20	dBc
I_{VCO}	VCO and VCO buffer current consumption	Amplitude [11] (pin 4)	-	35	-	mA
I_{DIV2}	DIVIDER by 2 consumption	(pin 3)	-	20	-	mA

Table 8. Integer-N synthesizer electrical characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
2 x LO output buffer (test purpose only)						
F_{OUT}	Frequency range	-	3.0	-	4.4	GHz
P_{OUT}	Output level	-	-	0	-	dBm
RL	Return Loss	Matched to 50ohm	-	10	-	dB
I_{2LOBUF}	Current Consumption	(pin 15, 16, 17)	-	28	-	mA
LO output buffer						
F_{OUT}	Frequency range	-	1.5	-	2.2	GHz
P_{OUT}	Output level	-	-	3	-	dBm
RL	Return Loss	Matched to 50ohm	-	12	-	dB
I_{LOBUF}	Current Consumption	(pin 15, 16, 17)	-	28	-	mA
External VCO (LO) buffer						
f_{INVCO}	Frequency range	-	1.5	-	2.2	GHz
P_{IN}	Input level	-	-	0	-	dBm
I_{EXTBUF}	Current Consumption	External VCO Buffer (pin 4)	-	25	-	mA
PLL miscellaneous						
I_{PLL}	PLL Current Consumption	Input Buffer, Prescaler, Digital Dividers, misc. (pin 24)	-	8	-	mA
I_{PRE}	Prescaler input buffer Current Consumption	(pin 12)	-	3	-	mA
I_{CP}	Charge Pump Current Consumption	CPSEL=[111], REXT_CP = 4.7 kΩ (pin 21)	-	4	-	mA
t_{LOCK}	Lock up time(5)	25 kHz PLL bandwidth; within 1ppm of frequency error	-	150	-	µs

1. The frequency step is related to the PFD input frequency as follows: $F_{STEP}=F_{PFD}/2$)
2. See relationship between ICP and R_{EXT_CP} in the Circuit Description section (Charge Pump)
3. The level of spurs may change depending on PFD frequency, Charge Pump current, selected channel and PLL loop BW.
4. When setting a specified output frequency, the VCO calibration procedure must be run first in order to select the best sub-range for the VCO covering the desired frequency. Once programmed at the initial temperature T_0 inside the operating temperature range (-40 °C to +85 °C), the synthesizer is able to maintain the lock status if the temperature drift (in either direction) is within the limit specified by ΔT_{LK}, provided that the final temperature T_1 is still inside the nominal range.
5. Frequency jump form 1900 to 2050 MHz; it includes the time required by the VCO calibration procedure (7 x F_{PFD} cycles =17.5 µs with F_{PFD} =400 kHz))

Table 9. Phase noise performance(1)

Parameters	Conditions	Min.	Typ.	Max.	Unit
In band phase noise floor, closed loop(2)					
Normalized In Band Phase Noise Floor (LO)	I_{CP}=4 mA, PLL BW = 50 kHz (including reference clock contribution)	-	-230	-	dBc/Hz
In Band Phase Noise Floor (LO)		-230+20log(N)+10log(F_{PFD})			dBc/Hz
PLL integrated phase noise					
Integrated Phase Noise (single sided) 100 Hz to 40 MHz	F_{LO}=2.050 GHz, F_{STEP}=200 kHz, I_{CP}=3 mA, PLL BW = 25 kHz	-	-45.3	-	dBc
		-	0.44	-	° rms
LOA (1500 MHz to 1800 MHz) – open loop					
Phase Noise @ 1 kHz	-	-	-69	-	dBc/Hz
Phase Noise @ 10 kHz	-	-	-96	-	dBc/Hz
Phase Noise @ 100 kHz	-	-	-118	-	dBc/Hz
Phase Noise @ 1 MHz	-	-	-139	-	dBc/Hz
Phase Noise @ 10 MHz	-	-	-153	-	dBc/Hz
Phase Noise Floor @ 40 MHz	-	-	-156	-	dBc/Hz
LOB (1900 MHz to 2200 MHz) – open loop					
Phase Noise @ 1 kHz	-	-	-64	-	dBc/Hz
Phase Noise @ 10 kHz	-	-	-91	-	dBc/Hz
Phase Noise @ 100 kHz	-	-	-115	-	dBc/Hz
Phase Noise @ 1 MHz	-	-	-136	-	dBc/Hz
Phase Noise @ 10 MHz	-	-	-152	-	dBc/Hz
Phase Noise Floor @ 40 MHz	-	-	-156	-	dBc/Hz

1. Phase Noise SSB. VCO amplitude set to maximum value [11]. All the closed-loop performances are specified using a Reference Clock signal at 76.8 MHz with phase noise of -144 dBc/Hz @1 kHz offset, -157 dBc/Hz @10 kHz offset and -168 dBc/Hz of noise floor.
2. Normalized PN = Measured LO PN – 20log(N) – 10log(F_{PFD}) where N is the VCO divider ratio (N=B*P+A) and F_{PFD} is the comparison frequency at the PFD input

7 Typical performance characteristics

Note: Vsupply digital = 3.3 V, Vsupply analog1 = 3.3 V, Vsupply analog2 = 5 V, F_{IF} = 150 MHz, T_A = +25 °C, RF power = 0 dBm, unless otherwise specified.

Figure 3. Conversion gain against RF frequency

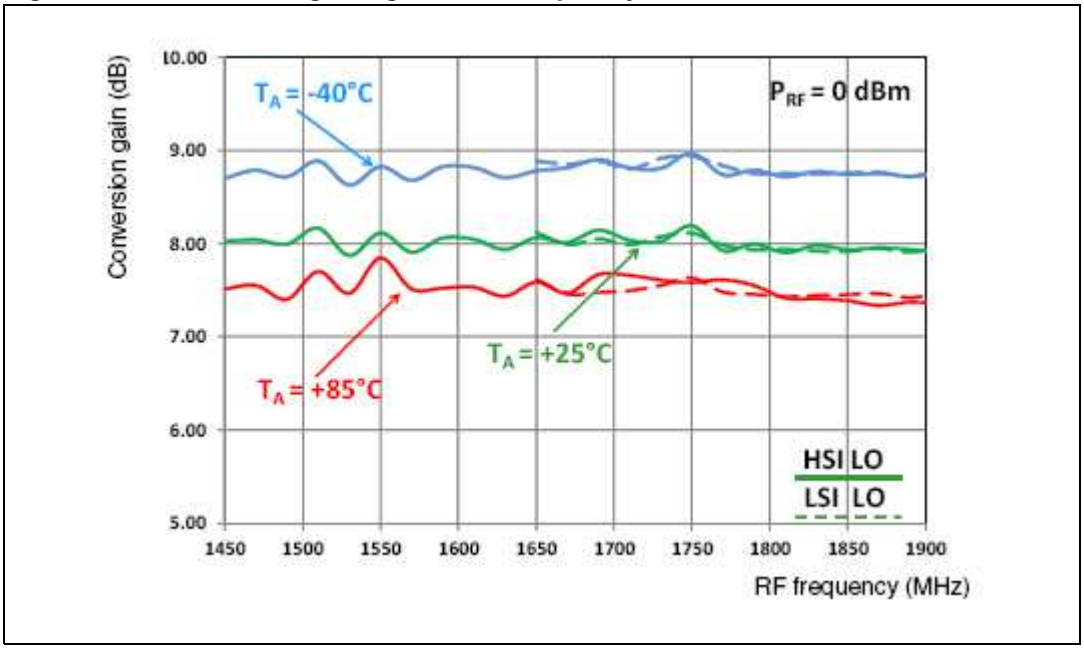


Figure 4. Noise figure against RF frequency

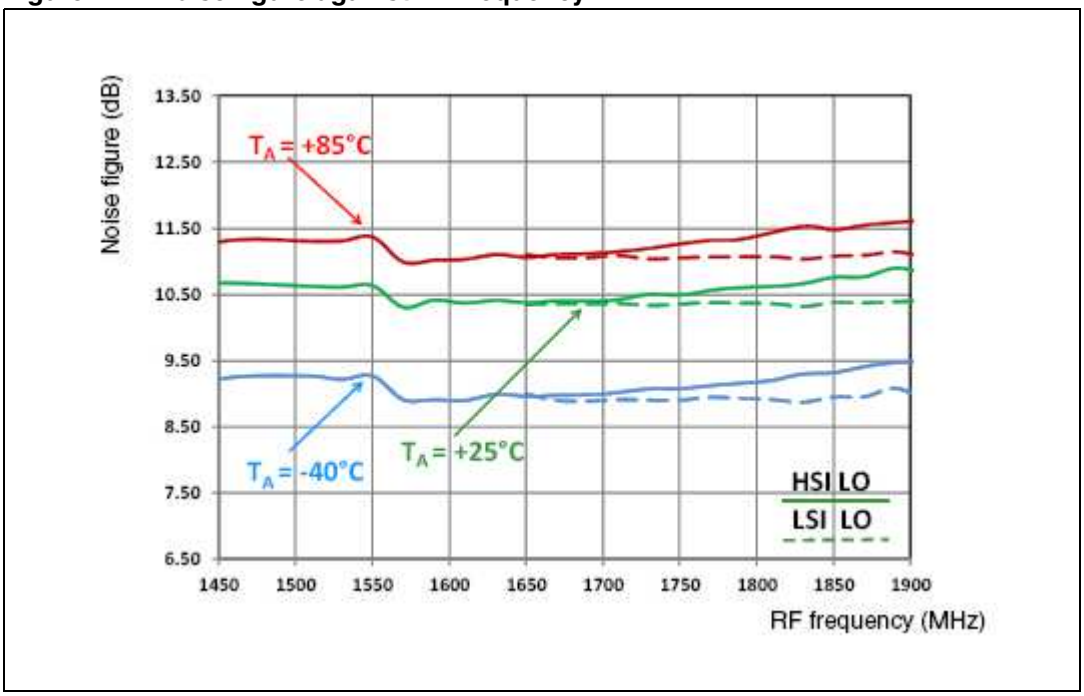


Figure 5. IIP3 against RF frequency

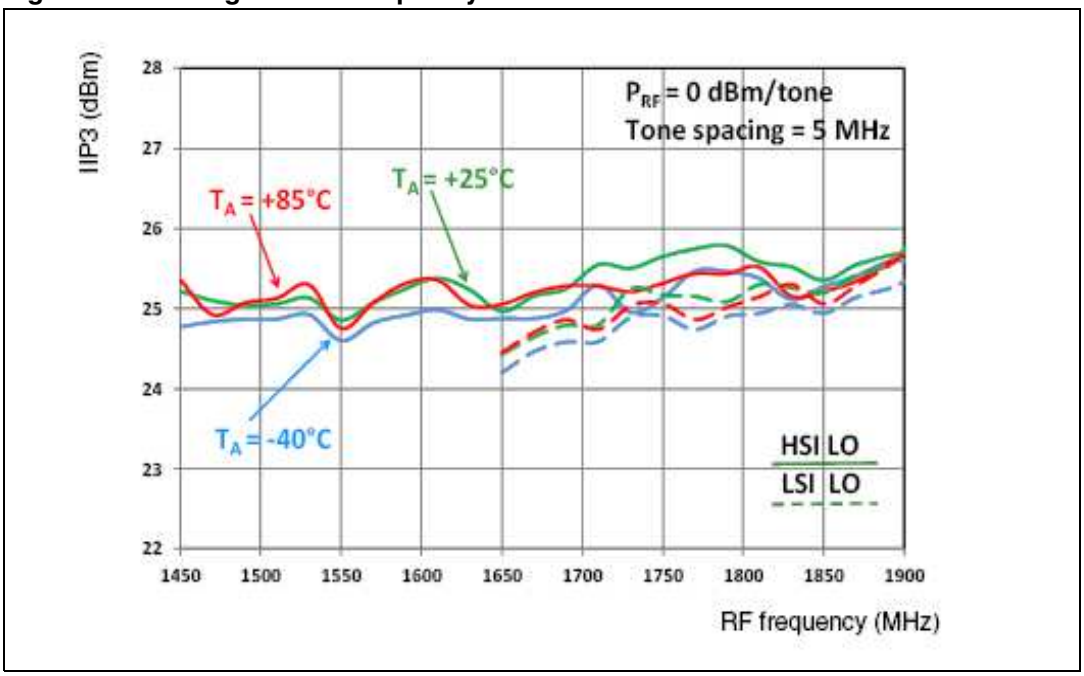


Figure 6. 2RF-2LO response against RF frequency

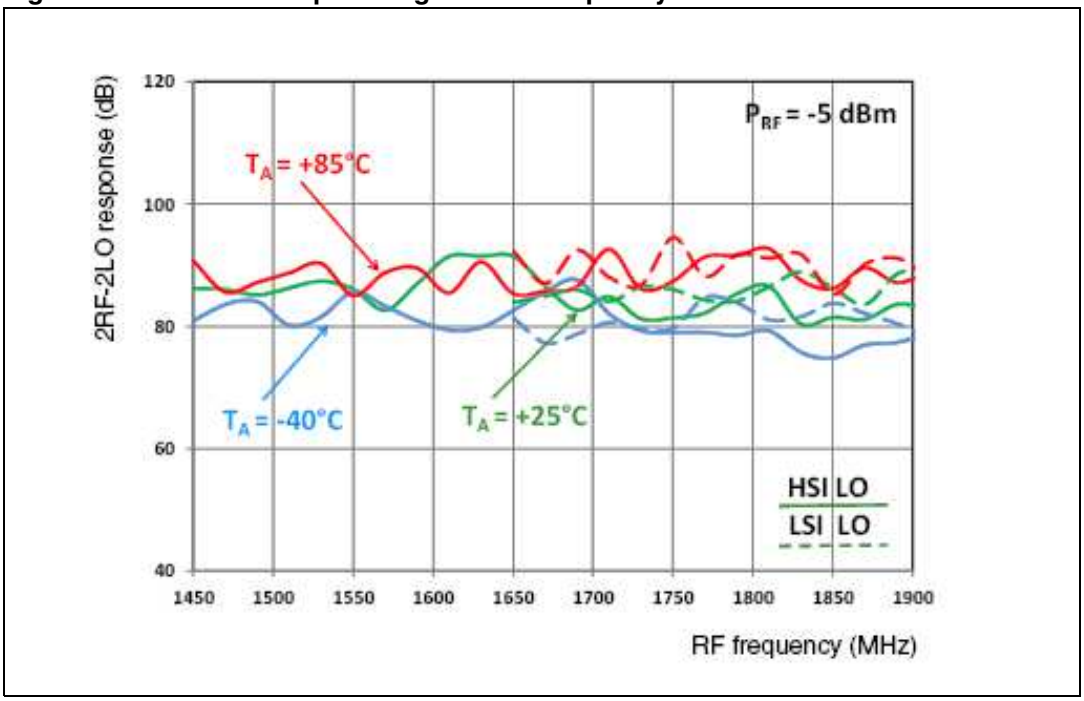


Figure 7. LOA (VCOA div. by 2) closed-loop phase noise at 1.65 GHz (F_{STEP} = 200 kHz, I_{CP} = 3 mA)

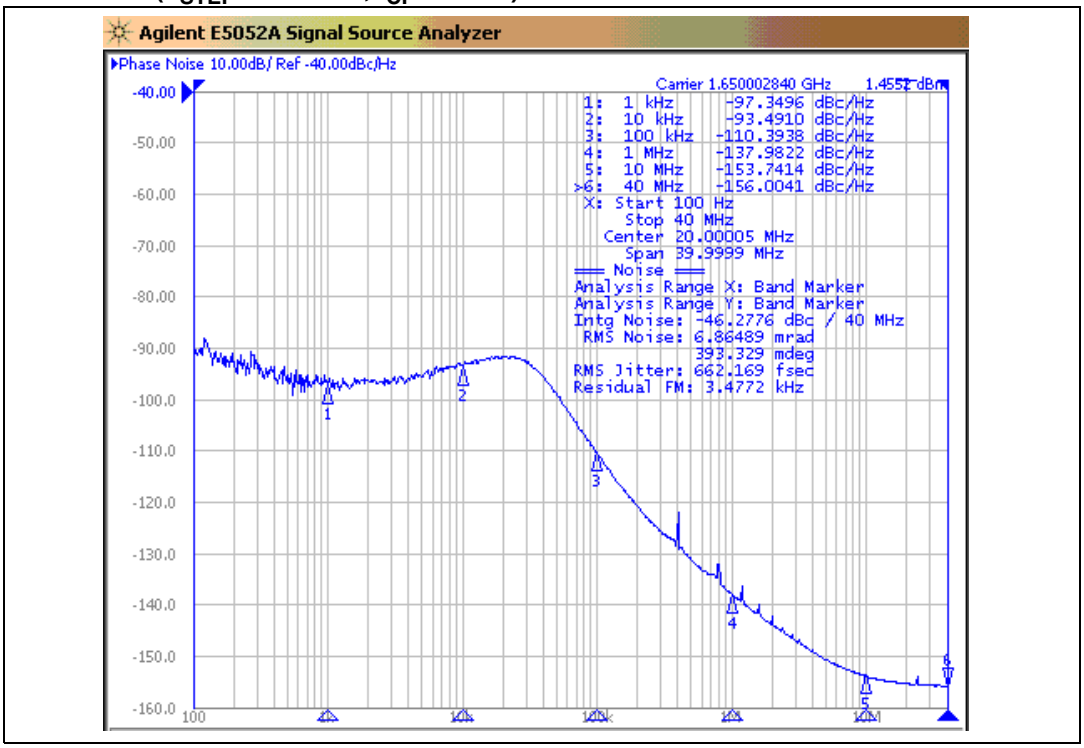
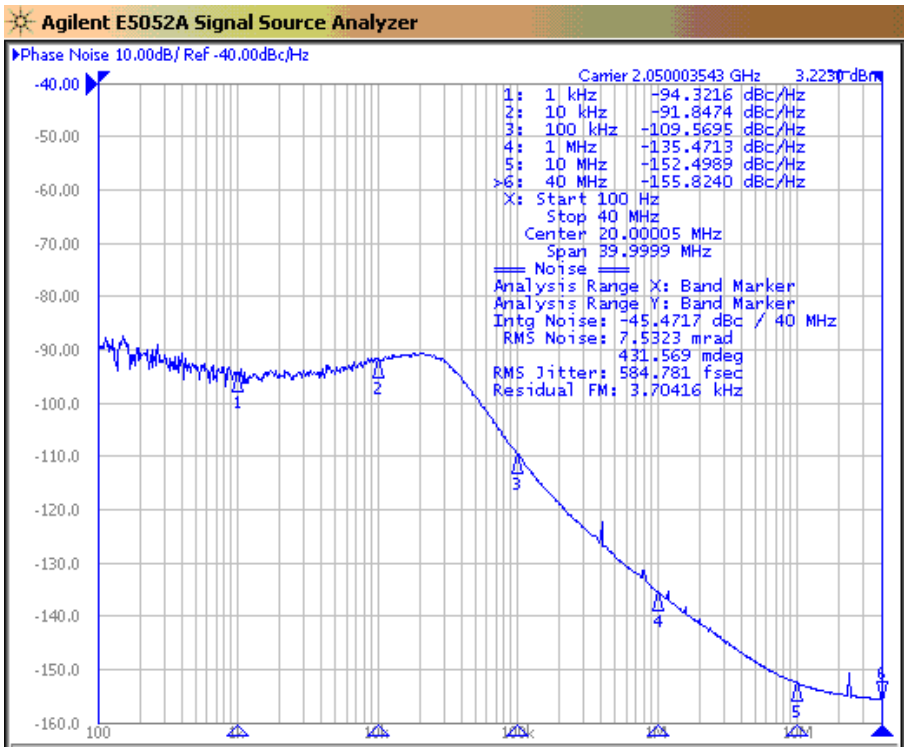


Figure 8. LOB (VCOB div. by 2) closed-loop phase noise at 2.05 GHz (F_{STEP} = 200 kHz, I_{CP} = 3 mA)



8 General description

The STW82102B (see *Figure 1: STW82102B block diagram on page 7*) consists of a high linearity passive CMOS mixer with integrated RF balun, an IF amplifier, a 10-bit current steering DAC with dual output, and an integrated integer-N synthesizer.

The synthesizer embeds 2 internal low-noise VCOs with buffer blocks, a divider by 2, a low noise PFD (Phase Frequency Detector), a precise charge pump, a 10-bit programmable reference divider, two programmable counters and a dual-modulus prescaler. The A-counter (5 bits) and B counter (12 bits) counters, in conjunction with the dual modulus prescaler P/P+1 (16/17 or 19/20), implement an N integer divider, where N = B*P+A.

The device is controlled through a digital interface (*I2C bus interface* or *SPI digital interface*).

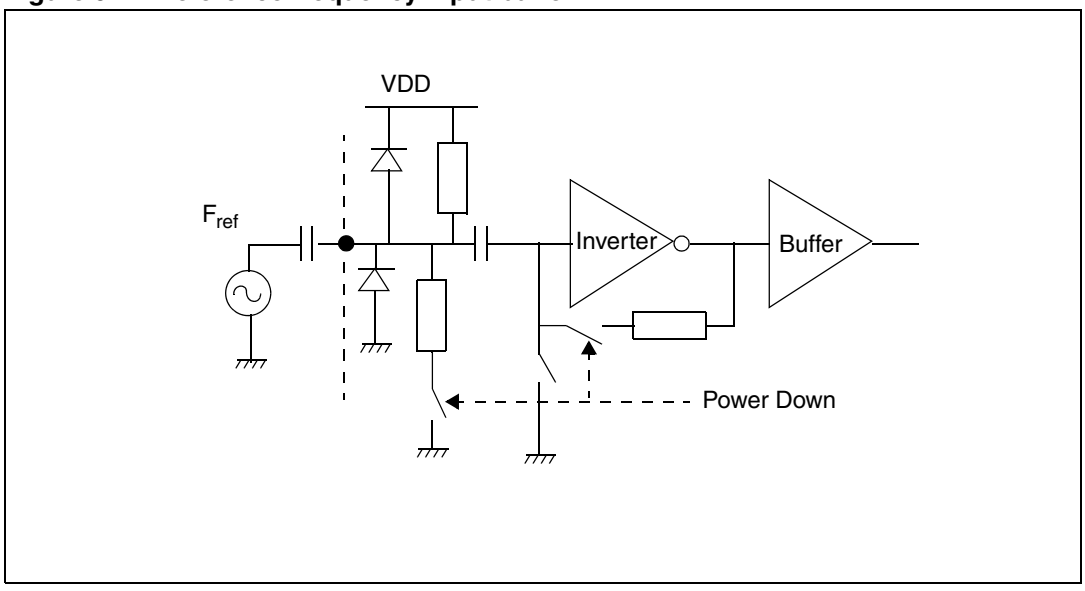
All internal devices operate with a power supply of 3.3 V except for the IF Amplifier output stage and the mixer driver stage operating at 5 V power supply in order to maximize the linearity performance. If the application requires a reduced linearity and noise figure performance the device is programmed in a low-current mode by using the minimum LO amplitude and the minimum biasing current in the IF amplifier. In low-current mode operation the device can use only the 3.3 V power supply thus dissipating less power.

8.1 Circuit description

8.1.1 Reference input stage

The reference input stage is shown in *Figure 9*. The resistor network feeds a DC bias at the F_{ref} input while the inverter used as the frequency reference buffer is AC coupled.

Figure 9. Reference frequency input buffer



8.1.2 Reference divider

The 10-bit programmable reference counter allows the input reference frequency to be divided to produce the input clock to the PFD. The division ratio is programmed through the digital interface.

8.1.3 Prescaler

The dual-modulus prescaler P/P+1 takes the CML clock from the VCO buffer and divides it down to a manageable frequency for the CMOS A and B counters. The modulus (P) is programmable and can be set to 16 or 19. It is based on a synchronous 4/5 core which division ratio depends on the state of the modulus input.

8.1.4 A and B counters

The A (5 bits) and B (12 bits) counters, in conjunction with the selected dual modulus (16/17 or 19/20) prescaler make it possible to generate output frequencies which are spaced only by the reference frequency divided by the reference division ratio. Thus, the division ratio and the VCO output frequency are given by the following formulae:

$$N = B \times P + A$$

$$F_{VCO} = \frac{(B \times P + A) \times F_{ref}}{R}$$

where:

F_{VCO}: VCO output frequency.

P: modulus of dual modulus prescaler (16 or 19 selected through the digital interface).

B: division ratio of the main counter.

A: division ratio of the swallow counter.

F_{ref}: input reference frequency.

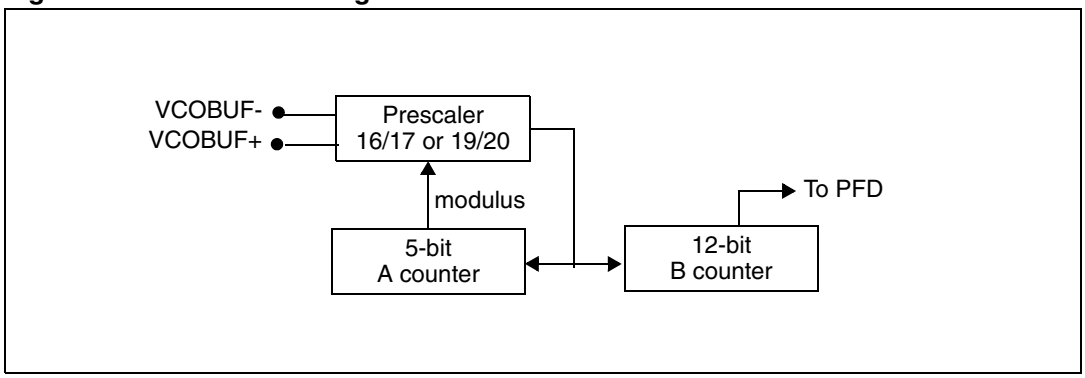
R: division ratio of the reference counter.

N: division ratio of the PLL

The following points should be noted:

- For the VCO divider to work correctly, B **must** be higher than A.
- A can take any value from 0 to 31.
- Two PLL division ratio (N) ranges are possible, depending on the value of P:
  - 256 to 65551 (when P=16)
  - 361 to 77836 (when P=19).

Figure 10. VCO divider diagram



8.1.5 Phase frequency detector (PFD)

The PFD takes inputs from the reference and the VCO dividers and produces an output proportional to the phase error. The PFD includes a delay gate that controls the width of the anti-backlash pulse. This pulse ensures that there is no dead zone in the PFD transfer function.

Figure 11 is a simplified schematic of the PFD.

Figure 11. PFD diagram