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N-channel 600 V, 0.065 Ω typ., 40 A MDmesh™ DM2 Power MOSFET in a TO-247 long leads package

Datasheet - production data

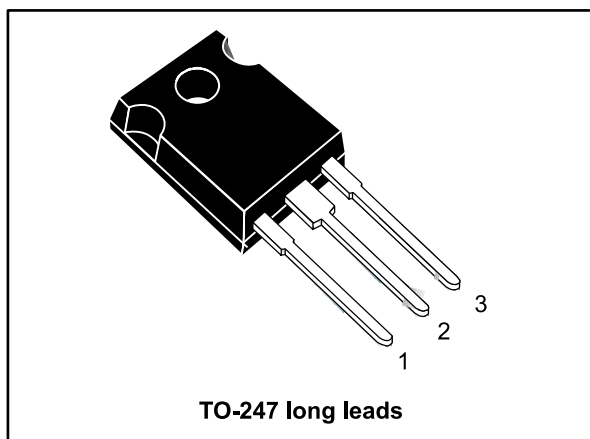
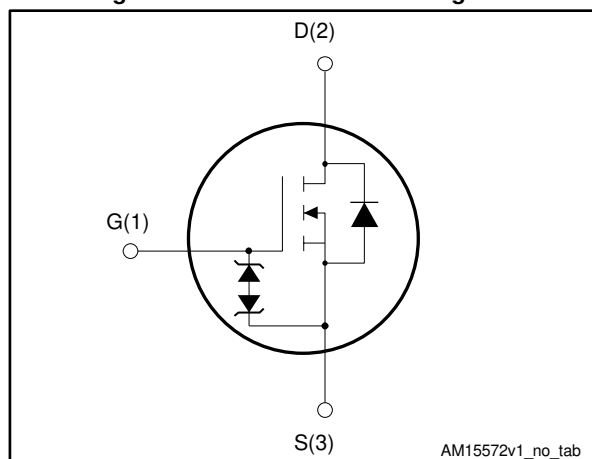


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D
STWA48N60DM2	600 V	0.079 Ω	40 A

- Fast-recovery body diode
- Extremely low gate charge and input capacitance
- Low on-resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Zener-protected

Applications

- Switching applications

Description

This high voltage N-channel Power MOSFET is part of the MDmesh™ DM2 fast recovery diode series. It offers very low recovery charge (Q_{rr}) and time (t_{rr}) combined with low $R_{DS(on)}$, rendering it suitable for the most demanding high efficiency converters and ideal for bridge topologies and ZVS phase-shift converters.

Table 1: Device summary

Order code	Marking	Package	Packing
STWA48N60DM2	48N60DM2	TO-247 long leads	Tube

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at $T_{case} = 25\text{ }^\circ\text{C}$	40	A
	Drain current (continuous) at $T_{case} = 100\text{ }^\circ\text{C}$	25	
$I_{DM}^{(1)}$	Drain current (pulsed)	160	A
P_{TOT}	Total dissipation at $T_{case} = 25\text{ }^\circ\text{C}$	300	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	50	V/ns
$dv/dt^{(3)}$	MOSFET dv/dt ruggedness		
T_{stg}	Storage temperature range	-55 to 150	$^\circ\text{C}$
T_j	Operating junction temperature range		

Notes:

(1) Pulse width is limited by safe operating area

(2) $I_{SD} \leq 40\text{ A}$, $di/dt=900\text{ A}/\mu\text{s}$; $V_{DS\text{ peak}} < V_{(BR)DSS}$, $V_{DD} = 400\text{ V}$

(3) $V_{DS} \leq 480\text{ V}$

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	0.42	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient	50	

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (Pulse width limited by T_{jmax})	7	A
E_{AR}	Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	950	mJ

2 Electrical characteristics

($T_{\text{case}} = 25\text{ °C}$ unless otherwise specified)

Table 5: Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(\text{BR})\text{DSS}}$	Drain-source breakdown voltage	$V_{\text{GS}} = 0\text{ V}$, $I_{\text{D}} = 1\text{ mA}$	600			V
I_{DSS}	Zero gate voltage drain current	$V_{\text{GS}} = 0\text{ V}$, $V_{\text{DS}} = 600\text{ V}$			1	μA
		$V_{\text{GS}} = 0\text{ V}$, $V_{\text{DS}} = 600\text{ V}$, $T_{\text{case}} = 125\text{ °C}^{(1)}$			100	
I_{GSS}	Gate-body leakage current	$V_{\text{DS}} = 0\text{ V}$, $V_{\text{GS}} = \pm 25\text{ V}$			± 5	μA
$V_{\text{GS(th)}}$	Gate threshold voltage	$V_{\text{DS}} = V_{\text{GS}}$, $I_{\text{D}} = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{\text{DS(on)}}$	Static drain-source on-resistance	$V_{\text{GS}} = 10\text{ V}$, $I_{\text{D}} = 20\text{ A}$		0.065	0.079	Ω

Notes:

⁽¹⁾Defined by design, not subject to production test

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{\text{DS}} = 100\text{ V}$, $f = 1\text{ MHz}$, $I_{\text{D}} = 0\text{ A}$	-	3250	-	μF
C_{oss}	Output capacitance		-	142	-	
C_{rss}	Reverse transfer capacitance		-	4.5	-	
$C_{\text{oss eq.}}^{(1)}$	Equivalent output capacitance	$V_{\text{DS}} = 0\text{ to }480\text{ V}$, $V_{\text{GS}} = 0\text{ V}$	-	258	-	μF
R_{G}	Intrinsic gate resistance	$f = 1\text{ MHz}$, $I_{\text{D}} = 0\text{ A}$	-	4	-	Ω
Q_{g}	Total gate charge	$V_{\text{DD}} = 480\text{ V}$, $I_{\text{D}} = 40\text{ A}$, $V_{\text{GS}} = 10\text{ V}$ (see Figure 14: "Test circuit for gate charge behavior")	-	70	-	nC
Q_{gs}	Gate-source charge		-	18	-	
Q_{gd}	Gate-drain charge		-	28	-	

Notes:

⁽¹⁾ $C_{\text{oss eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$, $I_D = 20\text{ A}$ $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 13 : "Test circuit for resistive load switching times" and Figure 18 : "Switching time waveform")	-	27	-	ns
t_r	Rise time		-	27	-	
$t_{d(off)}$	Turn-off delay time		-	131	-	
t_f	Fall time		-	9.8	-	

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}^{(1)}$	Source-drain current		-		40	A
$I_{SDM}^{(2)}$	Source-drain current (pulsed)		-		160	A
$V_{SD}^{(3)}$	Forward on voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 40\text{ A}$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 40\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$ (see Figure 15 : "Test circuit for inductive load switching and diode recovery times")	-	140		ns
Q_{rr}	Reverse recovery charge		-	0.7		μC
I_{RRM}	Reverse recovery current		-	10		A
t_{rr}	Reverse recovery time	$I_{SD} = 40\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 15 : "Test circuit for inductive load switching and diode recovery times")	-	256		ns
Q_{rr}	Reverse recovery charge		-	2.5		μC
I_{RRM}	Reverse recovery current		-	20		A

Notes:

- (1) Limited by maximum junction temperature
(2) Pulse width is limited by safe operating area.
(3) Pulse test: pulse duration = 300 μs , duty cycle 1.5%.

Table 9: Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 250\ \mu\text{A}$, $I_D = 0\text{ A}$	± 30	-	-	V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

2.1 Electrical characteristics (curves)

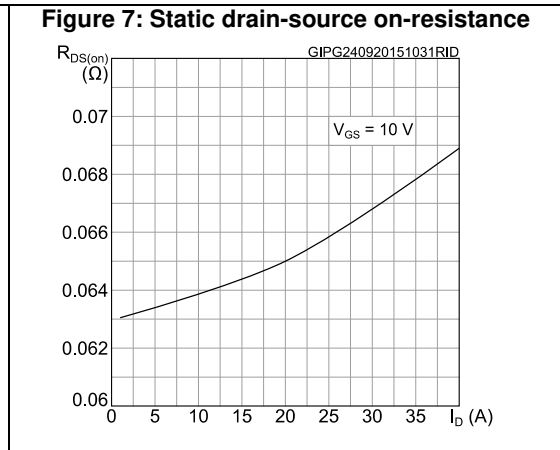
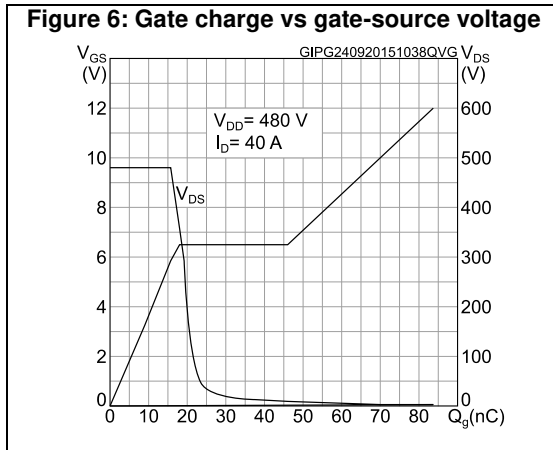
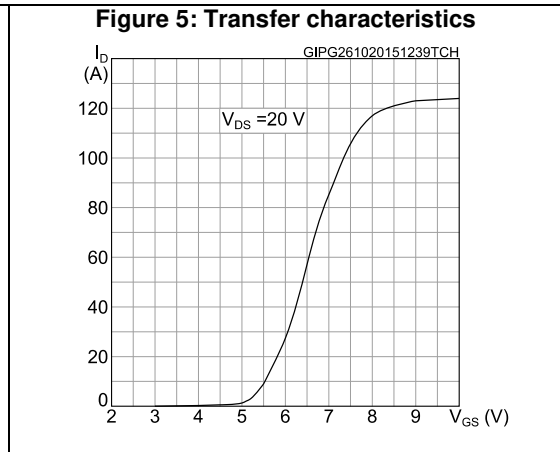
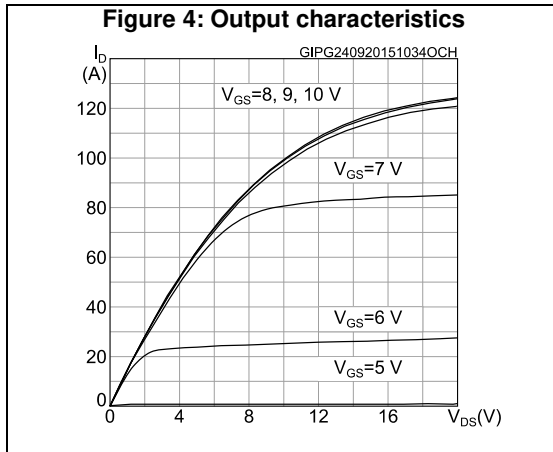
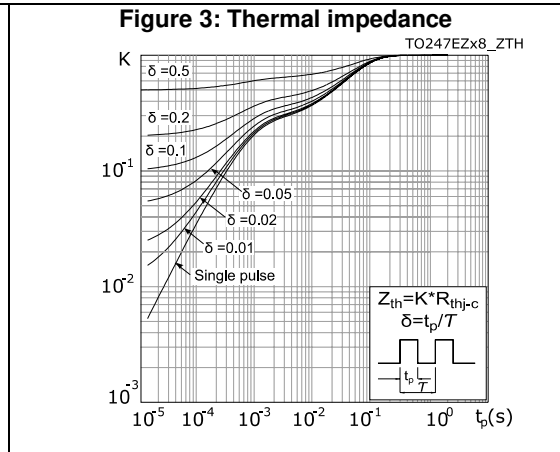
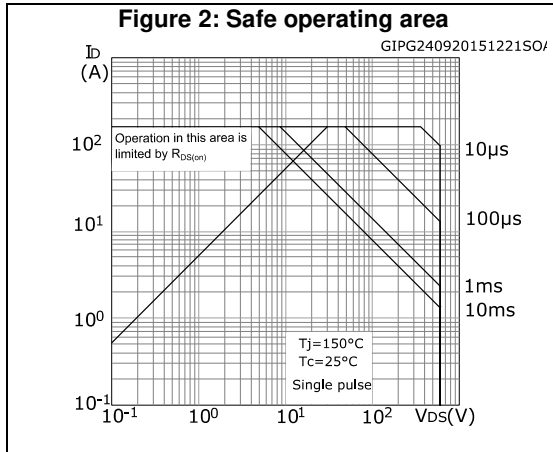


Figure 8: Capacitance variations

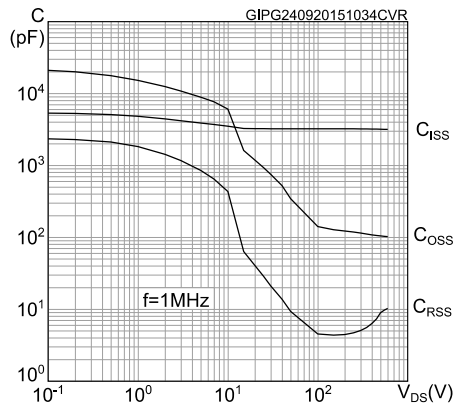


Figure 9: Normalized gate threshold voltage vs temperature

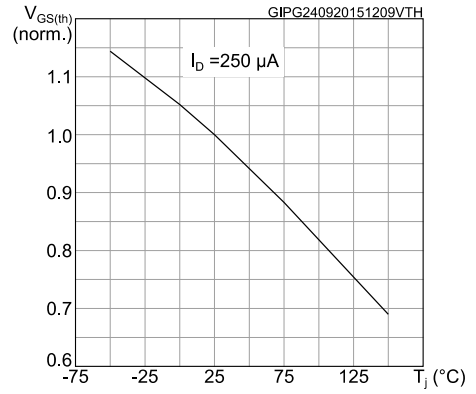


Figure 10: Normalized on-resistance vs temperature

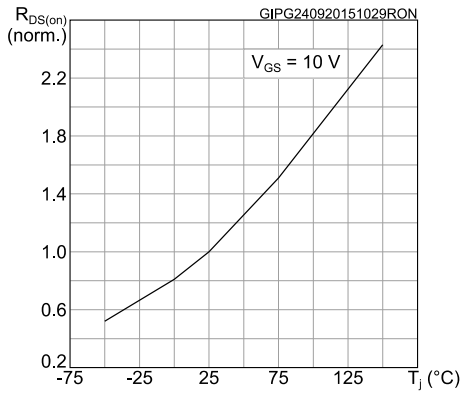


Figure 11: Normalized V_(BR)DSS vs temperature

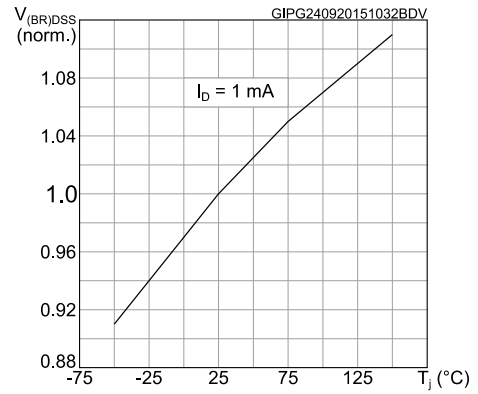
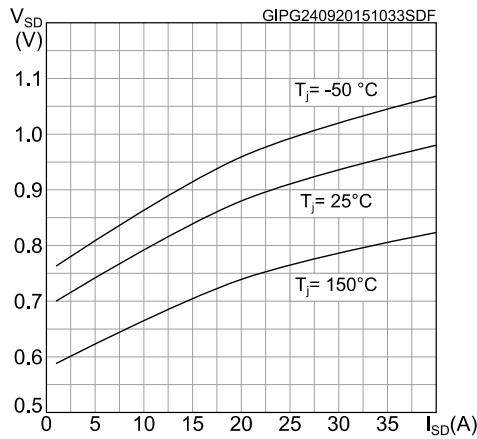


Figure 12: Source- drain diode forward characteristics



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 TO-247 long leads package information

Figure 19: TO-247 long leads package outline

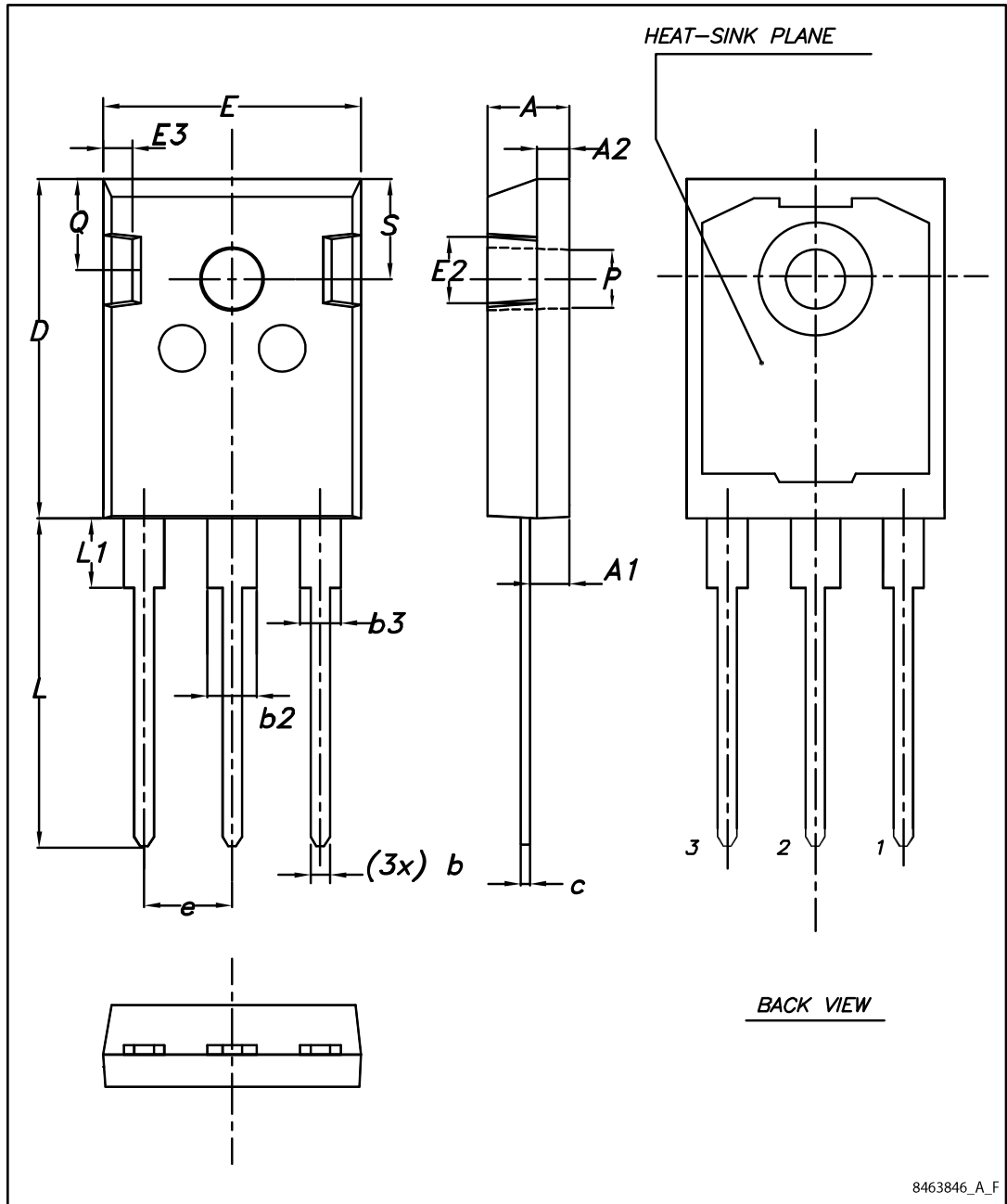


Table 10: TO-247 long leads package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.90	5.00	5.10
A1	2.31	2.41	2.51
A2	1.90	2.00	2.10
b	1.16		1.26
b2			3.25
b3			2.25
c	0.59		0.66
D	20.90	21.00	21.10
E	15.70	15.80	15.90
E2	4.90	5.00	5.10
E3	2.40	2.50	2.60
e	5.34	5.44	5.54
L	19.80	19.92	20.10
L1			4.30
P	3.50	3.60	3.70
Q	5.60		6.00
S	6.05	6.15	6.25

5 Revision history

Table 11: Document revision history

Date	Revision	Changes
20-Dec-2016	1	First release

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