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Digital controller for wireless battery charger transmitters for wearable and smartwatch applications

Datasheet - production data

VFQFPN32

Features

- Digital controller for wireless battery charger transmitters
- Optimized for < 3 W applications
  - Smartwatches and healthcare
  - Internet of Things (IoT) battery-powered smart devices
  - Remote controllers
- Cost effective half-bridge topology with integrated drivers
- Optional full-bridge configuration for 3 W applications
- V_{IN} range: 3 V to 5.5 V
  - Supports USB V_{IN}
- Active presence detector
- Parametric customization via graphical interface
- 2 firmware options:
  - Turnkey solution for quick design
  - APIs available for application customization
- Peripherals available via APIs
  - ADC, with 10-bit precision
  - UART
  - I^2C master fast/slow speed rate
  - GPIOs
- Memory
  - Flash and EEPROM with read-while-write (RWW) and Error Correction Code (ECC)
  - Program memory: 32 Kbytes Flash; data retention:15 years at 85 °C after 10 kcycles at 25 °C
  - Data memory: 1 Kbyte true data EEPROM; data retention: 15 years at 85 °C after 100 kcycles at 85 °C
  - RAM: 6 Kbytes
- Transmitter reference design:
  - Evaluation board order code: STEVAL-ISB038V1T
  - 2-layer PCBs
  - Active object detection
  - Graphical user interface for application monitoring
  - Interoperable with receiver: STEVAL-ISB038V1R
- Operating temperature
  - -40 °C up to 105 °C
- Package
  - VFQFPN32

Table 1. Ordering information

Order code	Type
STWBC-WA	Controller (tube)
STWBC-WATR	Controller (tape and reel)
STEVAL-ISB038V1T	Transmitter evaluation board
STEVAL-ISB038V1R	Receiver evaluation board
STEVAL-ISB038V1	Transmitter and receiver evaluation kit

Contents

1 Description

The STWBC-WA is STMicroelectronics' wireless battery charger transmitter application optimized for wearable usage.

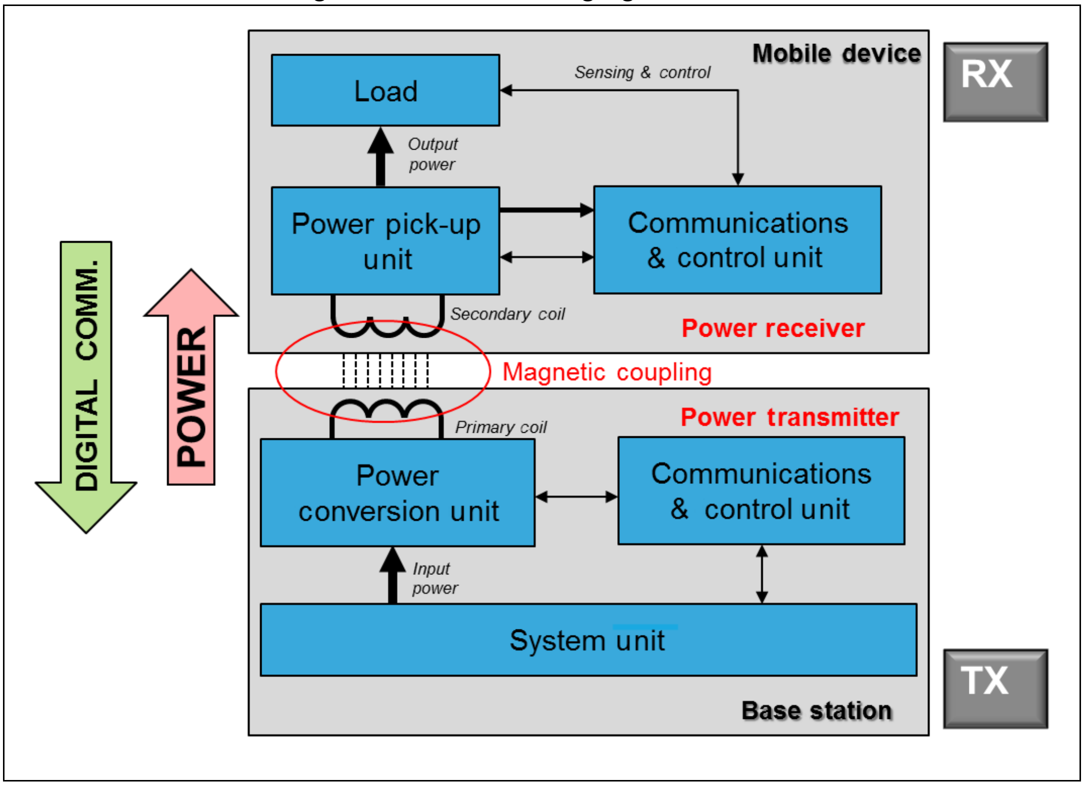
Thanks to its 5 V native supply, the STWBC-WA device is ideal to operate with USB power supplies.

Wireless battery charging systems replace the traditional power supply cable by means of electromagnetic induction between a transmitting pad or dongle (TX) and a battery-powered unit (RX), such as a smartwatch or sports gear.

The power transmitter unit is responsible for controlling the transmitting coil and generating the correct amount of power requested by the receiver unit. The receiver unit continuously provides the transmitter the correct power level requested, by modulating the transmitter carrier through controlled resistive or capacitive insertion. Generating the correct amount of power guarantees the highest level of end-to-end efficiency due to reduced energy waste. It also helps to maintain a lower operational temperature.

The digital wireless battery transmitter can adapt to the amount of energy transferred by the coil by modulating the frequency, duty cycles or coil input voltage.

Figure 1. Wireless charging architecture



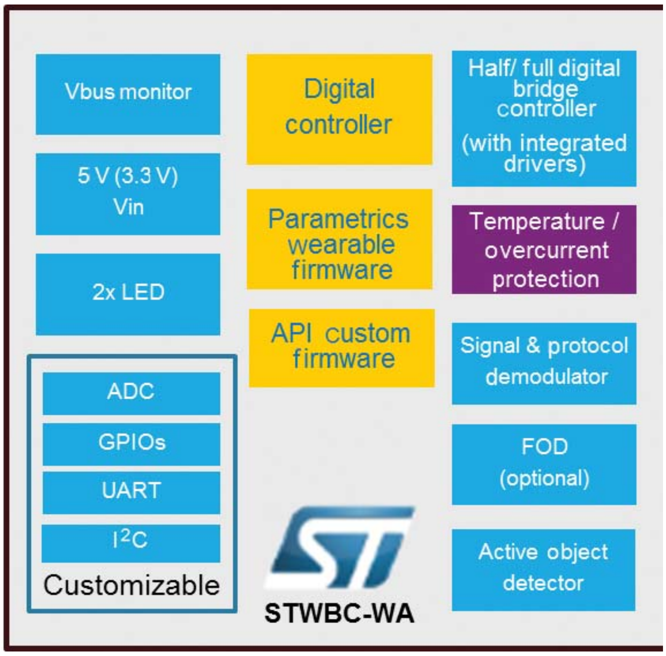
The STWBC-WA firmware sits on the top of the hardware to monitor and control the correct wireless charging operations.

2 STWBC-WA system architecture

Figure 2 illustrates the overall system blocks implemented in the STWBC-WA architecture.

The STWBC-WA is a flexible controller which can be configured to support both half-bridge topologies for < 1 W power levels as well as full-bridge systems for driving < 3 W wearable devices. The integrated drivers require no external components between the STWBC-WA and the power MOSFETs application.

Figure 2. STWBC-WA device architecture



Firmware

The STWBC-WA firmware is available in two separate software packages:

- Turnkey: the firmware is distributed as a binary file.
- API customizable: the firmware is designed as a library, and external functions as well as peripherals can be added by means of APIs.

The STWBC-WA provides a set of APIs which allows the user to customize the application and tailor the system architecture to his needs. The UART and I^{2}C communication interfaces, ADC and GPIOs can be controlled by the custom firmware via convenient APIs.

The software APIs allow a great deal of freedom to customize applications. The STWBC-WA device and the API library can be accessed by programming the internal controller via standard programming tools such as the IAR™ Workbench® Studio.

3 STWBC-WA pinout and pin description

This section illustrates the pinout used by the STWBC-WA device.

Figure 3. STWBC-WA pin configuration

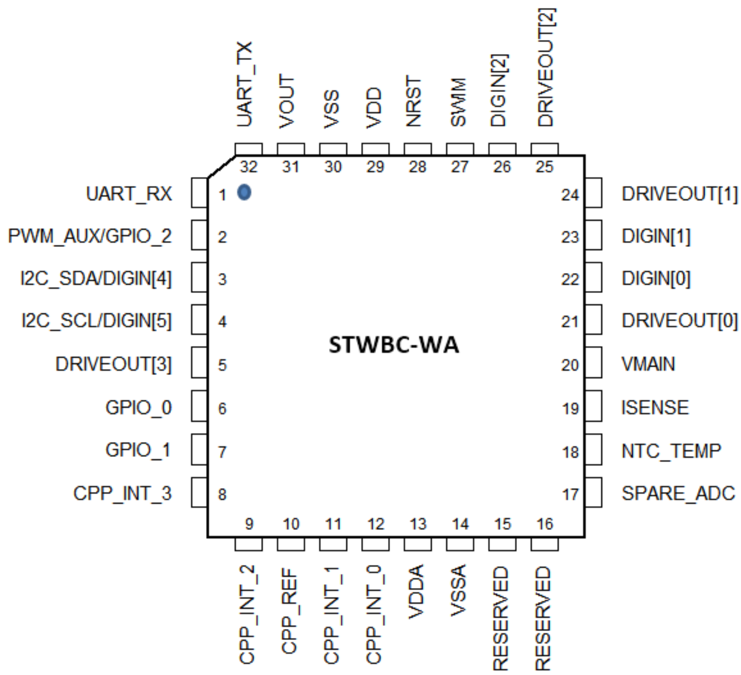


Table 2. Pinout description

Pin number	Pin name	Pin type	Turnkey firmware description
1	UART_RX(1)	DI	UART RX link
2	PWM_AUX/GPIO_2(1)	DO	Not used, must not be connected to any potential
3	I2C_SDA/DIGIN[4](1)	-	Inactive (internal pull-up)
4	I2C_SCL/DIGIN[5](1)	-	Inactive (internal pull-up)
5	DRIVEOUT[3](1)	DO	Output driver for full-bridge configuration (optional)
6	GPIO_0(1)	DO	Digital output for the green light indicator
7	GPIO_1(1)	DO	Digital output for the red light indicator
8	CPP_INT_3	AI	Connected to GND
9	CPP_INT_2	AI	Connected to GND
10	CPP_REF	AI	External reference for CPP_INT_3 (if not used, must be tied to GND)
11	CPP_INT_1	AI	Connected to GND
12	CPP_INT_0	AI	WAVE_SNS signal for symbol detection
13	VDDA	PS	Analog power supply

Table 2. Pinout description (continued)

Pin number	Pin name	Pin type	Turnkey firmware description
14	VSSA	PS	Analog ground
15	RESERVED	AI	Reserved
16	RESERVED	-	Reserved
17	SPARE_ADC(1)	-	Connected to the USB_ID signal
18	NTC_TEMP	AI	NTC temperature measurement
19	ISENSE	AI	LC tank current measurement
20	VMAIN	AI	Vmain monitor
21	DRIVEOUT[0]	DO	Output driver for the low-side branch
22	DIGIN[0](1)	-	Inactive (internal pull-up)
23	DIGIN[1](1)	-	Inactive (internal pull-up)
24	DRIVEOUT[1]	DO	Output driver for the high-side branch
25	DRIVEOUT[2]	DO	Output driver for full-bridge configuration (optional)
26	DIGIN[2](1)	-	Not connected
27	SWIM	DIO	Debug interface
28	NRST	DI	Reset
29	VDD	PS	Digital and I/O power supply
30	VSS	PS	Digital and I/O ground
31	VOUT	Supply	Internal LDO output
32	UART_TX(1)	DO	UART TX link

1. API configurable.

Note: All analog inputs are VDD compliant but can be used only between 0 and 1.2 V.

4 Electrical characteristics

4.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS}. V_{DDA} and V_{DD} must be connected to the same voltage value. V_{SS} and V_{SSA} must be connected together with the shortest wire loop.

4.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of the ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and $T_A = T_A$ max. (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in *Table 3*, *Table 4* and in the footnotes of *Table 6 on page 12* to *Table 18 on page 24*, and are not tested in production.

4.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} and V_{DDA} = 3.3 V. They are given only as design guidelines and are not tested. Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range.

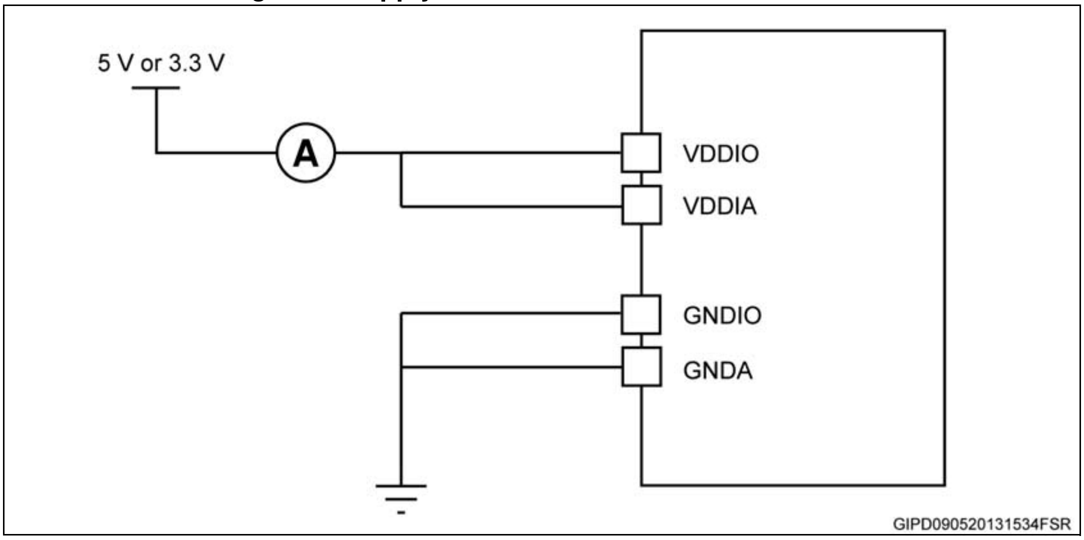
4.1.3 Typical curves

Unless otherwise specified, all typical curves are given as design guidelines only and are not tested.

4.1.4 Typical current consumption

For typical current consumption measurements, V_{DD} and V_{DDA} are connected together as shown in *Figure 4*.

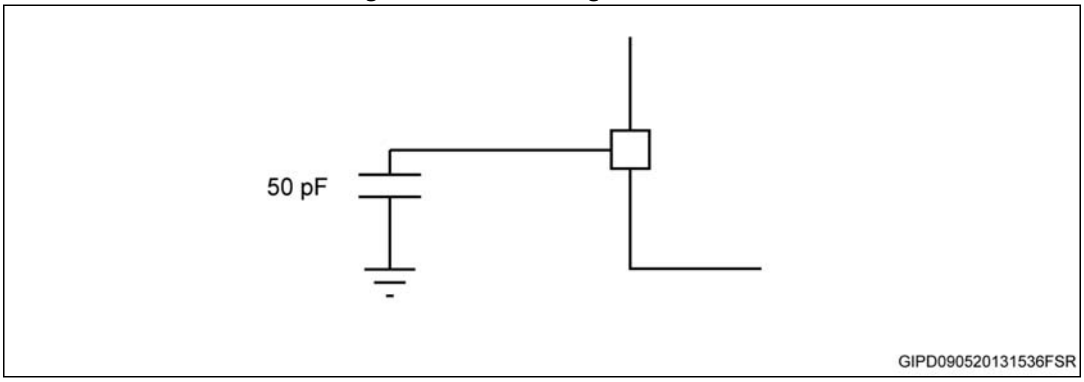
Figure 4. Supply current measurement conditions



4.1.5 Loading capacitors

The loading conditions used for the pin parameter measurement are shown in *Figure 5*:

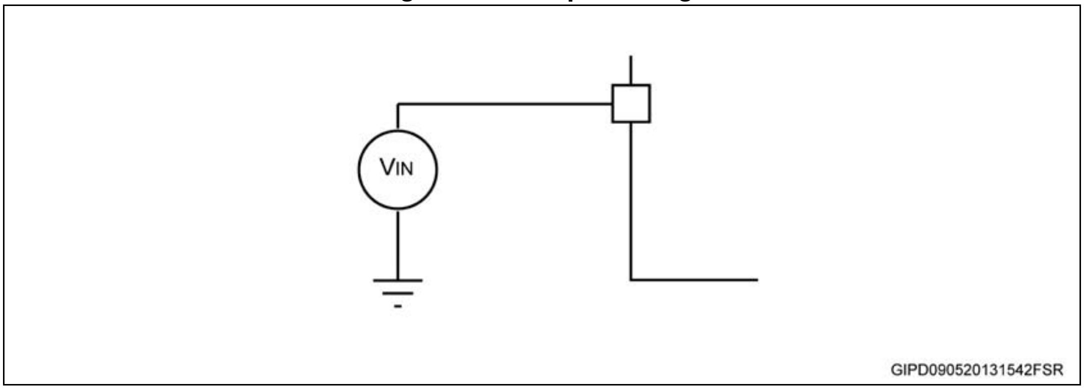
Figure 5. Pin loading conditions



4.1.6 Pin output voltage

The input voltage measurement on a pin is described in *Figure 6*.

Figure 6. Pin input voltage



4.2 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and the functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 3. Voltage characteristics

Symbol	Ratings	Min.	Max.	Unit
V_{DDX} - V_{SSX}	Supply voltage(1)	-0.3	6.5	V
V_{IN}	Input voltage on any other pin(2)	VSS -0.3	VDD +0.3	
V_{DD} - V_{DDA}	Variation between different power pins	-	50	mV
V_{SS} - V_{SSA}	Variation between all the different ground pins(3)	-	50	
V_{ESD}	Electrostatic discharge voltage	Refer to absolute maximum ratings (electrical sensitivity) in *Section 4.4.1 on page 26*.		

1. All power V_{DDX} (V_{DD}, V_{DDA}) and ground V_{SSX} (V_{SS}, V_{SSA}) pins must always be connected to the external power supply.
2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$.
3. V_{SS} and V_{SSA} signals must be interconnected together with a short wire loop.

Table 4. Current characteristics

Symbol	Ratings	Max.(1)	Unit
I_{VDDX}	Total current into VDDX power lines(2)	100	mA
I_{VSSX}	Total current out of VSSX power lines(2)	100	
I_{IO}	Output current sunk by any I/Os and control pin	Ref. to *Table 12 on page 16*	
	Output current source by any I/Os and control pin	-	
$I_{INJ(PIN)}$(3), (4)	Injected current on any pin	±4	
$I_{INJ(TOT)}$(3), (4), (5)	Sum of injected currents	±20	

1. Data based on characterization results, not tested in production
2. All power V_{DDX} (V_{DD}, V_{DDA}) and ground V_{SSX} (V_{SS}, V_{SSA}) pins must always be connected to the external power supply.
3. The $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if the V_{IN} maximum is respected. If the V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$.
4. The negative injection disturbs the analog performance of the device.
5. When several inputs are submitted to a current injection, the maximum $\Sigma_{IINJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterization with the $\Sigma_{IINJ(PIN)}$ maximum current injection on four I/O port pins of the device.

Table 5. Thermal characteristics

Symbol	Ratings	Max.	Unit
T_{STG}	Storage temperature range	-65 to 150	ºC
T_J	Maximum junction temperature	150	ºC

4.3 Operating conditions

The device must be used in operating conditions that respect the parameters in *Table 6*. In addition, a full account must be taken for all physical capacitor characteristics and tolerances.

Table 6. General operating conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD1}, V_{DDA1}	Operating voltages	-	3(1)	-	5.5(1)	V
V_{DD}, V_{DDA}	Nominal operating voltages	-	3.3(1)	-	5(1)	V
V_{OUT}	Core digital power supply	-	-	1.8(2)	-	V
V_{OUT}	C_{VOUT}: capacitance of external capacitor(3)	at 1 MHz	470	-	3300	nF
V_{OUT}	ESR of external capacitor(2)	at 1 MHz	0.05	-	0.2	Ω
V_{OUT}	ESL of external capacitor(2)	at 1 MHz	-	-	-	-
Θ_{JA}(4)	FR4 multilayer PCB	VFQFPN32	-	26	-	°C/W
T_A	Ambient temperature	Pd = 100 mW	-40	-	105	°C

1. The external power supply can be within the range from 3 V up to 5.5 V.
2. Internal core power supply voltage.
3. Care should be taken when the capacitor is selected due to its tolerance, dependency on temperature, DC bias and frequency.
4. To calculate P_{Dmax} (T_A), use the formula $P_{Dmax} = (T_{Jmax} - T_A)/\Theta_{JA}$.

Table 7. Operating conditions at power-up/power-down

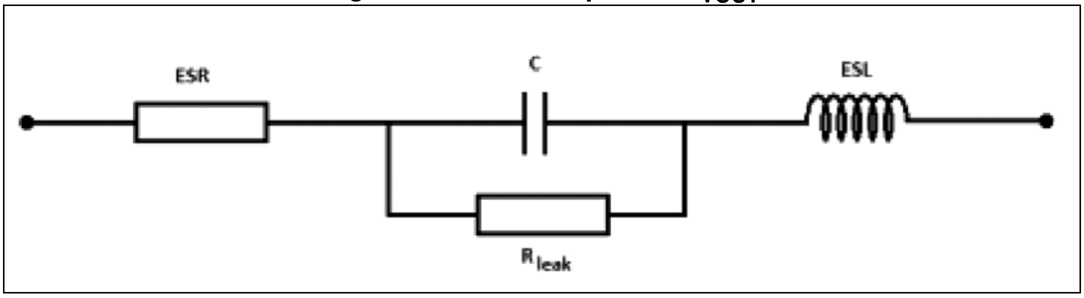
Symbol	Parameter	Conditions	Min.(1)	Typ.	Max.(2)	Unit
t_{TEMP}	Reset release delay	V_{DD} rising	-	3	-	ms
V_{IT+}	Power-on reset threshold	-	2.65	2.8	2.98	V
V_{IT-}	Brownout reset threshold	-	2.58	2.73	2.88	V

1. Guaranteed by design, not tested in production.
2. The power supply ramp must be monotone.

4.3.1 VOUT external capacitor

The stabilization of the main regulator is achieved by connecting an external capacitor C_{VOUT}[a] to the VOUT pin. The C_{VOUT} is specified in *Section 4.3: Operating conditions*. Care should be taken to limit the series inductance to less than 15 nH.

Figure 7. External capacitor C_{VOUT}



4.3.2 Internal clock sources and timing characteristics

HSI RC oscillator

The HSI RC oscillator parameters are specified under general operating conditions for V_{DD} and T_A.

Table 8. HSI RC oscillator

Symbol	Parameter	Conditions	Min.(1)	Typ.	Max.(1)	Unit
f_{HSI}	Frequency	-	-	16	-	MHz
ACC_{HSI}	Accuracy of the HSI oscillator (factory calibrated)(1), (2)	V_{DD} = 3.3 V T_A= 25 ºC	-1%	-	+1%	%
		V_{DD} = 3.3 V -40 ºC ≤ T_A ≤ 105 ºC	-4%	-	+4%	
		V_{DD} = 5 V -40 ºC ≤ T_A ≤ 105 ºC	-4%	-	+4%	
$t_{SU(HSI)}$	HSI oscillator wakeup time including calibration	-	-	1	-	µs

1. Data based on characterization results, not tested in production.
2. Variation referred to f_{HSI} nominal value.

a. ESR is the equivalent series resistance and ESL is the equivalent inductance.

LSI RC oscillator

The LSI RC oscillator parameters are specified under general operating conditions for V_{DD} and T_A.

Table 9. LSI RC oscillator

Symbol	Parameter	Conditions	Min.(1)	Typ.	Max.(1)	Unit
f_{LSI}	Frequency	-	-	153.6	-	kHz
ACC_{LSI}	Accuracy of LSI oscillator	$3.3\ V \leq V_{DD} \leq 5\ V$ $-40\ ºC \leq T_A \leq 105\ ºC$	-10%	-	10%	%
$t_{SU(LSI)}$	LSI oscillator wakeup time	-	-	7	-	µs

1. Guaranteed by design, not tested in production.

PLL internal source clock

Table 10. PLL internal source clock

Symbol	Parameter	Conditions	Min	Typ.	Max.(1)	Unit
f_{IN}	Input frequency(2)	$3.3\ V \leq V_{DD} \leq 5\ V$ $-40\ ºC \leq T_A \leq 105\ ºC$	-	16	-	MHz
f_{OUT}	Output frequency		-	96	-	
t_{lock}	PLL lock time		-	-	200	µs

1. Data based on characterization results, not tested in production.
2. PLL maximum input frequency 16 MHz.

4.3.3 Memory characteristics

Flash program and memory/data EEPROM memory

General conditions: T_A = -40 °C to 105 °C.

Table 11. Flash program memory/data EEPROM memory

Symbol	Parameter	Conditions	Min.(1)	Typ.(1)	Max.(1)	Unit
t_{PROG}	Standard programming time (including erase) for the byte/word/block (1 byte/4 bytes/128 bytes)	-	-	6	6.6	ms
	Fast programming time for 1 block (128 bytes)	-	-	3	3.3	ms
t_{ERASE}	Erase time for 1 block (128 bytes)	-	-	3	3.3	ms
N_{WE}	Erase/write cycles(2) (program memory)	T_A = 25 °C	10 K	-	-	Cycles
	Erase/write cycles(2) (data memory)	T_A = 85 °C	100 K	-	-	
		T_A = 105 °C	35 K	-	-	
t_{RET}	Data retention (program memory) after 10 K erase/write cycles at T_A= 25 °C	T_{RET} = 85 °C	15	-	-	Years
	Data retention (program memory) after 10 K erase/write cycles at T_A= 25 °C	T_{RET} = 105 °C	11	-	-	
	Data retention (data memory) after 100 K erase/write cycles at T_A= 85 °C	T_{RET} = 85 °C	15	-	-	
	Data retention (data memory) after 35 K erase/write cycles at T_A= 105 °C	T_{RET} = 105 °C	6	-	-	
I_{DDPRG}	Supply current during program and erase cycles	-40 ºC ≤ T_A ≤ 105 ºC		2	-	mA

1. Data based on characterization results, not tested in production.
2. The physical granularity of the memory is 4 bytes, so cycling is performed on 4 bytes even when a write/erase operation addresses a single byte.

4.3.4 I/O port pin characteristics

The I/O port pin parameters are specified under general operating conditions for V_{DD} and T_A unless otherwise specified. Unused input pins should not be left floating.

Table 12. Voltage DC characteristics

Symbol	Description	Min.(1)	Typ.	Max.(1)	Unit
V_{IL}	Input low voltage	-0.3	-	0.3 * V_{DD}	V
V_{IH}	Input high voltage(2)	0.7 * V_{DD}	-	V_{DD}	
V_{OL1}	Output low voltage at 3.3 V(3)	-	-	0.4(4)	
V_{OL2}	Output low voltage at 5 V(3)	-	-	0.5	
V_{OL3}	Output low voltage high sink at 3.3 V / 5 V(2),(5), (6)	-	0.6(4)	-	
V_{OH1}	Output high voltage at 3.3 V(3)	V_{DD} - 0.4(4)	-	-	
V_{OH2}	Output high voltage at 5 V(3)	V_{DD} - 0.5	-	-	
V_{OH3}	Output high voltage high sink at 3.3 V / 5 V(2), (5), (6)	V_{DD} - 0.6(4)	-	-	
H_{VS}	Hysteresis input voltage(7)	0.1 * V_{DD}	-	-	
R_{PU}	Pull-up resistor	30	45	60	kΩ

1. Data based on characterization result, not tested in production.
2. All signals are not 5 V tolerant (input signals cannot exceed V_{DDX} (V_{DDX} = V_{DD}, V_{DDA}).
3. Parameter applicable to signals: GPIO_[0:2], DRIVEOUT[0:3], PWM_AUX.
4. Electrical threshold voltage not yet characterized at -40 ºC.
5. The parameter applicable to the signal: SWIM.
6. The parameter applicable to the signal: DIGIN [0].
7. Applicable to any digital inputs.

Table 13. Current DC characteristics

Symbol	Description	Min.	Typ.	Max.[1]	Unit
I_{OL1}	Standard output low level current at 3.3 V and V_{OL1}[2]	-	-	1.5	mA
I_{OL2}	Standard output low level current at 5 V and $V_{OL\ 2}$[2]	-	-	3	
I_{OLhs1}	High sink output low level current at 3.3 V and V_{OL3} [3],[4]	-	-	5	
I_{OLhs2}	High sink output low level current at 5 V and V_{OL}[3],[4]	-	-	7.75	
I_{OH1}	Standard output high level current at 3.3 V and V_{OH1}[2]	-	-	1.5	
I_{OH2}	Standard output high level current at 5 V and V_{OLH2}[2]	-	-	3	
I_{OHhs1}	High sink output low level current at 3.3 V and V_{OH3}[3], [4]	-	-	5	
I_{OHhs2}	High sink output low level current at 5 V and V_{OH3}[3], [4]	-	-	7.75	
I_{LKg}	Input leakage current digital - analog $V_{SS} \leq V_{IN} \geq V_{DD}$[5]	-	-	± 1	µA
$I_{\_Inj}$	Injection current[6], [7]	-	-	±4	mA
$\Sigma I_{\_Inj}$	Total injection current (sum of all I/O and control pins)[6]	-	-	± 20	

1. Data based on characterization result, not tested in production.
2. The parameter applicable to signals: GPIO_[0:2], DRIVEOUT[0:3], PWM_AUX.
3. The parameter applicable to the signal: SWIM.
4. The parameter applicable to the signal: DIGIN [0].
5. Applicable to any digital inputs.
6. The maximum value must never be exceeded.
7. The negative injection current on the ADCIN [7:0] signals (product depending) => SPARE_ADC signals have to be avoided since they impact ADC conversion accuracy.

4.3.5 Typical output level curves

This section shows the typical output voltage level curves measured on a single output pin for the two-pad family present in the STWBC-WA device.

Standard pad

This pad is associated to the following signals: DIGIN [0:1], SWIM and GPIO_[0:2] when available.

Figure 8. V_{OH} standard pad at 3.3 V

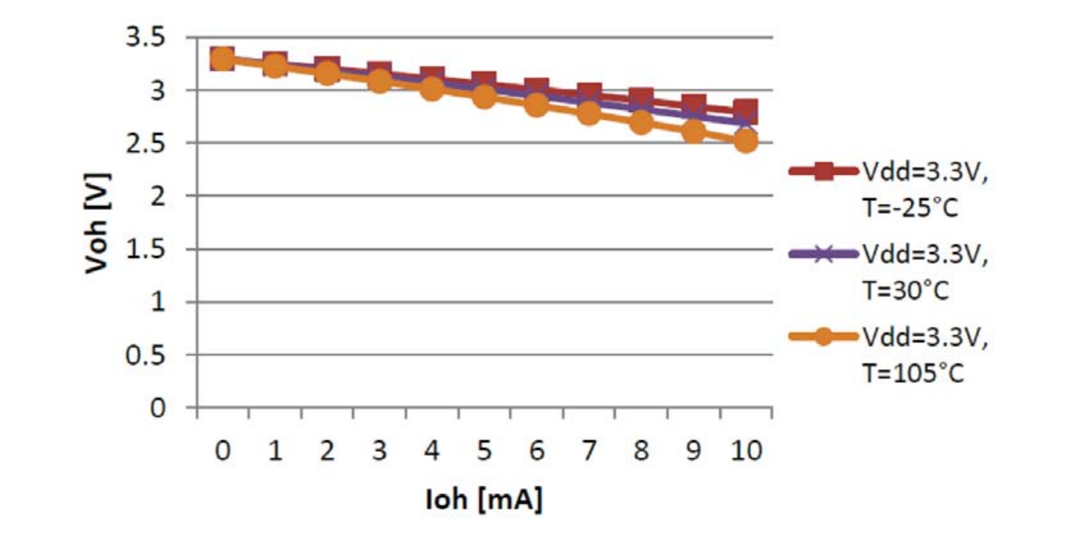


Figure 9. V_{OL} standard pad at 3.3 V

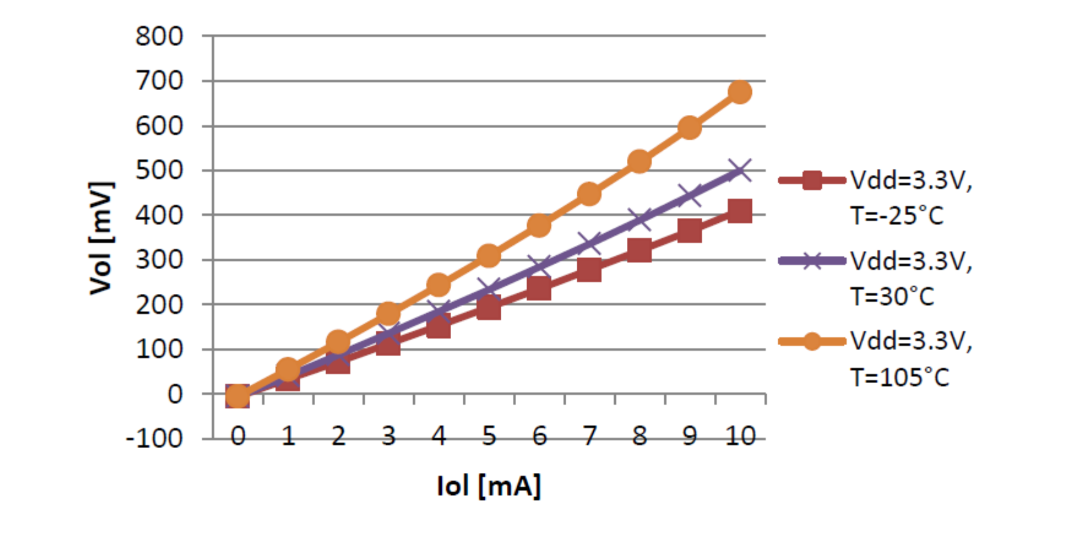


Figure 10. V_{OH} standard pad at 5 V

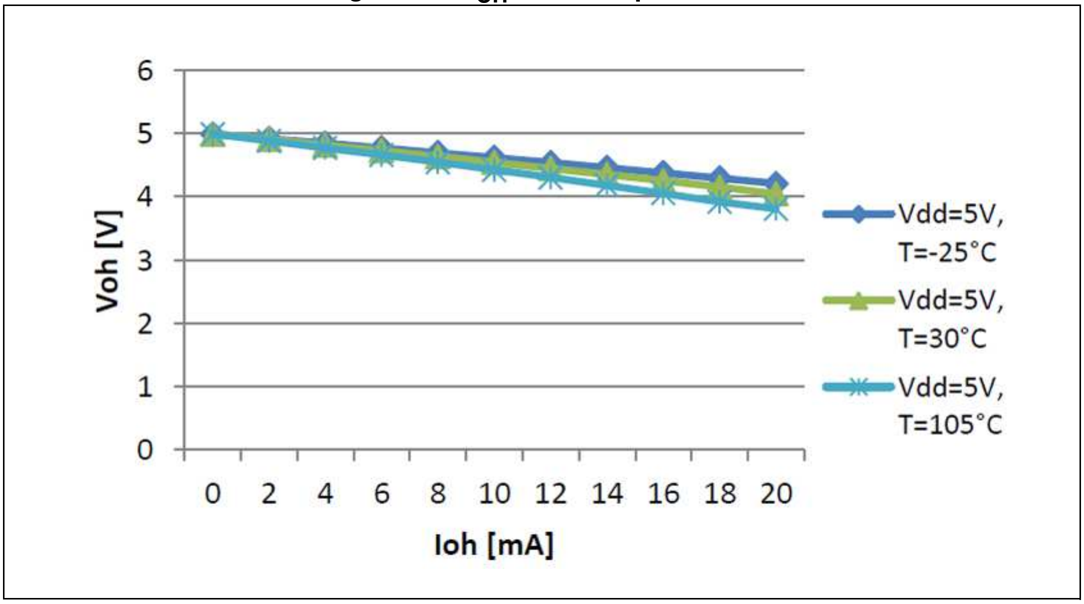
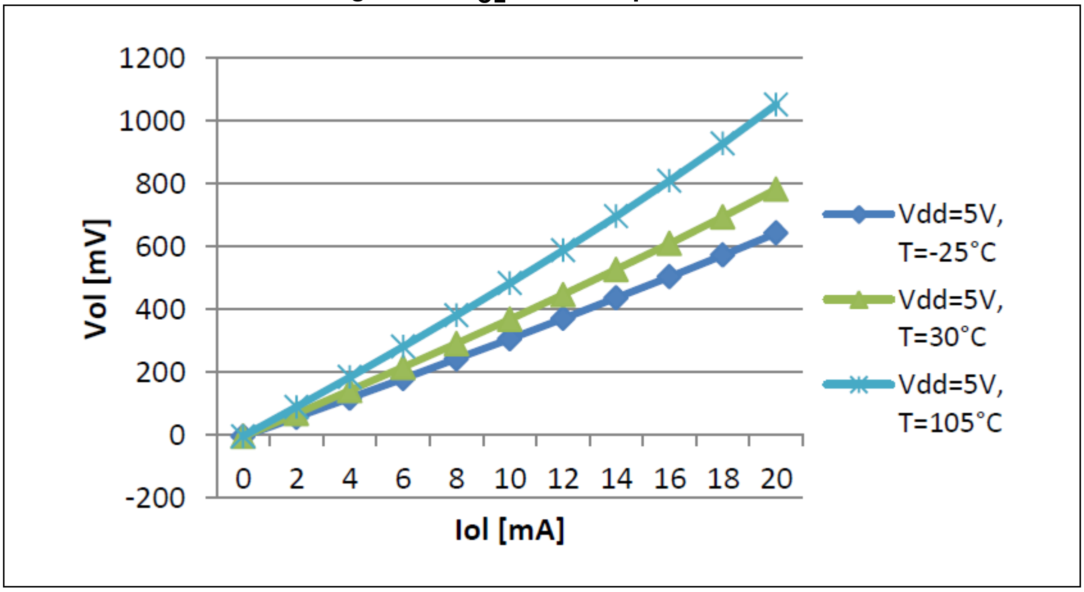


Figure 11. V_{OL} standard pad at 5 V



4.3.6 Fast pad

This pad is associated to the DRIVEOUT[0:3], PWM_AUX signals if the external pin is available.

Figure 12. V_{OH} fast pad at 3.3 V

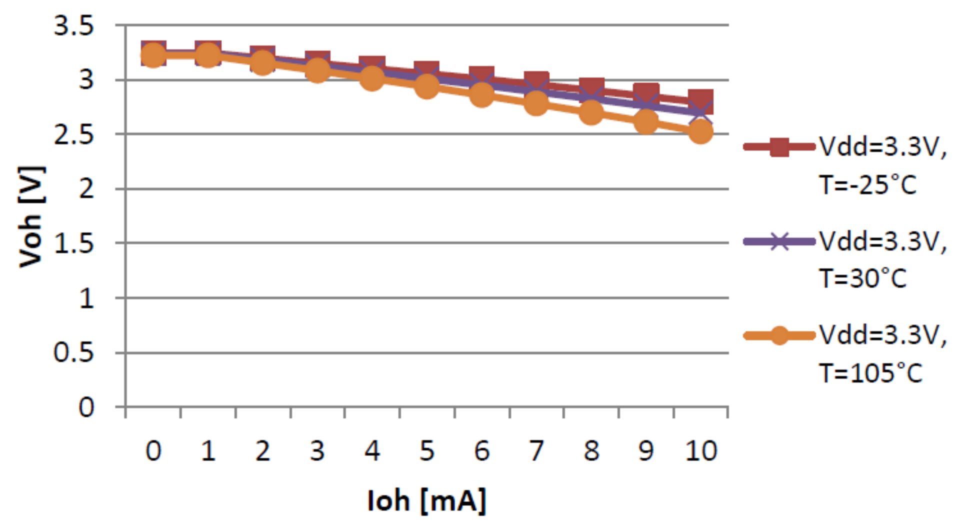


Figure 13. V_{OL} fast pad at 3.3 V

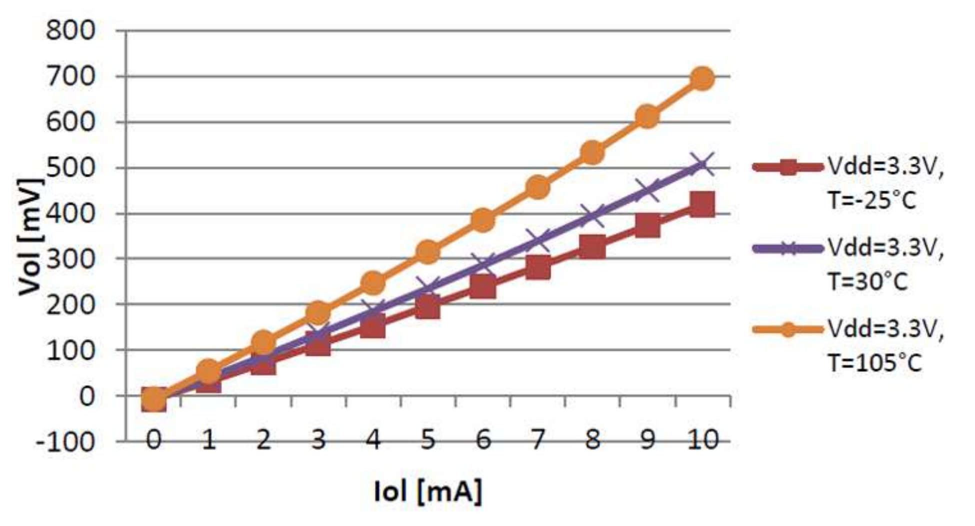


Figure 14. V_{OH} fast pad at 5 V

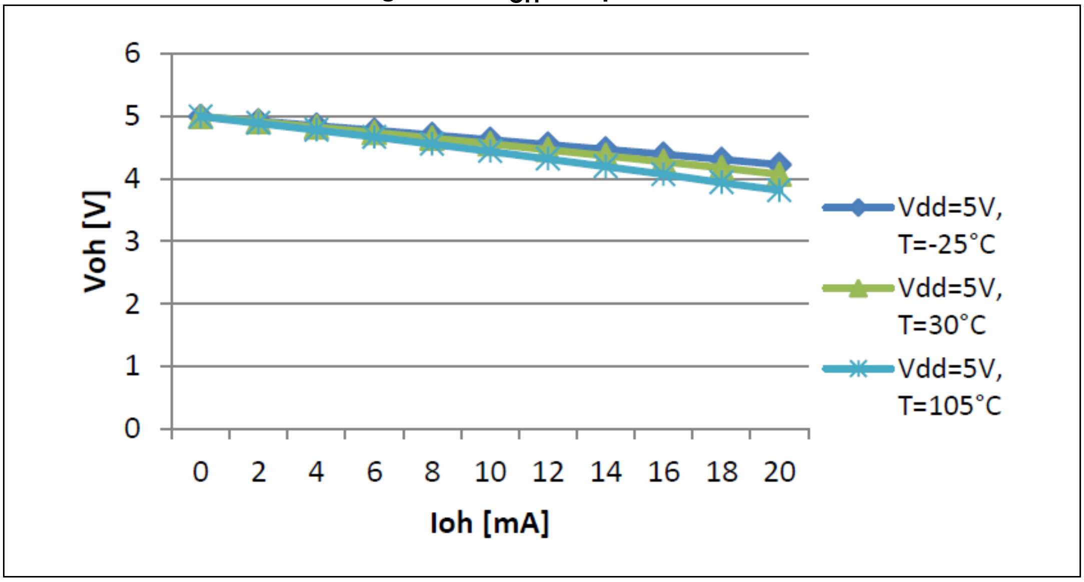
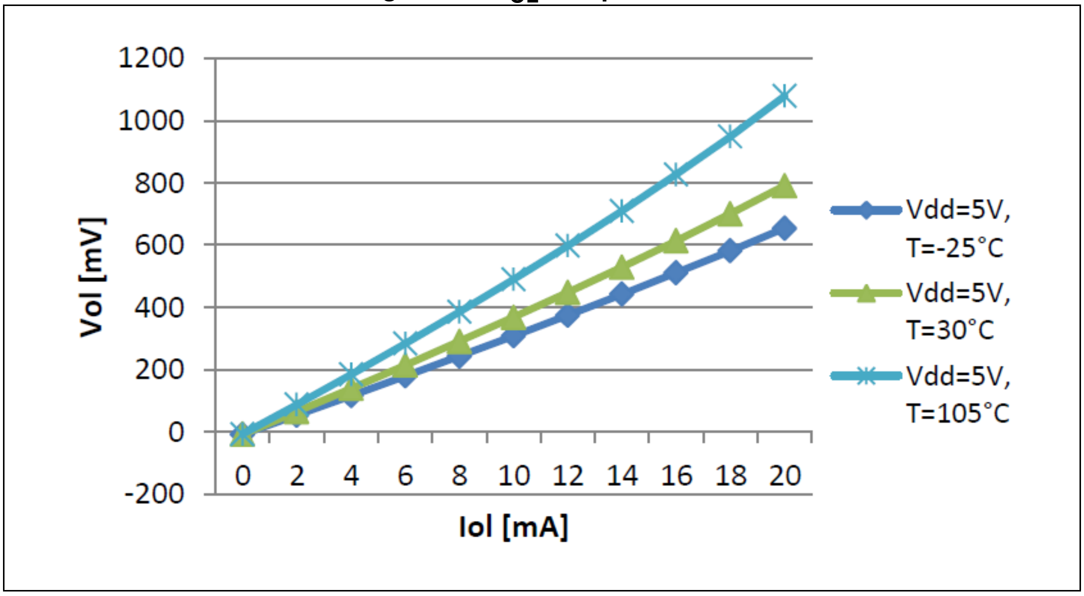


Figure 15. V_{OL} fast pad at 5 V



4.3.7 Reset pin characteristics

The reset pin parameters are specified under general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 14. NRST pin characteristics

Symbol	Parameter	Conditions	Min.(1)	Typ.	Max.(1)	Unit
$V_{IL(NRST)}$	NRST input low level voltage(1)	-	-0.3	-	0.3 x V_{DD}	V
$V_{IH(NRST)}$	NRST input high level voltage(1)	-	0.7 x V_{DD}	-	V_{DD} + 0.3	
$V_{OL(NRST)}$	NRST output low level voltage(1)	I_{OL} = 2 mA	-	-	0.5	
$R_{PU(NRST)}$	NRST pull-up resistor(2)	-	30	40	60	kΩ
$t_{IFP(NRST)}$	NRST input filtered pulse(3)	-	-	-	75	ns
$t_{INFP(NRST)}$	NRST not input filtered pulse(3)	-	500	-	-	
$t_{OP(NRST)}$	NRST output filtered pulse(3)	-	15	-	-	µs

1. Data based on characterization results, not tested in production.
2. The RPU pull-up equivalent resistor is based on a resistive transistor.
3. Data guaranteed by design, not tested in production.

4.3.8 I^2C interface characteristics

Table 15. I^2C interface characteristics

Symbol	Parameter	Standard mode		Fast mode		Unit
		Min.(1)	Max.(1)	Min.(1)	Max.(1)	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	µs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	0(2)	-	0(2)	900(2)	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time (VDD = 3.3 to 5 V)(3)	-	1000	-	300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time (VDD = 3.3 to 5 V)(3)	-	300	-	300	
$t_{h(STA)}$	START condition hold time	4.0	-	0.6	-	µs
$t_{su(STA)}$	Repeated START condition setup time	4.7	-	0.6	-	
$t_{su(STO)}$	STOP condition setup time	4.0	-	0.6	-	µs
$t_{w(STO:STA)}$	STOP to START condition time (bus free)	4.7	-	1.3	-	µs
C_b	Capacitive load for each bus line(4)	-	50	-	50	pF

1. Data based on the standard I^2C protocol requirement, not tested in production.
2. The maximum hold time of the start condition need only be met if the interface does not stretch the low time.
3. I^2C multifunction signals require the high sink pad configuration and the interconnection of 1 K pull-up resistances.
4. 50 pF is the maximum load capacitance value to meet the I^2C std. timing specifications.

4.3.9 10-bit SAR ADC characteristics

The 10-bit SAR ADC oscillator parameters are specified under general operating conditions for V_{DDA} and T_A unless otherwise specified.

Table 16. ADC characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
N	Resolution	-	-	10	-	bit
R_{ADCIN}	ADC input impedance	-	1	-	-	MΩ
V_{IN1}	Conversion voltage range for the gain x1	-	0	-	1.25[(1), (2)]	V
V_{ref}	ADC main reference voltage[(3)]	-	-	1.250	-	V

1. The maximum input analog voltage cannot exceed V_{DDA}.
2. Exceeding the maximum voltage on the SPARE_ADC signals for the related conversion scale must be avoided since the ADC conversion accuracy can be impacted.
3. The ADC reference voltage at T_A = 25 °C.

ADC accuracy characteristics at V_{DD}/V_{DDA} 3.3 V

Table 17. ADC accuracy characteristics at V_{DD}/V_{DDA} 3.3 V

Symbol	Parameter	Typ.[(1)]	Min.[(2)]	Max.[(2)]	Unit
$\|E_T\|$	Total unadjusted error[(3), (4), (5)]	2.8	-	-	LSB
$\|E_O\|$	Offset error[(3), (4), (5)]	0.3	-	-	
$\|E_G\|$	Gain error[(3), (4), (5), (6)]	0.4	-	-	
E_{O+G}	Offset + gain error[(6), (7)]	-	-8.5	9.3	
E_{O+G}	Offset + gain error[(6), (8)]	-	-11	11	
E_{O+G}	Offset + gain error[(6), (9)]	-	-14.3	11.3	
$\|E_D\|$	Differential linearity error[(1), (2), (3)]	0.5	-	-	
$\|E_L\|$	Integral linearity error[(3), (4), (5)]	1.4	-	-	

1. Temperature operating: T_A = 25 °C.
2. Data based on characterization results, not tested in production.
3. ADC accuracy vs. the negative injection current. The injecting negative current on any of the analog input pins should be avoided as this reduces the accuracy of the conversion being performed on another analog input. It is recommended a Schottky diode (pin to ground) to be added to standard analog pins which may potentially inject the negative current. Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in the I/O port pin characteristic section does not affect the ADC accuracy. The ADC accuracy parameters may be also impacted exceeding the ADC maximum input voltage V_{IN1} or V_{IN2}.
4. Results in the manufacturing test mode.
5. Data aligned with trimming voltage parameters.
6. Gain error evaluation with the two point method.
7. Temperature operating range: 0 ºC ≤ T_A ≤ 85 ºC.
8. Temperature operating range: -25 ºC ≤ T_A ≤ 105 ºC.
9. Temperature operating range: -40 ºC ≤ T_A ≤ 105 ºC.

ADC accuracy characteristics at V_{DD}/V_{DDA} 5 V

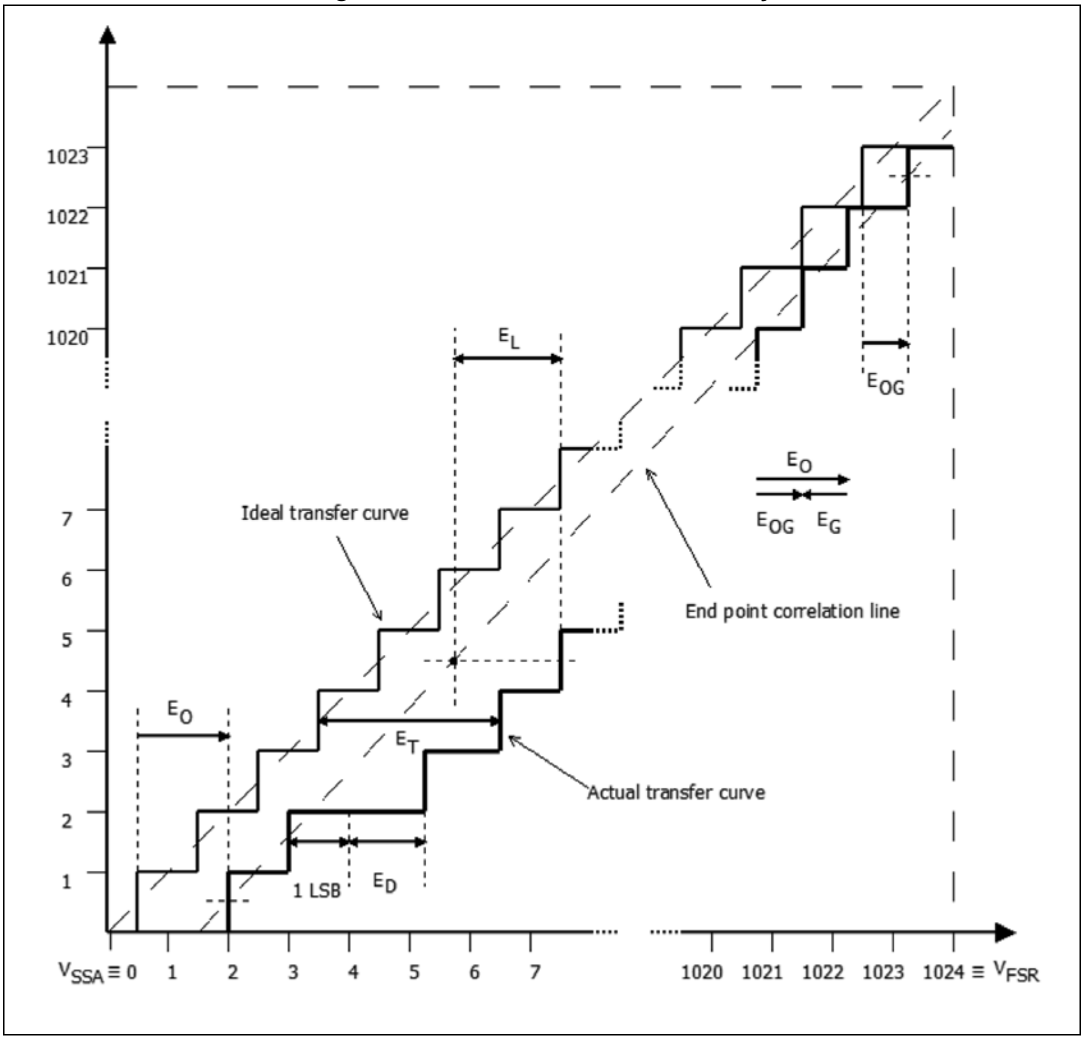
Table 18. ADC accuracy characteristics at V_{DD}/V_{DDA} 5 V

Symbol	Parameter	Typ.(1)	Min.(2)	Max.(2)	Unit
$\lvert E_T \rvert$	Total unadjusted error(3) (4), (5)	TBD	-	-	LSB
$\lvert E_O \rvert$	Offset error(3), (4), (5)	0.5	-	-	
$\lvert E_G \rvert$	Gain error(3), (4), (5), (6)	0.4	-	-	
E_{O+G}	Offset + gain error(6), (7)	-	-8.3	8.9	
E_{O+G}	Offset + gain error(6), (8)	-	-10.9	10.9	
EO+G	Offset + gain error(6), (9)	-	-13.8	10.9	
$\lvert E_D \rvert$	Differential linearity error(1), **(2)**, (3)	0.8	-	-	
$\lvert E_L \rvert$	Integral linearity error(3), (4), (5)	2.0	-	-	

1. Operating temperature: T_A = 25 °C.
2. Data based on characterization results, not tested in production.
3. ADC accuracy vs. the negative injection current. The injecting negative current on any of the analog input pins should be avoided as this reduces the accuracy of the conversion being performed on another analog input. It is recommended that a Schottky diode (pin to ground) be to added to standard analog pins which may potentially inject the negative current. Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma_{IINJ(PIN)}$ in the I/O port pin characteristic section does not affect the ADC accuracy. The ADC accuracy parameters may be also impacted exceeding the ADC maximum input voltage V_{IN1} or V_{IN2}.
4. Results in the manufacturing test mode.
5. Data aligned with trimming voltage parameters.
6. Gain error evaluation with the two point method.
7. Operating temperature range: 0 ºC ≤ T_A ≤ 85 ºC.
8. Operating temperature range: -25 ºC ≤ T_A ≤ 105 ºC.
9. Operating temperature range: -40 ºC ≤ T_A ≤ 105 ºC.

ADC conversion accuracy

Figure 16. ADC conversion accuracy



ADC accuracy parameter definitions:

- $\mathbf{E_T}$ = total unadjusted error: the maximum deviation between the actual and the ideal transfer curves.
- $\mathbf{E_O}$ = offset error: the deviation between the first actual transition and the first ideal one.
- $\mathbf{E_{OG}}$ = offset + gain error (1-point gain): the deviation between the last ideal transition and the last actual one.
- $\mathbf{E_G}$ = gain error (2-point gain): defined so that $E_{OG} = E_O + E_G$ (parameter correlated to the deviation of the characteristic slope).
- $\mathbf{E_D}$ = differential linearity error: the maximum deviation between actual steps and the ideal one.
- $\mathbf{E_L}$ = integral linearity error: the maximum deviation between any actual transition and the end point correlation line.