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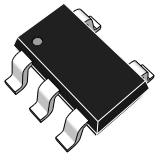
STWD100

Watchdog timer circuit

Datasheet - production data

SOT23-5/SC70-5 (SOT323-5)



Features

- Current consumption 13 µA typ.
- Available watchdog timeout periods are 3.4 ms, 6.3 ms, 102 ms, and 1.6 s
- Chip enable input
- Open drain or push-pull $\overline{\text{WDO}}$ output
- Operating temperature range: –40 to 125 °C
- Packages: SOT23-5 and SC70-5 (SOT323-5)
- ESD performance
  - HBM: 2000 V
  - CDM: 1000 V
- Automotive qualified

Applications

- Telecommunications
- Alarm systems
- Industrial equipment
- Networking
- Medical equipment
- UPS (uninterruptible power supply)
- Automotive

Description

The STWD100 watchdog timer circuits are self-contained devices which prevent system failures that are caused by certain types of hardware errors (such as, non-responding peripherals and bus contention) or software errors (such as a bad code jump and a code stuck in loop).

The STWD100 watchdog timer has an input, WDI, and an output, $\overline{\text{WDO}}$. The input is used to clear the internal watchdog timer periodically within the specified timeout period, t_{wd}. While the system is operating correctly, it periodically toggles the watchdog input, WDI. If the system fails, the watchdog timer is not reset, a system alert is generated and the watchdog output, $\overline{\text{WDO}}$, is asserted.

The STWD100 circuit also has an enable pin, $\overline{\text{EN}}$, which can enable or disable the watchdog functionality. The $\overline{\text{EN}}$ pin is connected to the internal pull-down resistor. The device is enabled if the $\overline{\text{EN}}$ pin is left floating.

This is information on a product in full production. www.st.com

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1 Package pin connections and pin description table

Figure 1: SOT23-5 and SC70-5 (SOT323-5) pin connections

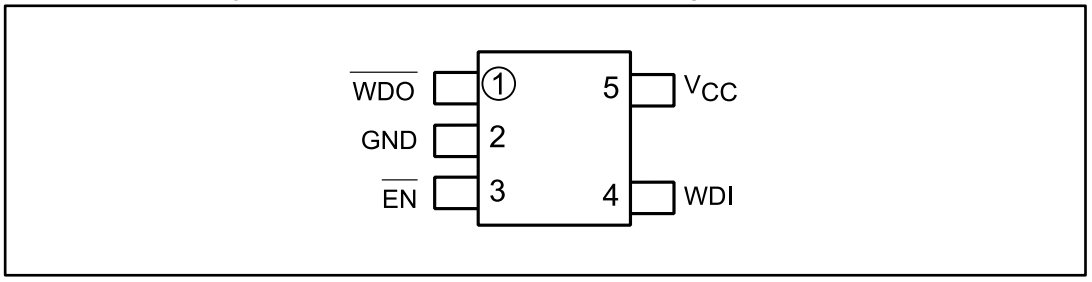
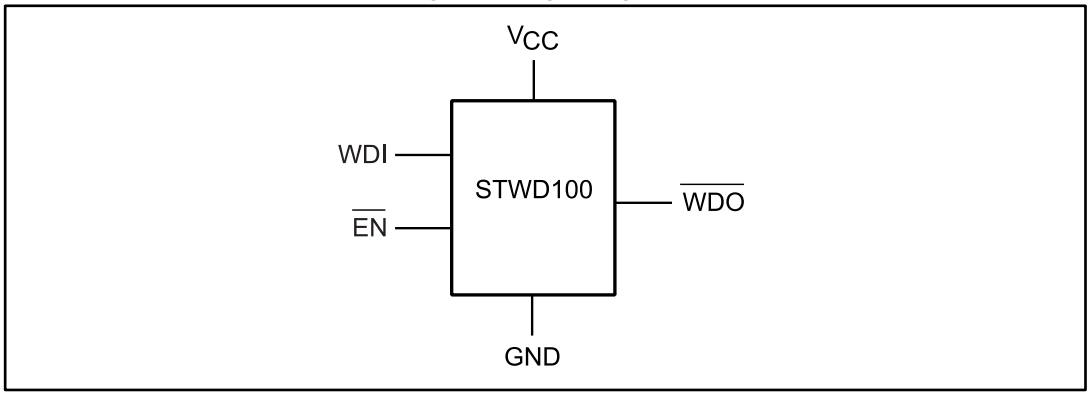


Table 1: SOT23-5 and SC70-5 (SOT323-5) pin description

Pin number	Name	Description
1	$\overline{WDO}$	Watchdog output
2	GND	Ground
3	$\overline{EN}$	Enable pin
4	WDI	Watchdog input
5	V_{CC}	Supply voltage

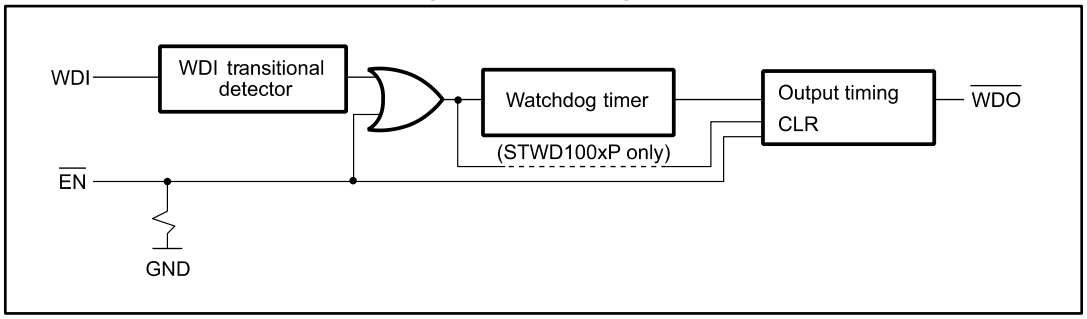
2 Functional description

Figure 2: Logic diagram



1. The $\overline{\text{WDO}}$ output is available *in open drain or push-pull configuration.*

Figure 3: Block diagram



1. If the positive pulse on the enable pin, $\overline{\text{EN}}$, is longer than 1 µs, it resets the watch.

3 Operation

The STWD100 device is used to detect an out-of-control MCU. The user has to ensure watchdog reset within the watchdog timeout period, otherwise the watchdog output is asserted and the MCU is restarted. The STWD100 can also be enabled or disabled by the chip enable pin.

3.1 Watchdog input (WDI)

The WDI input has to be toggled within the watchdog timeout period, t_{WD}, otherwise the watchdog output, $\overline{WDO}$, is asserted. The internal watchdog timer, which counts the t_{WD} period, is cleared as follows:

1. by a transition on the watchdog output, $\overline{WDO}$ (see *Figure 8: "Timeout without re-trigger"*) or
2. by a pulse on the enable pin, $\overline{EN}$ (see *Figure 10: "Enable pin, $\overline{EN}$, triggering"*) or
3. by toggling the WDI input (low-to-high on all versions and high-to-low on the STWD100xW, STWD100xX and STWD100xY only).

The pulses on the WDI input with a duration of at least 1 µs are detected and glitches shorter than 100 ns are ignored.

If the WDI is permanently tied high or low and $\overline{EN}$ is tied low, the $\overline{WDO}$ toggles every 3.4 ms (t_{WD}) on the STWD100xP and every t_{WD} and t_{PW} on the STWD100xW, STWD100xX and STWD100xY (see *Figure 8: "Timeout without re-trigger"*).

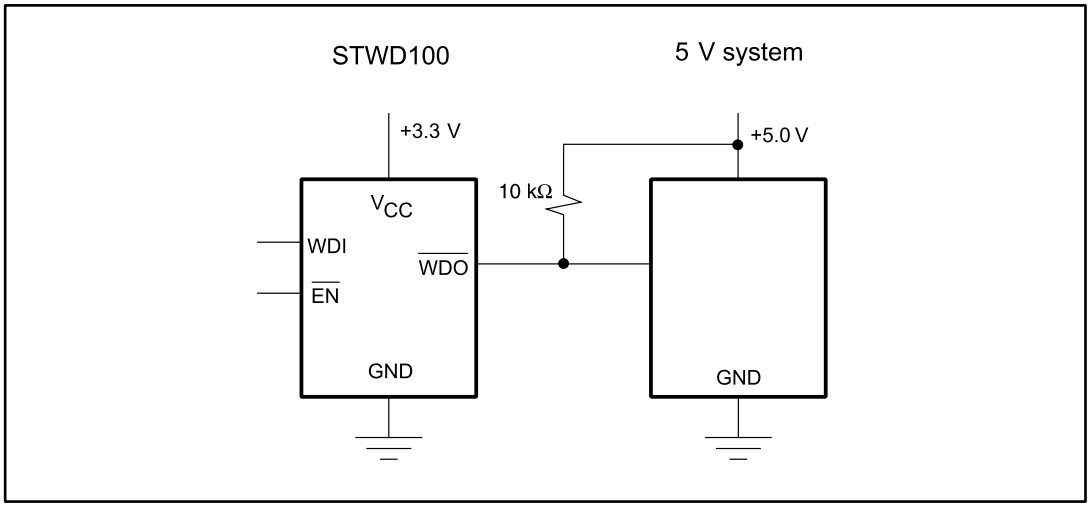
3.2 Watchdog output ($\overline{WDO}$)

When the V_{CC} exceeds the timer startup voltage, V_{START}, after power-up, the internal watchdog timer starts counting. If the timer is not cleared within the t_{WD}, the $\overline{WDO}$ goes low (see *Figure 6: "Power-up"*).

After exceeding the t_{WD}, the $\overline{WDO}$ is asserted for t_{PW} on STWD100xW, STWD100xX and STWD100xY regardless of possible WDI transitions (see *Figure 9: "Trigger after timeout"*). On the STWD100xP, $\overline{WDO}$ is asserted for a minimum of 10 µs and a maximum of t_{WD} after exceeding the t_{WD} period (see *Figure 8: "Timeout without re-trigger"* and *Figure 9: "Trigger after timeout"*).

The STWD100 has an active low open drain or push-pull output. An external pull-up resistor connected to any supply voltage up to 6 V is required in case of an open drain $\overline{WDO}$ output (see *Figure 4: "Open drain $\overline{WDO}$ output connection"*). Select a resistor value large enough to register a logic low, and small enough to register a logic high while supplying all input current and leakage paths connected to the reset output line. A 10 kΩ pull-up resistor is sufficient in most applications.

Figure 4: Open drain $\overline{\text{WDO}}$ output connection



3.3 Chip enable input ($\overline{\text{EN}}$)

All states mentioned in *Section 3.1: "Watchdog input (WDI)"* and *Section 3.2: "Watchdog output ($\overline{\text{WDO}}$)"* are valid under the condition that $\overline{\text{EN}}$ is in logical low state.

The behavior of $\overline{\text{EN}}$ is common to all versions (i.e. STWD100xP, STWD100xW, STWD100xX and STWD100xY).

If the $\overline{\text{EN}}$ goes high after power-up, in less than t_{WD} from the moment that V_{CC} exceeds the timer startup voltage, V_{START}, the $\overline{\text{WDO}}$ stays high for the same time period as $\overline{\text{EN}}$, plus t_{WD} (see *Figure 10: "Enable pin, $\overline{\text{EN}}$, triggering"*).

If the $\overline{\text{EN}}$ goes high anytime during normal operation, the $\overline{\text{WDO}}$ goes high as well, but the minimum possible $\overline{\text{WDO}}$ pulse width is 10 µs (see *Figure 10: "Enable pin, $\overline{\text{EN}}$, triggering"*).

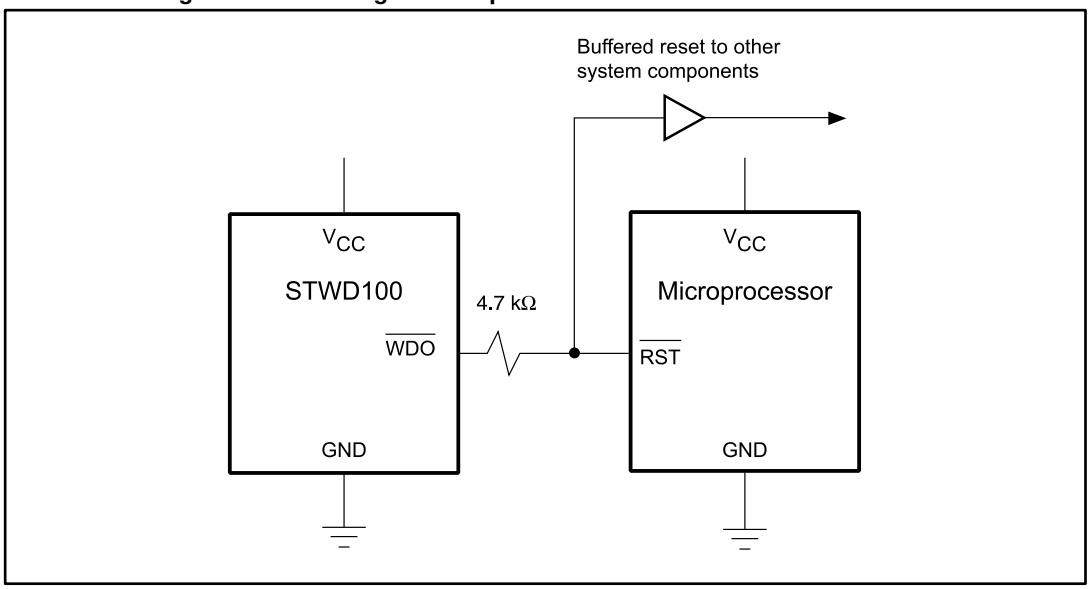
Pulses on the $\overline{\text{EN}}$ pin with a duration of at least 1 µs are detected and glitches shorter than 100 ns are ignored.

3.4 Applications information

Interfacing to microprocessors with bidirectional reset pins

Microprocessors with bidirectional reset pins can contend with the STWD100 watchdog output, $\overline{WDO}$. For example, if the $\overline{WDO}$ output is driven high and the micro wants to pull it low, signal contention is the result. To prevent this from occurring, connect a 4.7 kΩ resistor between the $\overline{WDO}$ output and the microprocessors reset I/O as in *Figure 5: "Interfacing to microprocessors with bidirectional reset I/O"*.

Figure 5: Interfacing to microprocessors with bidirectional reset I/O



4 Watchdog timing

Figure 6: Power-up

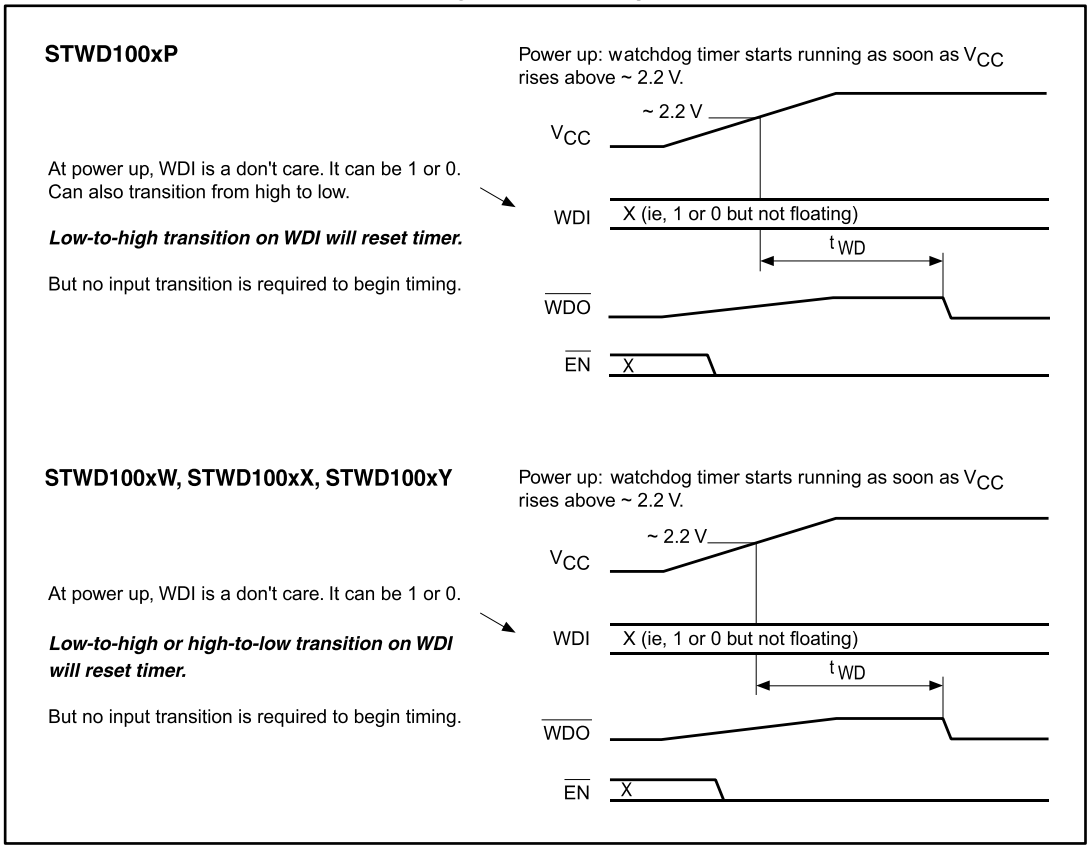


Figure 7: Normal triggering

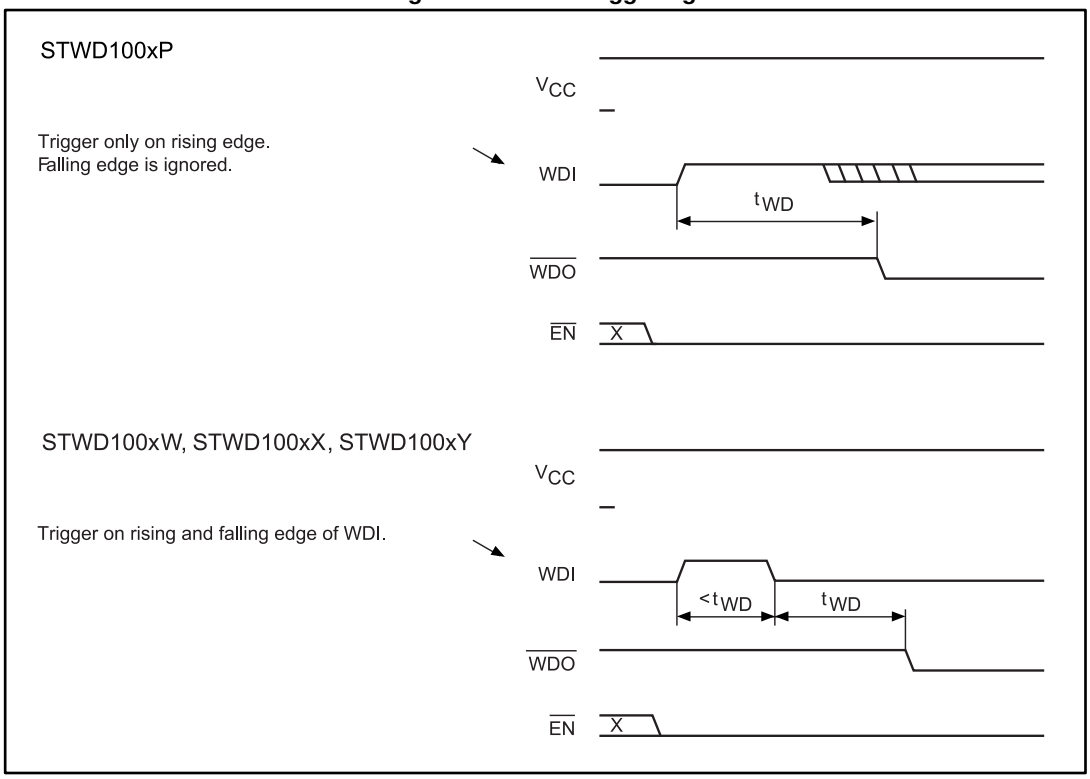


Figure 8: Timeout without re-trigger

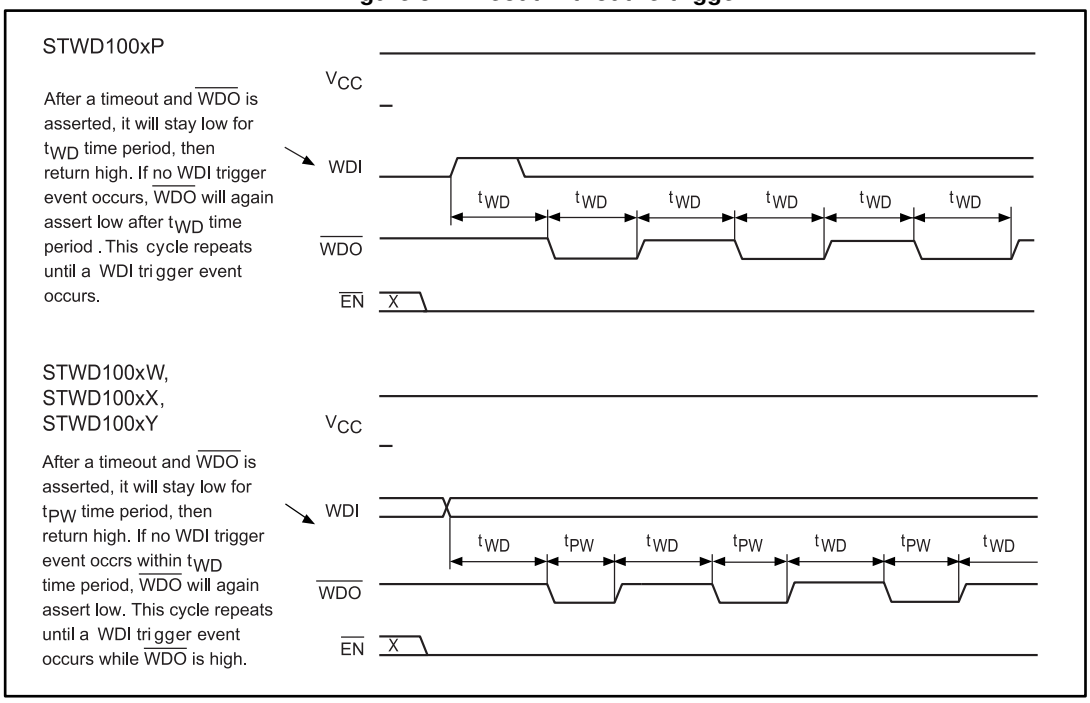


Figure 9: Trigger after timeout

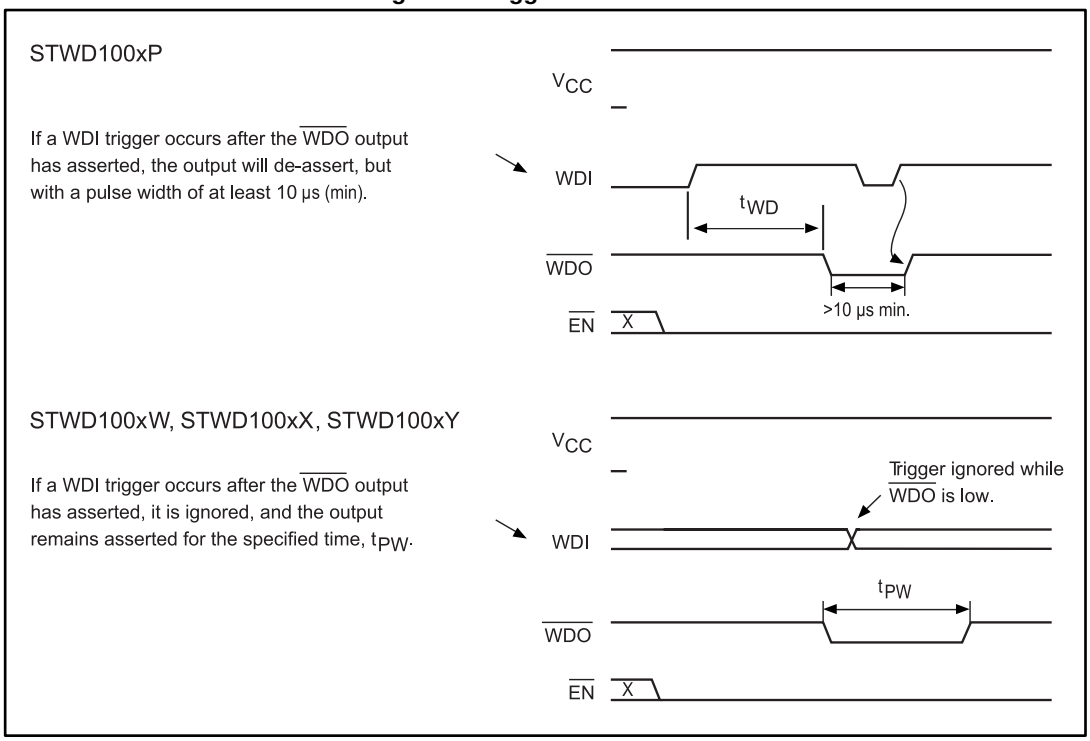
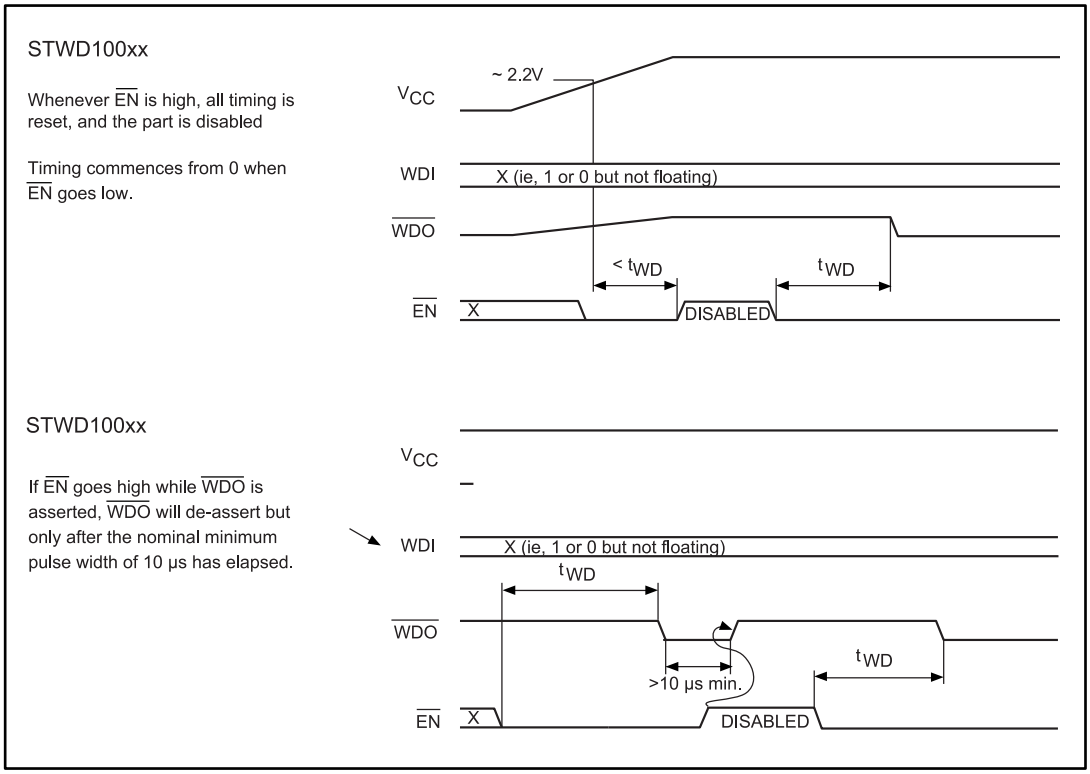


Figure 10: Enable pin, $\overline{EN}$, triggering



5 Maximum ratings

Stressing the device above the ratings listed in *Table 2: "Absolute maximum ratings"* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in *Table 3: "Operating and AC measurement conditions"* of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE program and other relevant quality documents.

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
T_{STG}	Storage temperature (V_{CC} off)	–55 to 150	°C
T_{SLD} (1)	Lead solder temperature for 10 seconds	260	
V_{IO}	Input or output voltage	–0.3 to V_{CC} + 0.3	V
V_{CC}	Supply voltage	–0.3 to 7.0	
I_O	Output current	20	mA
P_D	Power dissipation	320	mW

Notes:

(1)Reflow at peak temperature of 260 °C (total thermal budget not to exceed 245 °C for greater than 30 seconds).

The maximum ratings related to soldering conditions are marked on the inner box label of the product packages.

6 DC and AC parameters

This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in that follow, are derived from tests performed under the measurement conditions summarized in *Table 3: "Operating and AC measurement conditions"*. Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

Table 3: Operating and AC measurement conditions

Parameter	Value	Unit
V_{CC} supply voltage	2.7 to 5.5	V
Ambient operating temperature (T_A)	–40 to 125	°C
Input rise and fall times	≤ 5	ns
Input pulse voltages	0.2 to 0.8 V_{CC}	V
Input and output timing ref. voltages	0.3 to 0.7 V_{CC}	

Table 4: DC and AC characteristics

Symbol	Description	Test condition (1)	Min.	Typ.	Max.	Unit
V_{CC}	Operating voltage		2.7	5	5.5	V
I_{CC}	V_{CC} supply current			13	26	µA
I_{LO}	Open drain output leakage current	From output to the GND or V_{CC}	-1		1	
	Input leakage current (WDI)		-1		1	
V_{IH}	Input high voltage (WDI, $\overline{EN}$)		0.7 V_{CC}			V
V_{IL}	Input low voltage (WDI, $\overline{EN}$)				0.3 V_{CC}	
V_{OL}	Output low voltage ($\overline{WDO}$)	V_{CC} ≥ 2.7 V, I_{SINK} = 1.2 mA			0.3	
		V_{CC} ≥ 4.5 V, I_{SINK} = 3.2 mA			0.4	
V_{OH}	Output high voltage ($\overline{WDO}$), push-pull only	V_{CC} ≥ 2.7 V, I_{SOURCE} = 500 µA	0.8 V_{CC}			
		V_{CC} ≥ 4.5 V, I_{SOURCE} = 800 µA	0.8 V_{CC}			
Enable pin ($\overline{EN}$)						
	$\overline{EN}$ input pulse width		1			µs
	$\overline{EN}$ glitch rejection			100		ns
	$\overline{EN}$ - to - $\overline{WDO}$ delay (2)			200		
	$\overline{EN}$ pull-down resistance		32	63	100	kΩ

Symbol	Description	Test condition (1)	Min.	Typ.	Max.	Unit
Watchdog timer						
V_{START}	Timer startup voltage		1.9	2.2	2.7	V
t_{WD}	Watchdog timeout period	STWD100xP	2.3	3.4	4.6	ms
		STWD100xW	4.3	6.3	8.6	
		STWD100YxW	5.1	6.3	8.6	
		STWD100xX	71	102	142	
		STWD100xY	1.12	1.6	2.24	s
t_{PW}	Watchdog active time		140	210	280	ms
	WDI - to - $\overline{WDO}$ delay (3)			150		ns
	WDI pulse width		1			µs
	WDI glitch rejection			100		ns

Notes:

(1)Valid for ambient operating temperature: T_A = –40 to 125 °C; V_{CC} = 2.7 V to 5.5 V except where noted.

(2) $\overline{WDO}$ asserts for minimum of 10 µs even if EN transitions high.

(3) $\overline{WDO}$ asserts for minimum of 10 µs regardless of transition on WDI (valid for STWD100xP only).

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

7.1 SOT23-5 package information

Figure 11: SOT23-5 package outline

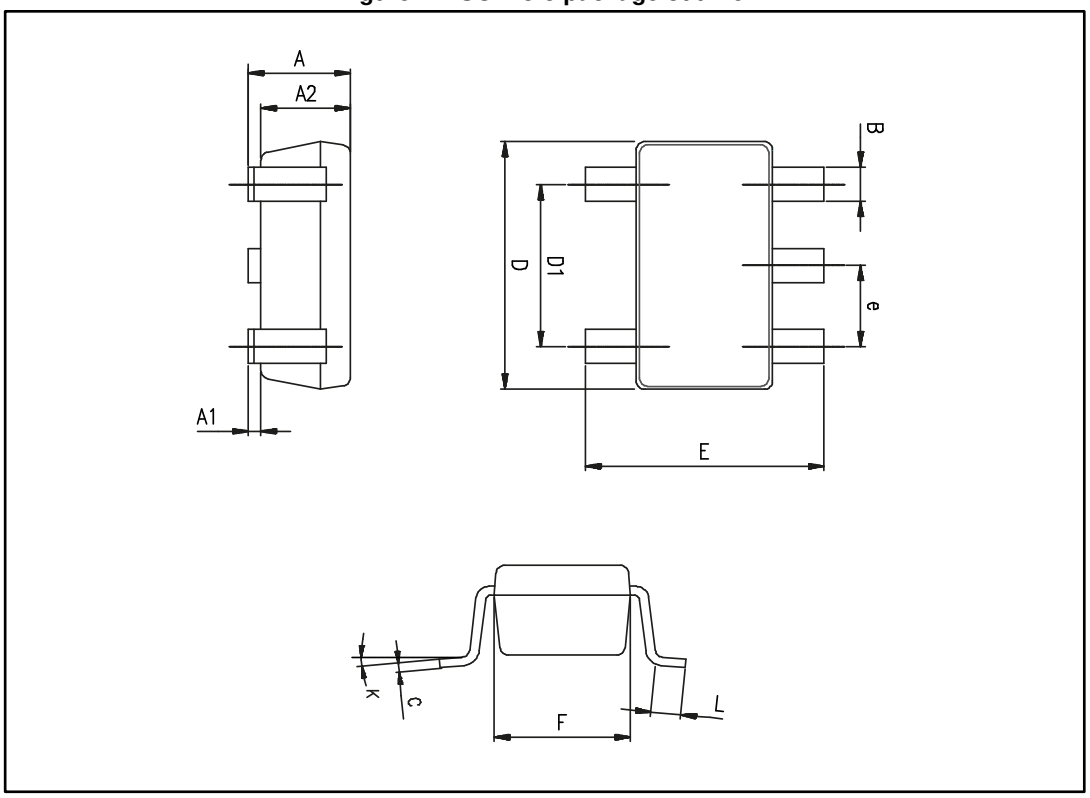


Table 5: SOT23-5 mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.90	1.20	1.45	0.035	0.047	0.057
A1			0.15			0.006
A2	0.90	1.05	1.30	0.035	0.041	0.051
B	0.35	0.40	0.50	0.014	0.016	0.020
C	0.09	0.15	0.20	0.004	0.006	0.008
D	2.80	2.90	3.00	0.110	0.114	0.118
D1		1.90			0.075	
e		0.95			0.037	
E	2.60	2.80	3.00	0.102	0.110	0.118
F	1.50	1.60	1.75	0.059	0.063	0.069
L	0.10	0.35	0.60	0.004	0.014	0.024
K	0 degrees		10 degrees	0 degrees		10 degrees

7.2 SC70-5 (or SOT323-5) package information

Figure 12: SC70-5 (or SOT323-5) package outline

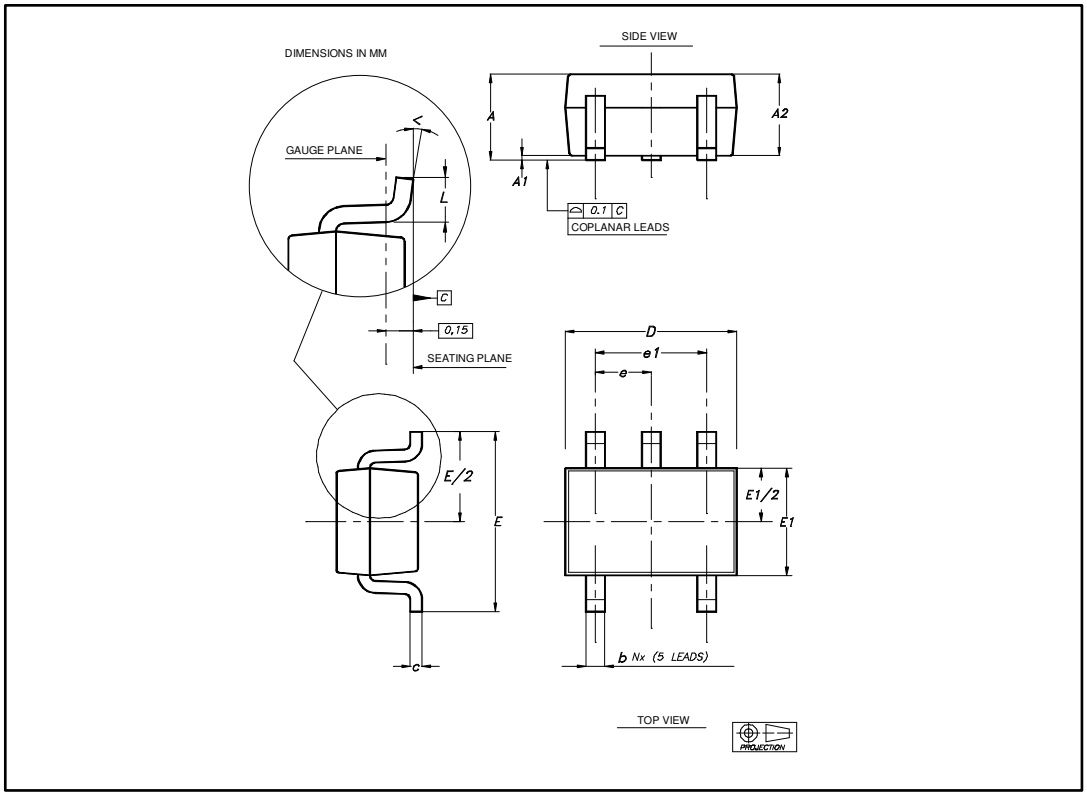


Table 6: SC70-5 (or SOT323-5) mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.80		1.10	0.032		0.043
A1			0.10			0.004
A2	0.80	0.90	1.00	0.032	0.035	0.039
b	0.15		0.30	0.006		0.012
c	0.10		0.22	0.004		0.009
D	1.80	2.00	2.20	0.071	0.079	0.087
E	1.80	2.10	2.40	0.071	0.083	0.094
E1	1.15	1.25	1.35	0.045	0.049	0.053
e		0.65			0.025	
e1		1.30			0.051	
L	0.26	0.36	0.46	0.010	0.014	0.018
<	0°		8°	0°		8°

8 Ordering information

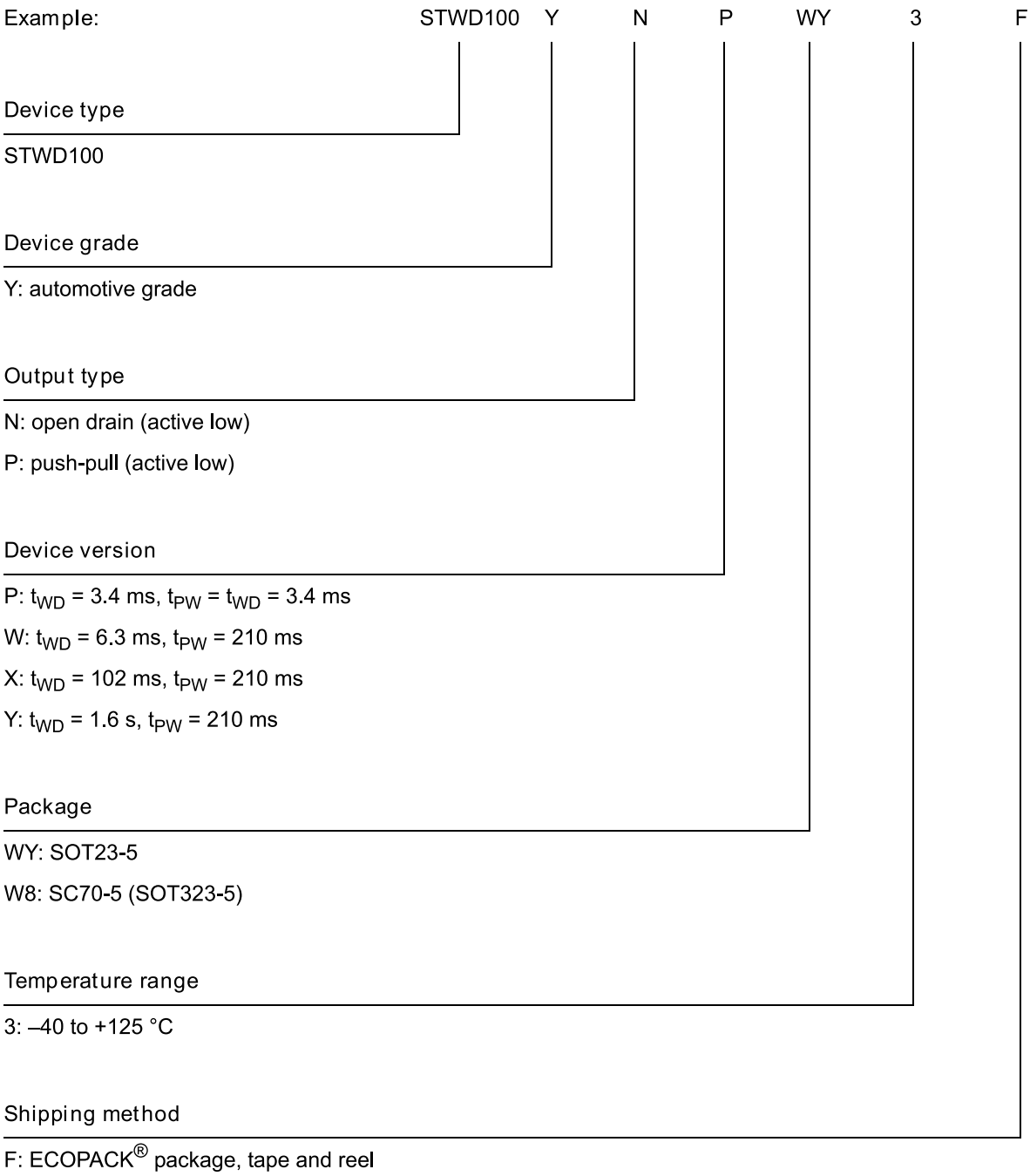
Table 7: Order codes

Order code	Temperature range	Package	Packing	Topside marking
STWD100NWWY3F	-40 to 125 °C	SOT23-5	Tape and reel	WNW
STWD100YNWWY3F (1)		SOT23-5 (automotive grade)		WYNW
STWD100NYWY3F		SOT23-5		WNY
STWD100YNYWY3F (1)		SOT23-5 (automotive grade)		WYNY
STWD100NPWY3F		SOT23-5		WNP
STWD100YNPWY3F (1)		SOT23-5 (automotive grade)		WYNP
STWD100PYW83F		SC70 (SOT323-5)		WPY
STWD100NXWY3F		SOT23-5		WNX
STWD100YNXWY3F (1)		SOT23-5 (automotive grade)		WYNX

Notes:

(1)Qualification and characterization according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 and Q002 or equivalent.

Figure 13: Ordering information scheme



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9 Revision history

Table 8: Document revision history

Date	Revision	Changes
08-Nov-2007	1	Initial release.
23-Jan-2008	2	Updated cover page and Table 4; document status upgraded to full datasheet.
28-Jan-2008	3	Updated cover page.
17-Mar-2008	4	Updated cover page, Figure 4, 7, 9, and Table 4, 9.
31-Jul-2008	5	Updated Features on cover page and Table 4.
05-Mar-2012	6	Added product maturity information and section Applications, updated Section 1, Section 3.4, Section 5, Section 6, Section 8 and Section 8, ECOPACK® text, minor text corrections throughout document.
26-Oct-2012	7	Updated Features (added ESD information). Added Table 1: Device summary. Updated Table 7 (added automotive grade version to the device type). Minor corrections throughout document.
11-Mar-2014	8	Updated Table 1: Device summary and Table 7: Ordering information scheme Added STWD100YxW and values to t_{WD} in Table 4: DC and AC characteristics
25-Sep-2015	9	Updated layout: added Section 1: Package connections and pin description and Section 2: Functional description; renamed Section 7: Part numbering as Section 8: Ordering information; renamed Table 1: Device summary as Table 7: Order codes and moved to Section 8: Ordering information. Added new order code STWD100YNXWY3F to Table 7: Order codes. Removed Section 8: Package marking information
22-Sep-2016	10	Updated document layout and made some small text changes. Features: added automotive qualification Applications: added automotive
20-Jan-2017	11	*Features*: replaced "RCDM" with "CDM". *Table 2: "Absolute maximum ratings"*: updated value of V_{IO}. *Table 7: "Order codes"*: added new order code STWD100NXWY3F.

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