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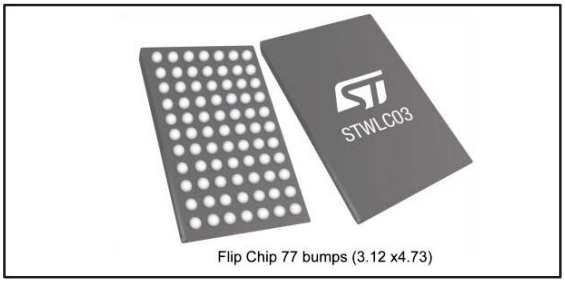
STWLC03

Dual mode Qi/PMA wireless power receiver

Datasheet - production data



Flip Chip 77 bumps (3.12 x4.73)

Features

- 1 W to 12 W output power
- Qi 1.1 and PMA wireless standard communication protocols
- Integrated high efficiency synchronous rectifier
- 800 kHz programmable step-down converter with input current and input voltage regulation loops
- Step-down converter efficiency up to 90%
- Simplified Li-Ion/Polymer charger function
- 32-bit, 16 MHz embedded microcontroller with 16 kB ROM and 2 kB RAM memory
- 2 kB NVM for customization
- Integrated driver for external supply switch
- Precise voltage and current measurements for received power calculation
- I^2C interface
- Configurable GPIO output
- Rx coil NTC protection
- Thermal protection
- Low power dissipative rectifier overvoltage clamp
- Flip Chip 77 bumps (3.12x4.73 mm)

Applications

- Cellular phones
- Power banks
- Navigation systems
- Tablets
- Medical and healthcare instrumentation

Description

The STWLC03 is an integrated wireless power receiver solution suitable for portable applications. The STWLC03 is able to operate with Qi 1.1 or PMA communication protocol. Thanks to the integrated low impedance synchronous rectifier and DC-DC step-down converter, the STWLC03 achieves high efficiency, low power dissipation and output power beyond 5 W. Digital control and precise analog control loops ensure stable operation. I^2C interface allows many parameters to be customized in the device and this configuration can be stored in the embedded NVM.

The STWLC03 can deliver the output power in two modes: as a power supply with configured output voltage or as a simple CC/CV battery charger with configurable charging current.

The STWLC03 can detect an external (wired) power supply connection and drive an external power switch.

Table 1: Device summary

Order code	Description	Package	Packing
STWLC03JR	12 W output	Flip Chip 77 bumps (3.12x4.73 mm)	Tape and reel

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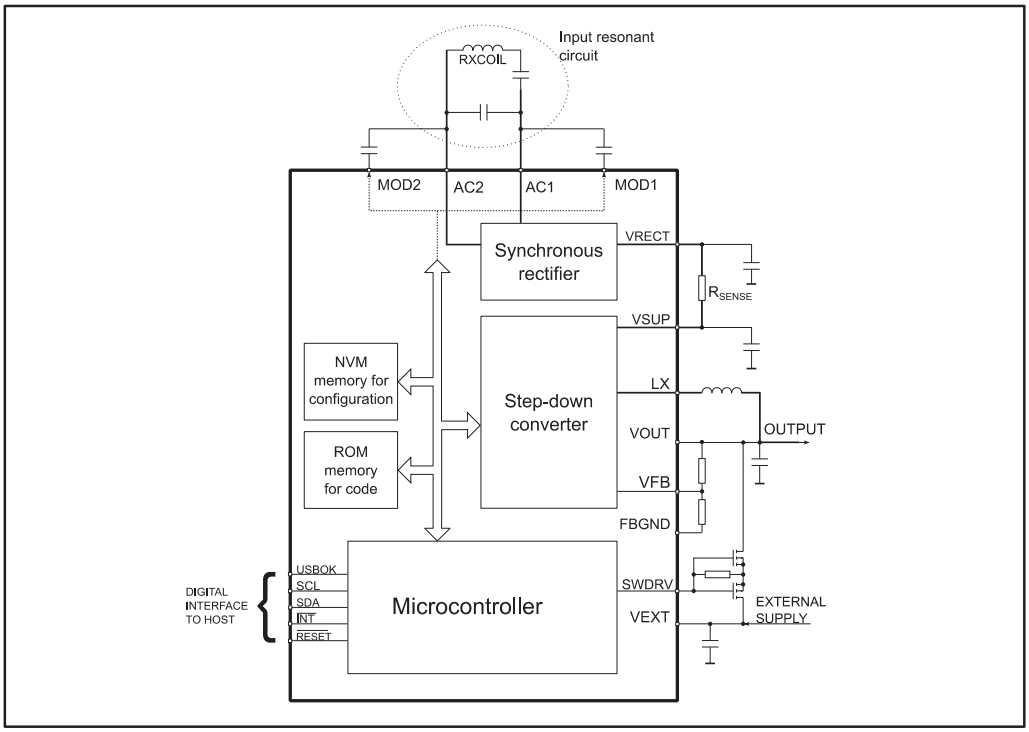
1 Introduction

The STWLC03 is a dual mode Qi/PMA wireless power receiver. It works as a voltage source with regulated output voltage, typically 5 V. It can be reconfigured into a simple battery charger mode (CC/CV) to charge directly Li-Ion or Li-Pol batteries. The STWLC03 can operate autonomously or can be controlled through I^2C by the host system.

Figure 1: Simplified block diagram



2 Pin configuration

Figure 2: Pin configuration Flip Chip 77 bumps (3.12x4.73 mm)

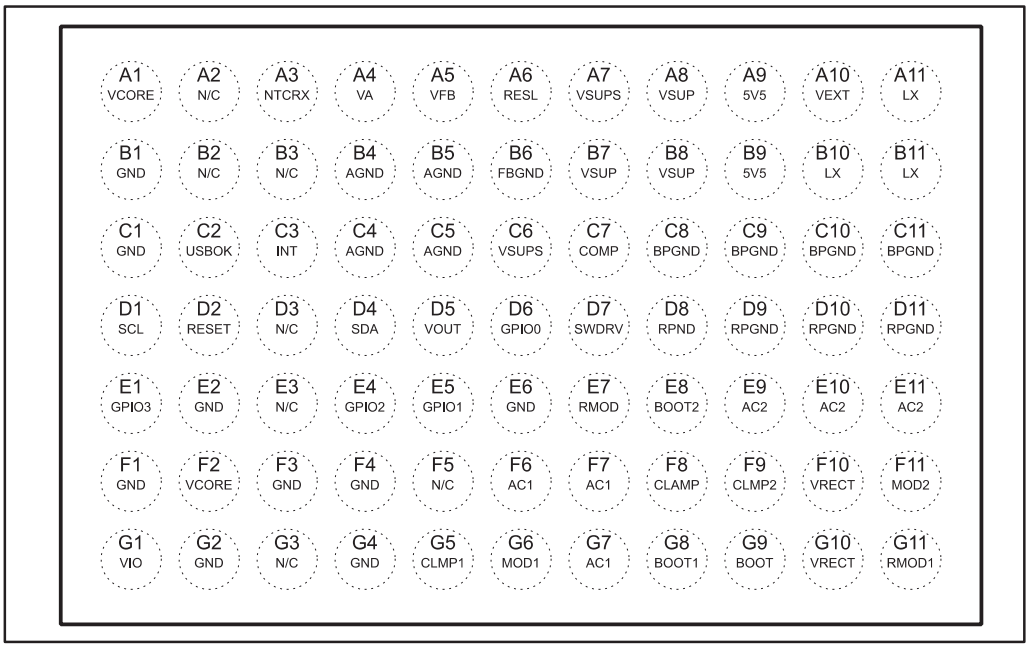


Table 2: Pin description

Pin name	Pin position	Description
AC1	F6, F7, G7	RX coil circuit terminal connection
AC2	E9, E10, E11	RX coil circuit terminal connection
MOD1	G6	Load modulation capacitor 1 connection
MOD2	F11	Load modulation capacitor 2 connection
CLMP1	G5	Clamping capacitor/resistor 1 connection
CLMP2	F9	Clamping capacitor/resistor 2 connection
RMOD	E7	Modulation current sink connection, internally connected to VRECT
RMOD1	G11	Load modulation external resistor connection. RM resistor is not necessary for most applications
VRECT	F10, G10	Synchronous rectifier output
BOOT1	G8	Bootstrap capacitor connection for the rectifier
BOOT2	E8	Bootstrap capacitor connection for the rectifier
BOOT	G9	Bootstrap capacitor connection for the step-down converter
CLAMP	F8	Low power clamp connection
VSUP	A8, B8, B7	Power supply input for the step-down converter
VSUPS	A7, C6	Sensing terminal of the external current sensing resistor

Pin name	Pin position	Description
RESL	A6	Sensing terminal of the external current sensing resistor
VOUT	D5	Step-down output voltage
VFB	A5	Step-down feedback input
FBGND	B6	Ground connection of the resistor feedback divider for step-down converter
LX	A11, B11, B10	Step-down converter coil connection
NTCRX	A3	Comparator input for RX coil temperature sensing
		NTC thermistor has to be placed close to RX coil
VA	A4	LDO1 output to filtering capacitor. ADC supply and sensitive analog circuitries are connected to this LDO; any external circuit cannot be connected to this node
VCORE	F2	LDO2 output to filtering capacitor. The microcontroller core and logic supply. VCORE voltage can be used as a reference voltage for the RX coil NTC divider
V5V	A9, B9	LDO3 output to filtering capacitor
VIO	G1	VIO power supply for the digital interface. It can be connected to VCORE or provided externally
SCL	D1	I^2C clock input
SDA	D4	I^2C data
GPIO0	D6	General purpose push-pull I/O pin. This function depends on firmware configuration
GPIO1	E5	General purpose push-pull I/O pin. This function depends on firmware configuration
GPIO2	E4	General purpose push-pull I/O pin. This function depends on firmware configuration
GPIO3	E1	Open drain output pin only. This function depends on firmware configuration
RESET	D2	Chip reset input, active low
INT	C3	Open drain interrupt output to the host platform
RPGND	D8, D9, D10, D11	Rectifier power ground
BPGND	C8, C9, C10, C11	Step-down converter power ground
GND	G2, F3	Digital ground
AGND	B4, C4, B5, C5	Analog ground
VEXT	A10	Detection of the external power supply voltage – adapter/USB voltage. 30 V spike tolerant
SWDRV	D7	External P-channel switch control for connecting adapter/USB voltage to VOUT
USBOK	C2	Digital input for the USBOK signal from platforms
COMP	C7	Step-down converter soft-start capacitor connection
GND	G4, F4	Reserved. Connect to ground
VCORE	A1	Reserved. Connect to VCORE

Pin name	Pin position	Description
N/C	G3	Reserved. Do not connect
GND	B1, E2, E6, F1	Reserved. Connect to ground
N/C	B2, B3, D3, E3	Reserved. Do not connect
GND	C1	Reserved. Connect to ground
N/C	A2, F5	Reserved. Do not connect

3 Maximum ratings

Table 3: Absolute maximum ratings

Pin	Parameter	Value	Unit
AC1, AC2	Input AC voltage	-0.3 to 20	V
MOD1, MOD2	Modulation transistor voltage	-0.3 to 20	V
CLMP1, CLMP2	Clamp transistor voltage	-0.3 to 20	V
BOOT1, BOOT2	Voltage on bootstraps	AC1, AC2 -0.3; AC1, AC2 + 6	V
BOOT	Voltage on bootstrap	VRECT-0.3; VRECT + 6	V
VRECT	Rectified voltage	-0.3 to 20	V
VRESL, VSUPS	Current sensing resistor connection voltage	-0.3 to 20	V
VRESL-VSUPS	Voltage on the current sensing resistor	-0.3 to 2	V
VSUP	Input voltage of the buck converter	-0.3 to 20	V
LX	Buck converter switching node voltage	-0.3 to 20	V
RMOD, RMOD1	Resistive modulation current source and transistor voltage	-0.3 to 20	V
FBGND	Internal feedback transistor VDS voltage	-0.3 to 20	V
VOUT	Output voltage range	-0.3 to 20	V
VFB	Buck converter feedback voltage	-0.3 to 3	V
VEXT, SWDRW	Detection pin for the external voltage and driver output for the external transistor	-0.3 to 30	V
NTCRX	RX coil NTC voltage	-0.3 to 2.3	V
VA, VCORE	LDO1,2 voltages	-0.3 to 2.3	V
V5V	LDO 3 voltage	-0.3 to 6	V
VIO	VIO voltage	-0.3 to 6	V
SCL, SDA, USBOK, INT, RESET	Digital interface voltage	-0.3 to VIO+0.3	V
GPIO0, GPIO1, GPIO2, GPIO3	General purpose I/O voltage	-0.3 to VIO+0.3	V
T_{STG}	Storage temperature range	-40 to 150	°C
T_{OP}	Operating ambient temperature range	-40 to +85	°C
T_J	Maximum junction temperature	+125	°C
ESD	Machine model	±100	V
	Charged device model	±500	V
	Human body model	±2000	V

Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

Table 4: Thermal data

Package	Symbol	Parameter	Value	Unit
Flip Chip 77 (3.12x4.73 mm)	R_{THJA}	Junction-to-ambient thermal resistance(1)	35	°C/W

Notes:

(1)This parameter corresponds to the PCB board, 4-layer with 1 inch^2 of cooling area.

4 Electrical characteristics

-30 °C < T_A < 85 °C; typical values are at T_A = 25 °C, unless otherwise specified.

Table 5: Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
General section						
V_{IN}	AC input voltage	Peak-to-peak voltage between AC1- AC2 over the period			32	V
V_{UVLO}	Undervoltage lockout threshold	V_{SUP} rising		3.6	3.8	V
		V_{SUP} falling	3.3	3.5		
$TIMEOUT_{RESET}$	Reset time-out for shutdown mode			1		ms
IQ	Current consumption in the shutdown mode	RESET=0 (active low) duration>1 ms, measured at VEXT		10		µA
		RESET=0 (active low) duration>1 ms, measured at VRECT		2	4	mA
I_{RESET}	Current consumption in the RESET condition	RESET=0 (active low), duration<1 ms, GPIO 0 floating		5		mA
I_{CC}	Current consumption of the device	RESET=1 (inactive), GPIO 0 floating		7		mA
LDO 1						
V_A	LDO 1 output voltage	I_A = 5 mA		1.8		V
I_{ILIM}	Load current limit			50		mA
LDO 2						
V_{CORE}	LDO 2 output voltage	V_{SUP} = 3.6 V to 11 V, I_{CORE} = 5 mA		1.8		V
I_{DDLIM}	Load current limit			40		mA
LDO 3						
V_{5V}	LDO 3 output voltage	I_{V5V} = 20 mA, V_R = 5.5 V		5		V
I_{ILIM}	Load current limit			30		mA
Synchronous rectifier						

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$R_{DS(on)}$	Drain-source NMOS on-resistance low-side	I_{RECT} = 1.4 A, V_{RECT} = 8 V		90		mΩ
	Drain-source NMOS on-resistance high-side			70		
Efficiency	Rectifier efficiency	I_{RECT} = 0.8 A, V_{RECT} = 7 V, $f_{Rectifier}$ = 130 kHz		91		%
IRACTIVE	Active mode rectifier threshold, voltage @ Rs	V_{RECT} = 10 V, rising edge		8.75		mV
		V_{RECT} = 10 V, falling edge		3.25		
$f_{RECTIFIER}$	Rectifier frequency range		50		500	kHz
V_{CLAMP}	Clamp of the rectified voltage	I_{CLAMP} = 1 mA		17.4		V
Active clamp drivers						
$R_{DS(on)CLMP1,2}$	Active clamp MOS $R_{DS(on)}$	V_{SUP} = 5 V		1		Ω
V_{OVP}	V_{RECT} voltage threshold of active clamp		15.4	15.9	16.4	V
$V_{OVP\ hyst}$	V_{RECT} voltage active clamp hysteresis			600		mV
Load modulation						
$R_{DS(on)MOD1,2}$	Load modulation MOS $R_{DS(on)}$	V_{SUP} = 5 V		1		Ω
I_{MOD}	R_{MOD} pin sink current range	V_{SUP} = 5 V	15		410	mA
	Modulation current tolerance	V_{SUP} = 5 to 12 V, I_{MOD} = 80 mA		10		%
$I_{MAXMOD1}$		V_{SUP} = 5 V, R_M = 2 Ω		2		A
Protections						
$VLD_{MAX.}$	Overcurrent protection threshold, voltage @ R_S	VLD_{MAX} = 0Fh		1.7		V
	VLD_{MAX} = 04h			0.875		
TOL_VLD_{MAX}	Tolerance of the VLD_{MAX}	VLD_{MAX} = 0Fh	-5		+5	%
	VLD_{MAX} = 04h		-10		+10	

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{NTCTRIG}$	NTC trigger voltage for RX			0.6		V
TOL_$V_{NTCTRIG}$	NTC trigger voltage tolerance			3		%
Hyst_$V_{NTCTRIG}$	NTC trigger voltage hysteresis			100		mV
t_{SHDN}	Thermal shutdown			150		°C
$t_{SHDNHYST}$	Thermal shutdown hysteresis			20		°C
Current-to-voltage converter						
EOC_CURRENT	End-of-charge current threshold	R_S = 0.05 Ω 1%, V_{SUP} = 5 to 15 V	0		400	mA
$TOL_{EOC\_CURRENT}$	Tolerance of the EOC threshold	R_S = 0.05 Ω 1%, V_{SUP} = 5 to 15 V, EOC_CURRENT = 50 mA		20		%
		R_S = 0.05 Ω 1%, V_{SUP} = 5 to 15 V, EOC_CURRENT = 200 mA		10		%
Step-down converter						
V_{VOUT}	Output voltage range		3		7	V
Tol_{VOUT}	VOUT tolerance	VOUTreg = 011, VOUT = 4.2 V		0.5		%
OVP_{VOUT}	Overvoltage protection threshold			8.5		V
I_{VOUT} + I_{FB}	Output leakage current	Step-down is off, VOUT = 5 V,			1	µA
I_{FB}	Feedback pin bias current				500	nA
I_{LIM}	Coil current limit		250		4000	mA
	Coil current limit accuracy	CURRLIM reg = 1111		10		%
$I_{OVERCURR}$	Overcurrent/short-circuit protection	V_{SUP} = 5 to 12 V		4500		mA
DIV_{VOUT}	Output voltage internal divider ratio			6		nA
f_{SW}	Switching frequency			0.8		MHz
V_{SUP}	Input voltage range	I_{OUT} = 2 A	5.5		12	V

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
N-$R_{DS(on)SW}$	NMOS $R_{DS(on)}$ high-side	Back-to-back connected transistors		130		mΩ
N-$R_{DS(on)SW}$	NMOS $R_{DS(on)}$ low-side			60		mΩ
Efficiency	Step-down efficiency	POUT = 5 W		89		%
		POUT = 12 W		80		
R_{FBGND}	VOUT feedback divider grounding switch resistance	I_{FBGND} = 500 µA			40	Ω
t_{START}	Buck converter soft-start time	C_{10} = 1 µF, P_{LOAD} = 0 to 12 W		1		s
Input voltage loop for output power limiting						
VRMIN	Minimum rectified voltage threshold for output power limitation	VRMIN = 00h		5		V
		VRMIN = 0Ah		7		
TOL_{VRMIN}	VRMIN threshold tolerance			5		%
Input current limitation loop						
IRREG	Input current limitation threshold, voltage @ R_s	IRREG = F6h		82.5		mV
		IRREG = 32h		17.55		
TOL_{IRREG}	IRREG threshold tolerance	IRREG = F6h		5		%
		IRREG = 32h		10		
External voltage switch driver						
$V_{EXTUVLO}$	External supply undervoltage threshold		4.2	4.4	4.6	V
V_{EXTOVP}	External supply overvoltage threshold		5.25	5.55	5.9	V
$I_{EXTCONS}$	Input consumption current	VEXT = 5 V, VRECT = 0 V, RESET = 1 (active low)		8		mA
V_{SWDRV}	Switch driver voltage drop	VEXT = 5 V, SWDRV low		200		mV
GPIO pins						
$IOUT_{GPIO0/1/2}$	GPIO pin current capability	GPIO0/1/2 high, V_{IO} = 1.8 V, $V_{GPIO0/1/2}$ = 1.4 V	3			mA

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{GPIO0/1/2/3}$	GPIO pin drop	GPIO0/1/2/3 low, V_{IO} = 1.8 V, $I_{GPIO0/1/2}$ = 3 mA		360		mV
V_{IL}	Low level input voltage				0.3*VIO	V
V_{IH}	High level input voltage		0.7*VIO			V
Microcontroller						
Architecture				32		bit
NVM	Memory size for customization			2		kbit
Clock generator						
f_{OSC}	Clock generator frequency	V_{SUP} = 4.5 to 15 V		16		MHz
TOL_{FOSC}	Tolerance of the clock generator frequency	T_{AMB} = 0 °C to 85 °C	-4		+4	%

5 Device description

5.1 Using the STWLC03 as a power supply

The STWLC03 is configured as a power supply with 5 V output voltage by default. Output voltage can be adjusted in 8 steps in runtime through I²C or as a new default start-up configuration in NVM. Output voltage can be also slightly fixed in the range among the software steps, by tuning the resistor feedback divider.

When the output voltage changes, the related parameters have to be taken into account: rectified voltage V_{RECT} and input voltage threshold for output limitation V_{RMIN}. The table below shows the recommended values.

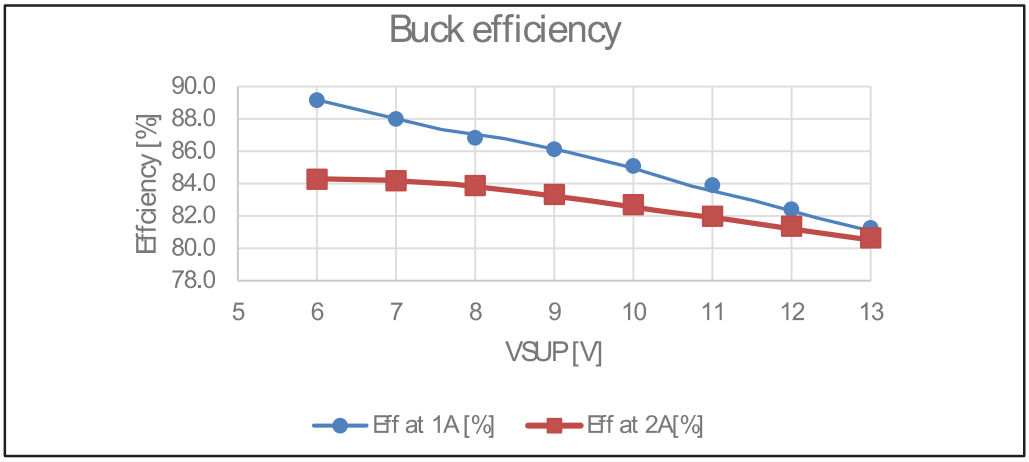
Table 6: Recommended VRECT and VRMIN values for various VOUT

Parameter	Min.	Typ.	Max.
VOUT	5 V	6 V	7 V
VRECT	7 V	8 V	9 V
VRMIN	5.6 V	5.6 V	5.6 V

Input current limit and overload threshold should be fixed according to maximum expected peak load in the application.

The STWLC03 monitors continuously the rectifier current. If the current drops below the defined threshold for the defined time, the power transfer is over. This configuration is stored in NVM, values Qi_EPT_Threshold, Qi_EPT_Time, PMA_EOC_Threshold, PMA_EOC_Time. This configuration is common for power supply mode and battery charger mode. To avoid power transfer termination, zero-current and maximum time have to be fixed.

Figure 3: Typical step-down converter efficiency



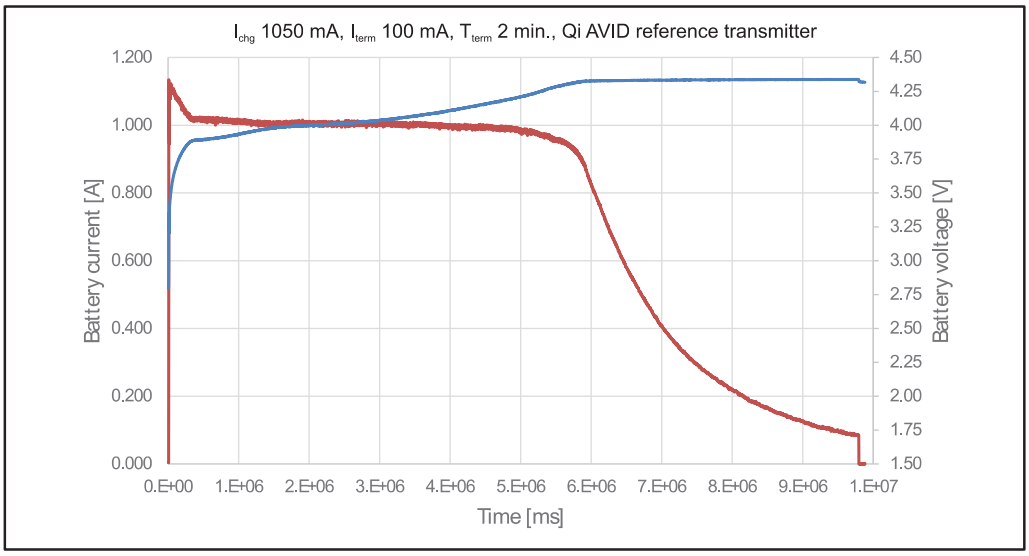
5.2 Using the STWLC03 as a battery charger

The STWLC03 is equipped with a software feature allowing the input current limitation loop to control the charging current. In this manner the STWLC03 can operate as a CC/CV

charger without HW output current control loop. VOUT pin leakage is minimized to save battery operation time.

The STWLC03 can be switched to battery charger mode instantly by I²C register (evaluation only, not recommended for production) or as a new default start-up configuration in NVM (safe recommended solution).

Figure 4: Typical charging profile

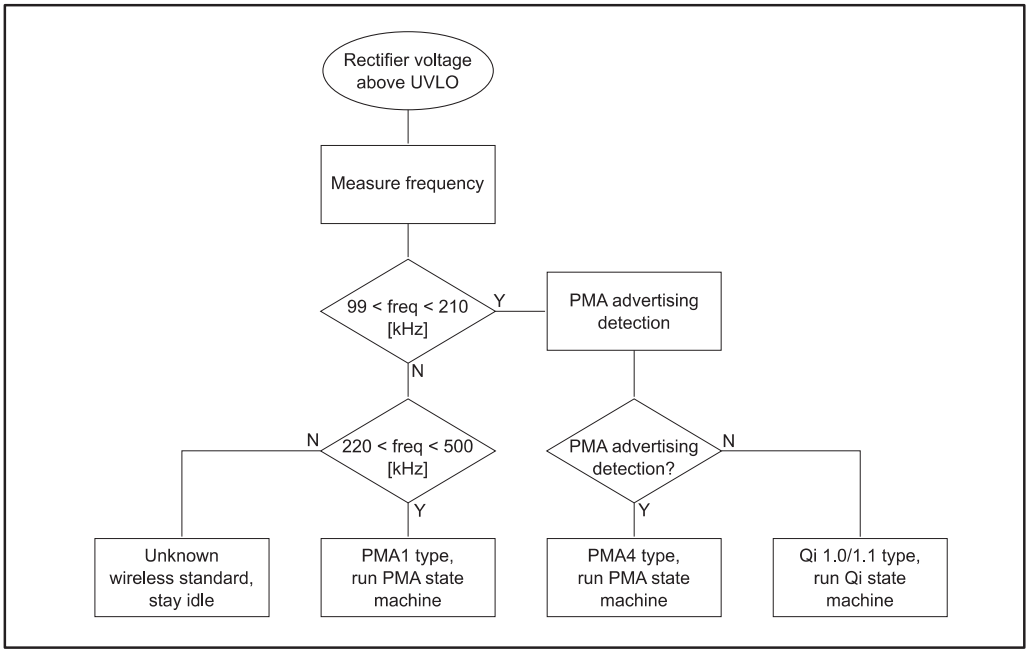


Thanks to very low leakage from VOUT pin, the STWLC03 can remain connected to the battery and does not cause any discharge.

5.3 Wireless standard auto-detection

The STWLC03 automatically detects the operating standard when it is placed on a wireless transmitter. Detection is based on combination of operating frequency and receiving FSK signaling from the transmitter.

Figure 5: Wireless standard detection flowchart



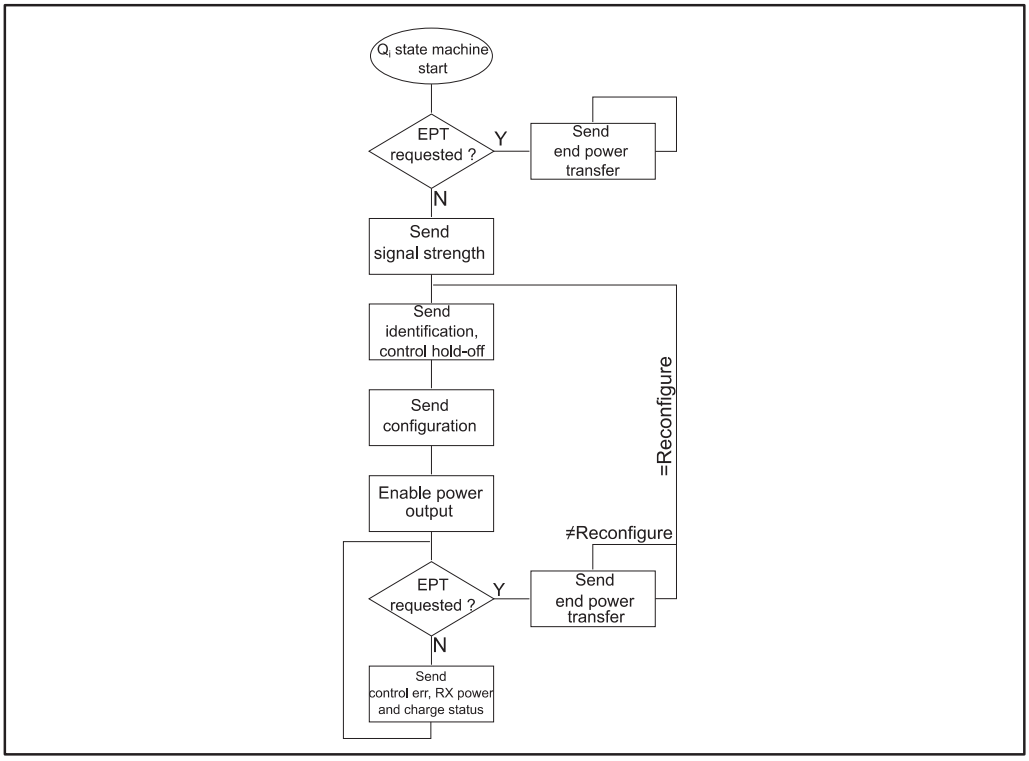
The STWLC03 can be also configured to skip the auto-detection and use directly the pre-configured wireless standard.

5.4 Qi operation and flow chart

The STWLC03 follows Qi 1.1.2 version.

When Qi state machine starts, it proceeds through ping and identification and configuration phases to power transfer phase according to Qi wireless power transfer, volume I: low power 1.1.2 specification.

Figure 6: Qi simplified flow diagram



End-power-transfer can be requested because of the following reasons:

Table 7: EPT reasons in Qi

Reason	EPT code
I²C “Force EPT” bit set	Unknown (00h)
VEXT above UVLO	
USBOK digital input	
Termination current reached	Charge complete (01h)
Charger in unexpected state	Internal fault (02h)
Step-down overload	
Step-down output overvoltage	
Rx coil NTC above threshold	Overtemperature (03h)
Chip temperature above threshold	
Rectifier output overvoltage	Overvoltage (04h)
Rectifier output overcurrent	Overcurrent (05h)
Charger output voltage above threshold	Battery failure (06h)
I²C “Reconfigure” bit set	Reconfigure (07h)

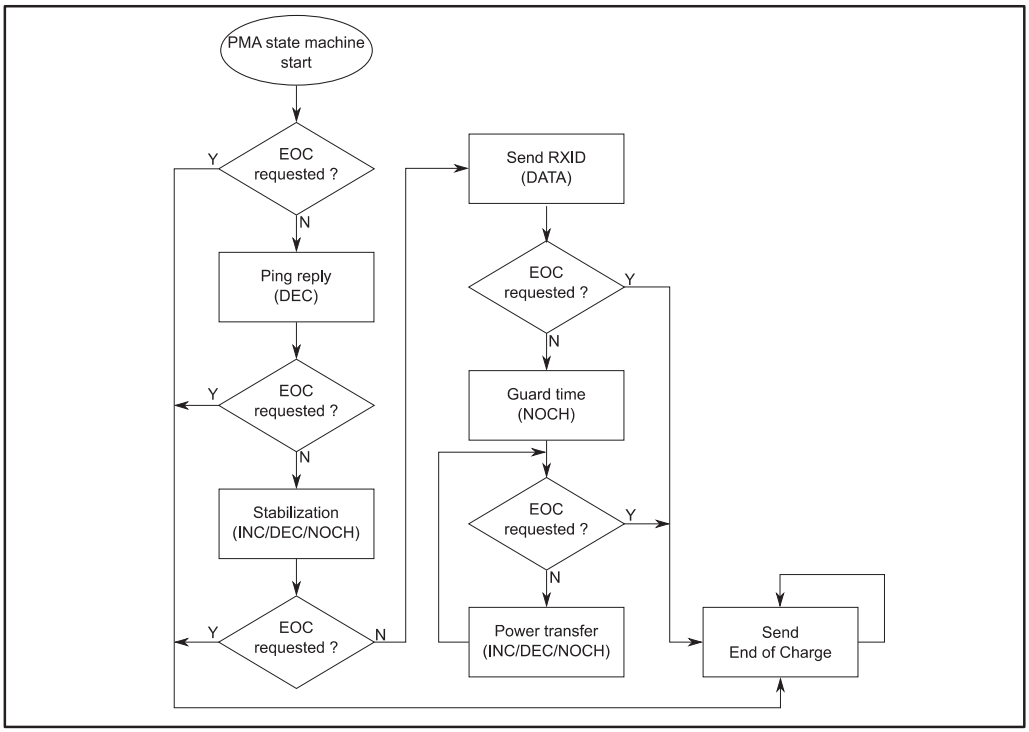
5.4.1 Received power calibration (FOD feature)

Although the STWLC03 is well-trimmed, inaccuracy in the received power estimation can be caused in the target application due to manufacturing different environment conditions. Different serial resistances of used receiver coil or different shieldings of the receiver coil (e.g. battery or ground plane in a near proximity of the coil) are the main issues. The STWLC03 features dedicated adjustment options placed in NVM.

5.5 PMA operation

The STWLC03 follows PMA1 SR1 specification. When PMA state machine starts, it proceeds through ping and identification phase to power transfer phase according to PMA inductive wireless power and charging receiver specifications, system release 1.

Figure 7: PMA simplified flow diagram



End-of-charge can be requested due to the following reasons:

Table 8: EOC reasons in PMA

Reasons
I^2C “Force EOC” bit set
VEXT above UVLO
USBOK digital input
Termination current reached
Charger in unexpected state
Step-down overload
Step-down output overvoltage
Rx coil NTC above threshold
Chip temperature above threshold
Rectifier output overvoltage
Rectifier output overcurrent
Charger output voltage above threshold

5.6 External power supply

Figure 8: "External power supply situation" illustrates the situation where the STWLC03 detects the external voltage presence and drives SWDRV (external voltage) to the output. The STWLC03 also terminates the wireless power transfer.

Figure 9: "External power supply situation 1" illustrates the situation where the STWLC03 is assembled in a system with another PMIC that serves multiple power supply inputs. PMIC uses digital line to let the STWLC03 know that there is a higher priority power supply available and the wireless power transfer should be terminated.

For proper operation, RESETn pin must be high. Connecting VEXT power supply, consumption from VIO increases if VIO supply is provided externally. (It has not effect if VIO is connected to VCORE).

Figure 8: External power supply situation

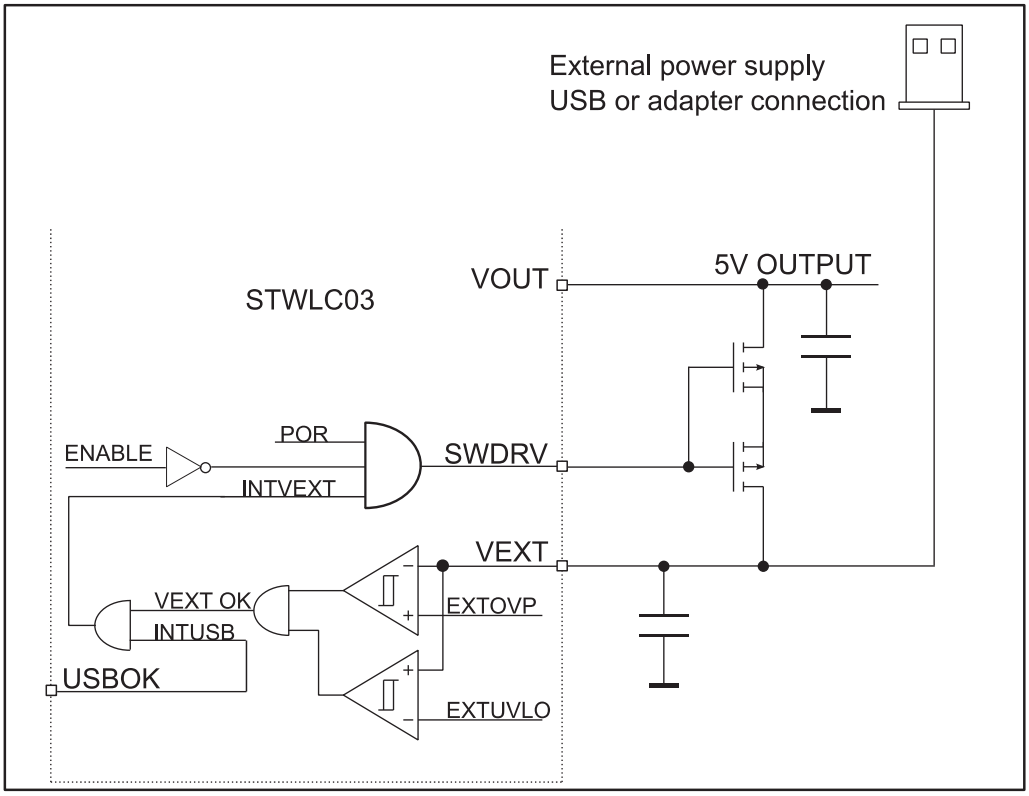
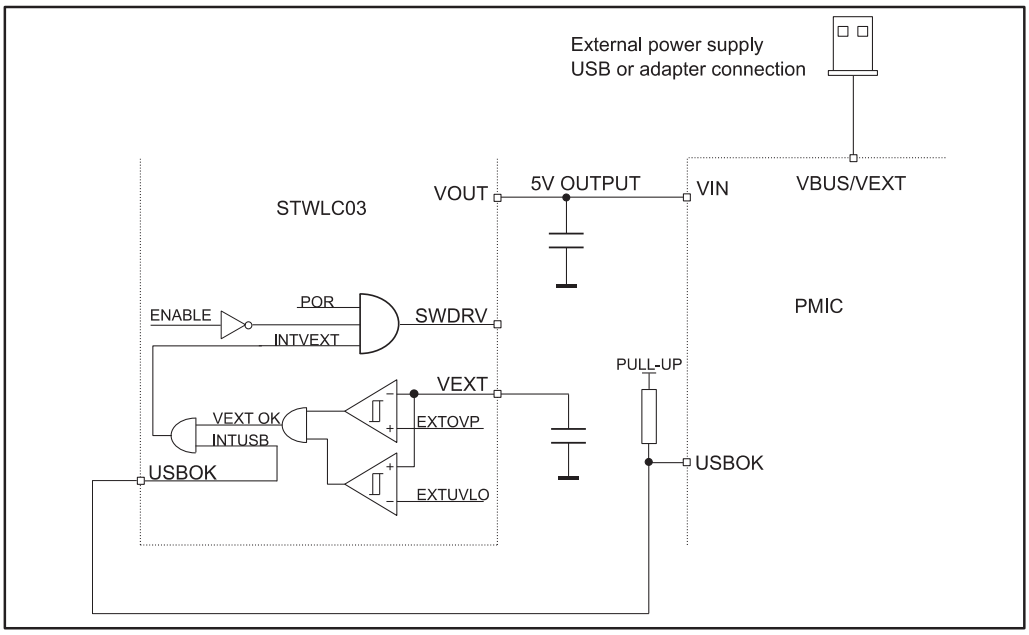


Figure 9: External power supply situation 1



5.7 The device interface

The STWLC03 is equipped with I²C interface with an open-drain interrupt line to connect with the host system. If I²C connection is not used by the host platform, SDA and SCL lines should be pulled-up to VIO voltage. The STWLC03 contains RESETn input. The device under reset conditions has very low power consumption. If reset is not controlled by the host platform it should be pulled-up to VIO voltage. USBOK is a digital input, which terminates power transfer if another preferred power supply is available. The STWLC03 features GPIO pins. By default GPIO 0 only is active and detects power transfer state on wireless interface.

6 I²C register description

The device I²C address is 14h (0010100b).

Table 9: User register map

Address	Register
00h	Control
01h	Reserved
02h	Target rectified voltage
03h	Input voltage threshold for output limitation
04h	Reserved
05h	Input current limit
06h	Overload threshold
07h	Buck output voltage
08h	Buck current limit
09h	Chip overtemperature
0Ah	Interrupt mask L
0Bh	Interrupt mask H
0Ch	Interrupt status L
0Dh	Interrupt status H
0Eh	Interrupt latch L
0Fh	Interrupt latch H
10h	Operation mode detection status
11h	Operation mode detection control
12h	Qi charge status packet content
13h	Charger status
14h	Charger control

Table 10: Control register

b7	b6	b5	b4	b3	b2	b1	b0	
Force/EPT	Disable/EPT on error	Qi reconfigure	-	-	-	-	USBcon_cnf	R/W
Loaded from NVM at startup								Default

USBcon_cnf:

0: auto connect switch + disable buck + send EPT@VEXT/disable buck + send EPT@USBOK

1: ignore VEXT/USBOK completely

Qi reconfigure:

0: no action