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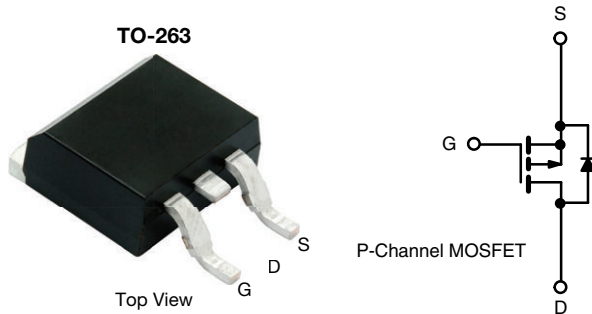


## P-Channel 60 V (D-S) 175 °C MOSFET

PRODUCT SUMMARY		
V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A) <sup>d</sup>
-60	0.0069 at V <sub>GS</sub> = -10 V	-110
	0.0088 at V <sub>GS</sub> = -4.5 V	

### FEATURES

- TrenchFET® power MOSFET
- Package with low thermal resistance
- Material categorization:  
for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)


**RoHS**  
COMPLIANT


### Ordering Information:

SUM110P06-07L-E3 (Lead (Pb)-free)

ABSOLUTE MAXIMUM RATINGS (T <sub>C</sub> = 25 °C, unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V <sub>DS</sub>	-60	V
Gate-Source Voltage	V <sub>GS</sub>	± 20	
Continuous Drain Current <sup>d</sup> (T <sub>J</sub> = 175 °C)	I <sub>D</sub>	T <sub>C</sub> = 25 °C	-110
		T <sub>C</sub> = 125 °C	-95
Pulsed Drain Current	I <sub>DM</sub>	-240	A
Avalanche Current	I <sub>AS</sub>	-75	
Single Pulse Avalanche Energy <sup>a</sup>	E <sub>AS</sub>	281	
Power Dissipation	P <sub>D</sub>	T <sub>C</sub> = 25 °C <sup>c</sup>	375
		T <sub>A</sub> = 25 °C <sup>b</sup>	3.75
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	°C

THERMAL RESISTANCE RATINGS			
PARAMETER	SYMBOL	TYPICAL	UNIT
Junction-to-Ambient	R <sub>thJA</sub>	40	°C/W
Junction-to-Case	R <sub>thJC</sub>	0.4	

### Notes

- Duty cycle ≤ 1 %.
- When mounted on 1" square PCB (FR4 material).
- See SOA curve for voltage derating.
- Limited by package.



SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = -250 μA	-60	-	-	V
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250 μA	-1	-	-3	
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V	-	-	± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = -60 V, V <sub>GS</sub> = 0 V	-	-	-1	μA
		V <sub>DS</sub> = -60 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C	-	-	-50	
		V <sub>DS</sub> = -60 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 175 °C	-	-	-250	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> = -5 V, V <sub>GS</sub> = -10 V	-120	-	-	A
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = -10 V, I <sub>D</sub> = -30 A	-	0.0055	0.0069	Ω
		V <sub>GS</sub> = -10 V, I <sub>D</sub> = -30 A, T <sub>J</sub> = 125 °C	-	-	0.0115	
		V <sub>GS</sub> = -10 V, I <sub>D</sub> = -30 A, T <sub>J</sub> = 175 °C	-	-	0.0138	
		V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -20 A	-	0.0070	0.0088	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = -15 V, I <sub>D</sub> = -50 A	20	-	-	S
<b>Dynamic <sup>b</sup></b>						
Input Capacitance	C <sub>ISS</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = -25 V, f = 1 MHz	-	11 400	-	pF
Output Capacitance	C <sub>OSS</sub>		-	1200	-	
Reverse Transfer Capacitance	C <sub>RSS</sub>		-	900	-	
Total Gate Charge <sup>c</sup>	Q <sub>g</sub>	V <sub>DS</sub> = -30 V, V <sub>GS</sub> = -10 V, I <sub>D</sub> = -110 A	-	230	345	nC
Gate-Source Charge <sup>c</sup>	Q <sub>gs</sub>		-	50	-	
Gate-Drain Charge <sup>c</sup>	Q <sub>gd</sub>		-	60	-	
Gate Resistance	R <sub>g</sub>	f = 1 MHz	-	3	-	Ω
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>	V <sub>DD</sub> = -30 V, R <sub>L</sub> = 0.27 Ω I <sub>D</sub> ≅ -110 A, V <sub>GEN</sub> = -10 V, R <sub>g</sub> = 1 Ω	-	20	30	ns
Rise Time <sup>c</sup>	t <sub>r</sub>		-	25	40	
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>		-	110	200	
Fall Time <sup>c</sup>	t <sub>f</sub>		-	50	100	
<b>Drain-Source Body Diode Characteristics (T<sub>C</sub> = 25 °C <sup>b</sup>)</b>						
Continuous Current	I <sub>S</sub>		-	-	-110	A
Pulsed Current	I <sub>SM</sub>		-	-	-240	
Forward Voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>F</sub> = -85 A, V <sub>GS</sub> = 0 V	-	-1	-1.5	V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = -85 A, di/dt = 100 A/μs	-	91	137	ns
Peak Reverse Recovery Charge	I <sub>RM(REC)</sub>		-	-6	-9	A
Reverse Recovery Charge	Q <sub>rr</sub>		-	0.21	0.44	μC

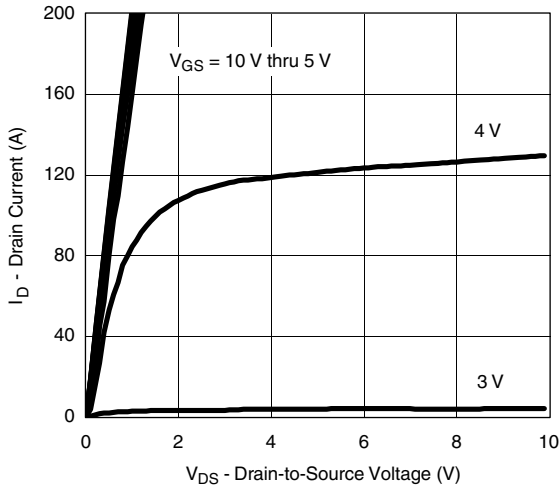
**Notes**

- Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
- Guaranteed by design, not subject to production testing.
- Independent of operating temperature.

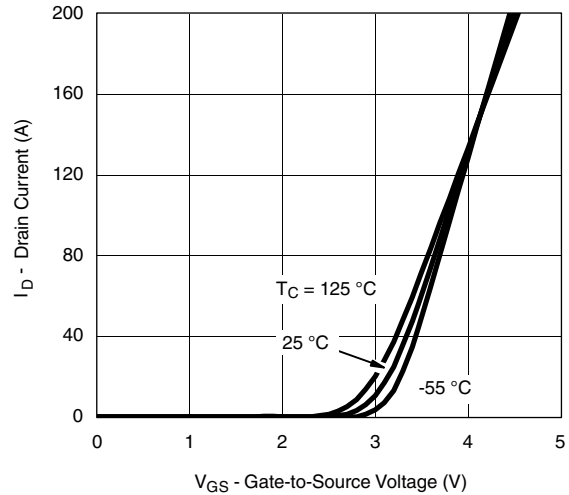
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.



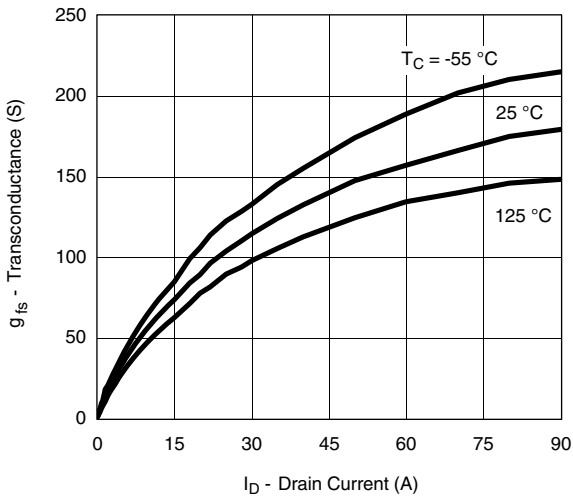
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



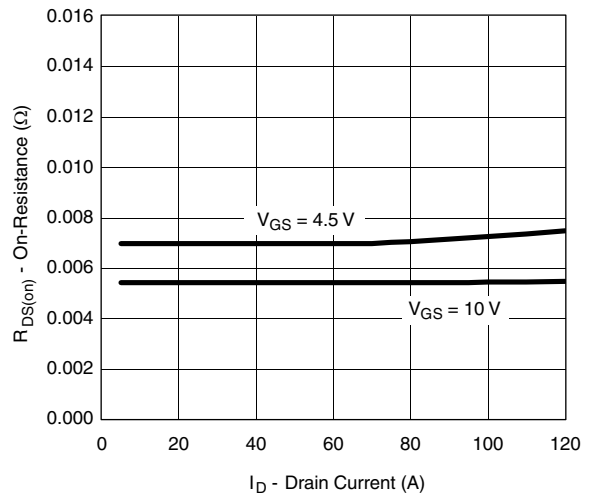
Output Characteristics



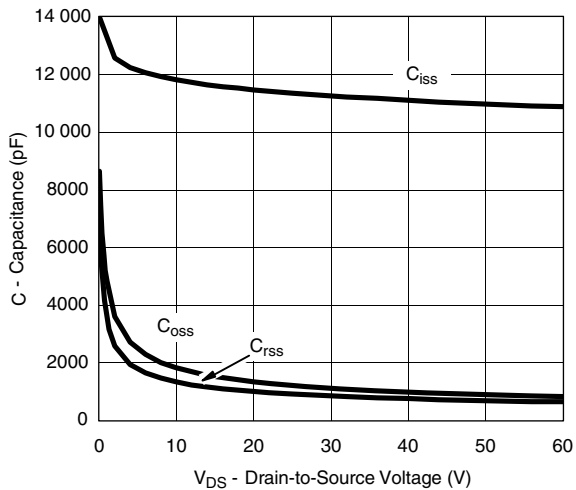
Transfer Characteristics



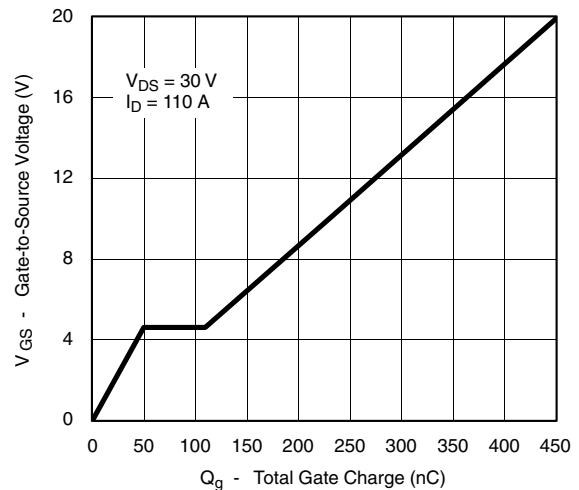
Transconductance



On-Resistance vs. Drain Current



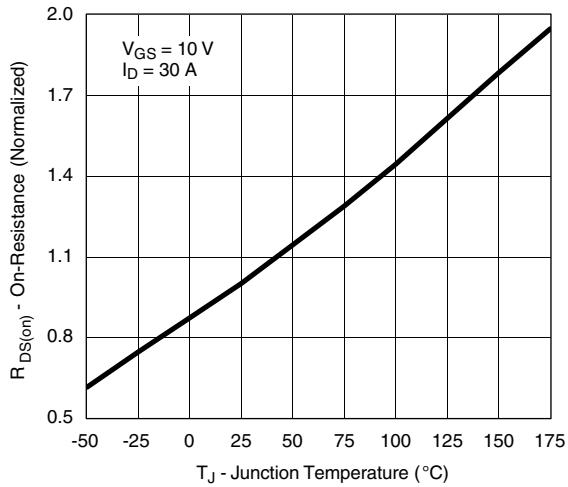
Capacitance



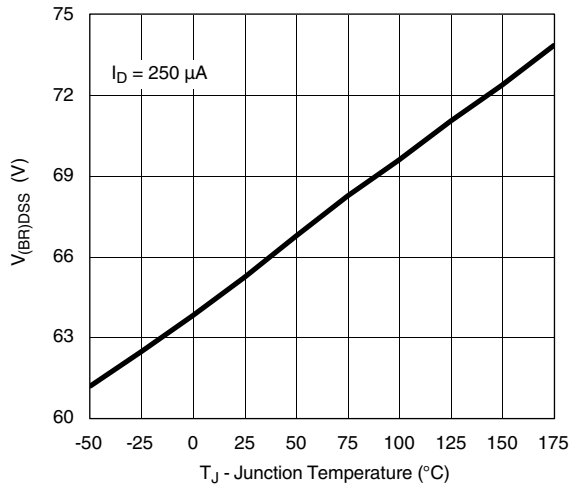
Gate Charge



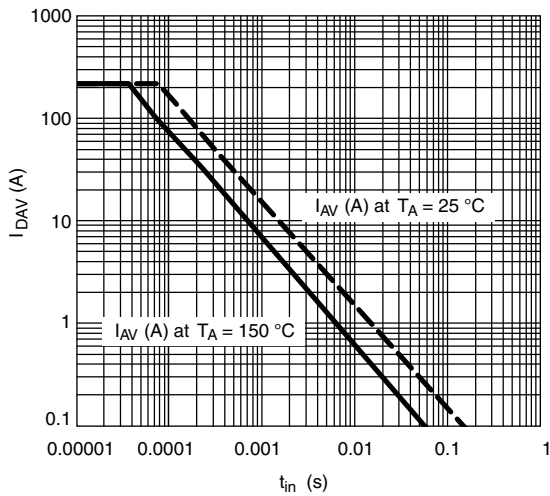
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



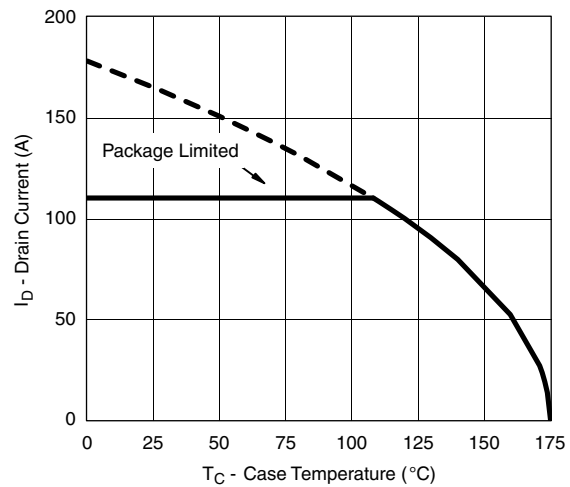
On-Resistance vs. Junction Temperature



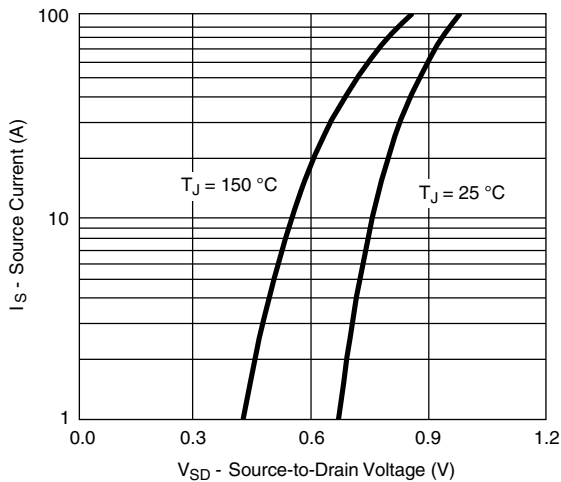
Drain Source Breakdown vs. Junction Temperature



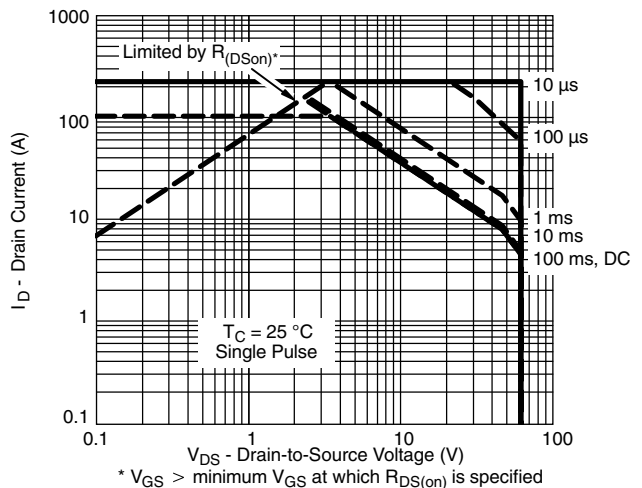
Avalanche Current vs. Time



Maximum Avalanche and Drain Current vs. Case Temperature



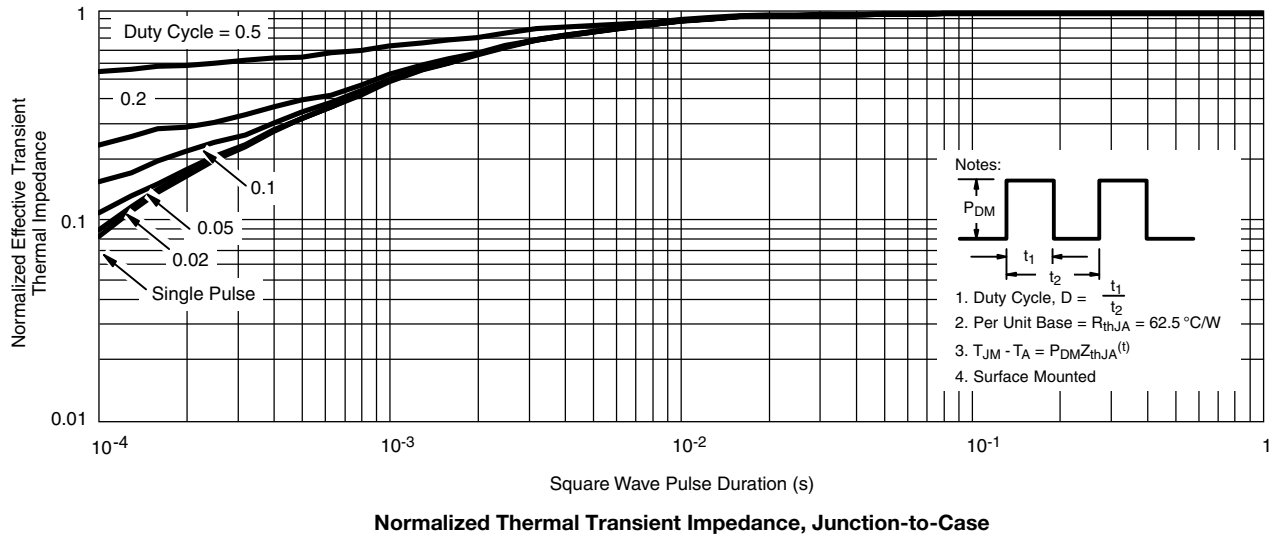
Source-Drain Diode Forward Voltage



Safe Operating Area

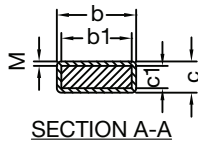
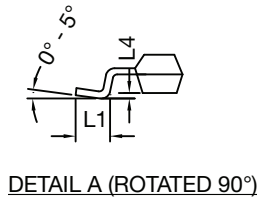
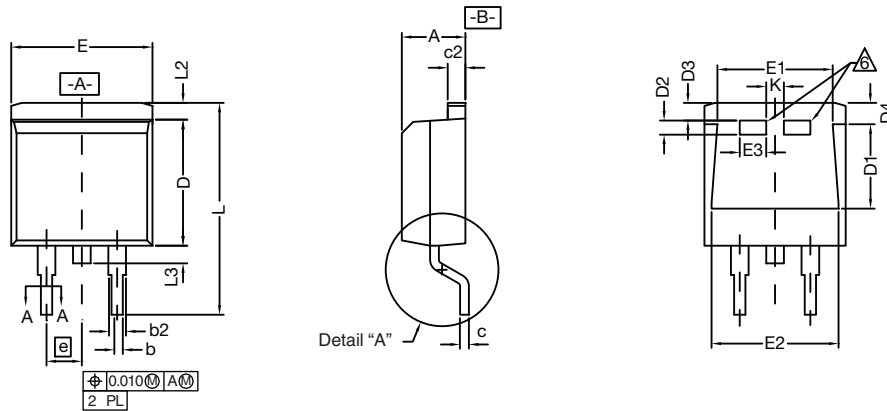


TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



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### TO-263 (D<sup>2</sup>PAK): 3-LEAD

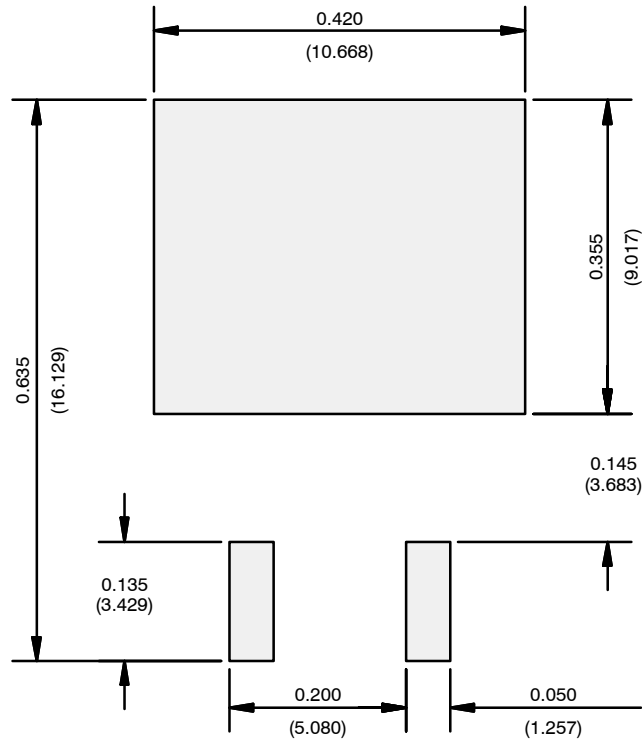


DIM.	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	
A	0.160	0.190	4.064	4.826	
b	0.020	0.039	0.508	0.990	
b1	0.020	0.035	0.508	0.889	
b2	0.045	0.055	1.143	1.397	
c*	Thin lead	0.013	0.018	0.330	0.457
	Thick lead	0.023	0.028	0.584	0.711
c1	Thin lead	0.013	0.017	0.330	0.431
	Thick lead	0.023	0.027	0.584	0.685
c2	0.045	0.055	1.143	1.397	
D	0.340	0.380	8.636	9.652	
D1	0.220	0.240	5.588	6.096	
D2	0.038	0.042	0.965	1.067	
D3	0.045	0.055	1.143	1.397	
D4	0.044	0.052	1.118	1.321	
E	0.380	0.410	9.652	10.414	
E1	0.245	-	6.223	-	
E2	0.355	0.375	9.017	9.525	
E3	0.072	0.078	1.829	1.981	
e	0.100 BSC		2.54 BSC		
K	0.045	0.055	1.143	1.397	
L	0.575	0.625	14.605	15.875	
L1	0.090	0.110	2.286	2.794	
L2	0.040	0.055	1.016	1.397	
L3	0.050	0.070	1.270	1.778	
L4	0.010 BSC		0.254 BSC		
M	-	0.002	-	0.050	
ECN: T13-0707-Rev. K, 30-Sep-13					
DWG: 5843					

**Notes**

- Plane B includes maximum features of heat sink tab and plastic.
- No more than 25 % of L1 can fall above seating plane by max. 8 mils.
- Pin-to-pin coplanarity max. 4 mils.
- \*: Thin lead is for SUB, SYB.  
Thick lead is for SUM, SYM, SQM.
- Use inches as the primary measurement.
- This feature is for thick lead.

**RECOMMENDED MINIMUM PADS FOR D<sup>2</sup>PAK: 3-Lead**



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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