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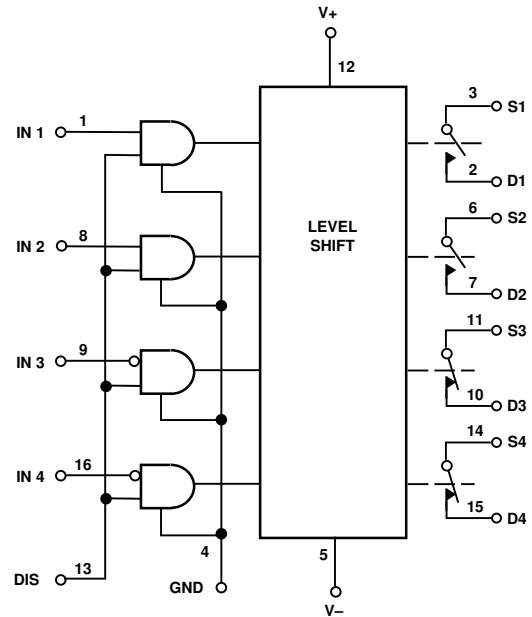
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



### FEATURES

- Two Normally Open and Two Normally Closed SPST Switches with Disable
- Switches Can Be Easily Configured as a Dual SPDT or a DPDT
- Highly Resistant to Static Discharge Destruction
- Higher Resistance to Radiation than Analog Switches Designed with MOS Devices
- Guaranteed  $R_{ON}$  Matching: 10% max
- Guaranteed Switching Speeds
  - $T_{ON} = 500$  ns max
  - $T_{OFF} = 400$  ns max
- Guaranteed Break-Before-Make Switching
- Low "ON" Resistance:  $80 \Omega$  max
- Low  $R_{ON}$  Variation from Analog Input Voltage: 5%
- Low Total Harmonic Distortion: 0.01%
- Low Leakage Currents at High Temperature
  - $T_A = +125^\circ\text{C}$ : 100 nA max
  - $T_A = +85^\circ\text{C}$ : 30 nA max
- Digital Inputs TTL/CMOS Compatible and Independent of  $V_+$
- Improved Specifications and Pin Compatible to LF-11333/13333
- Dual or Single Power Supply Operation
- Available in Die Form

### FUNCTIONAL BLOCK DIAGRAM



### GENERAL DESCRIPTION

The SW06 is a four channel single-pole, single-throw analog switch that employs both bipolar and ion-implanted FET devices. The SW06 FET switches use bipolar digital logic inputs which are more resistant to static electricity than CMOS devices. Ruggedness and reliability are inherent in the SW06 design and construction technology.

Increased reliability is complemented by excellent electrical specifications. Potential error sources are reduced by minimizing "ON" resistance and controlling leakage currents at high temperatures. The switching FET exhibits minimal  $R_{ON}$  variation over a 20 V analog signal range and with power supply voltage changes. Operation from a single positive power supply voltage is possible. With  $V_+ = 36$  V,  $V_- = 0$  V, the analog signal range will extend from ground to +32 V.

PNP logic inputs are TTL and CMOS compatible to allow the SW06 to upgrade existing designs. The logic "0" and logic "1" input currents are at microampere levels reducing loading on CMOS and TTL logic.

### REV. A

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# SW06\* PRODUCT PAGE QUICK LINKS

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## COMPARABLE PARTS

View a parametric search of comparable parts.

## DOCUMENTATION

### Data Sheet

- SW06: Quad SPST JFET Analog Switch Data Sheet
- SW06: Military Data Sheet

## DESIGN RESOURCES

- SW06 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

## DISCUSSIONS

View all SW06 EngineerZone Discussions.

## SAMPLE AND BUY

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## TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

## DOCUMENT FEEDBACK

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# SW06–SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS (@ $V_+ = +15\text{ V}$ , $V_- = -15\text{ V}$ and $T_A = +25^\circ\text{C}$ , unless otherwise noted)

Parameter	Symbol	Conditions	SW06B			SW06F			SW06G			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
“ON” RESISTANCE	$R_{ON}$	$V_S = 0\text{ V}$ , $I_S = 1\text{ mA}$ $V_S = \pm 10\text{ V}$ , $I_S = 1\text{ mA}$	60	80		60	100		100	150		$\Omega$
$R_{ON}$ MATCH BETWEEN SWITCHES	$R_{ON\ Match}$	$V_S = 0\text{ V}$ , $I_S = 100\ \mu\text{A}^1$	5	10		5	20			20		%
ANALOG VOLTAGE RANGE	$V_A$	$I_S = 1\text{ mA}^2$ $I_S = 1\text{ mA}^2$	+10	+11		+10	+11		+10	+11		V
ANALOG CURRENT RANGE	$I_A$	$V_S = \pm 10\text{ V}$	10	15		7	12		5	10		mA
$\Delta R_{ON}$ VS. APPLIED VOLTAGE	$\Delta R_{ON}$	$-10\text{ V} \leq V_S \leq 10\text{ V}$ , $I_S = 1.0\text{ mA}$	5	15		10	20		10	20		%
SOURCE CURRENT IN “OFF” CONDITION	$I_{S(OFF)}$	$V_S = 10\text{ V}$ , $V_D = -10\text{ V}^3$	0.3	2.0		0.3	2.0		0.3	10		nA
DRAIN CURRENT IN “OFF” CONDITION	$I_{D(OFF)}$	$V_S = 10\text{ V}$ , $V_D = -10\text{ V}^3$	0.3	2.0		0.3	2.0		0.3	10		nA
SOURCE CURRENT IN “ON” CONDITION	$I_{S(ON)+}$ $I_{D(ON)}$	$V_S = V_D = \pm 10\text{ V}^3$	0.3	2.0		0.3	2.0		0.3	10		nA
LOGICAL “1” INPUT VOLTAGE	$V_{INH}$	Full Temperature Range <sup>2, 4</sup>	2.0			2.0			2.0			V
LOGICAL “0” INPUT VOLTAGE	$V_{INL}$	Full Temperature Range <sup>2, 4</sup>		0.8			0.8			0.8		V
LOGICAL “1” INPUT CURRENT	$I_{INH}$	$V_{IN} = 2.0\text{ V}$ to $15.0\text{ V}^5$		5			5			10		$\mu\text{A}$
LOGICAL “0” INPUT	$I_{INL}$	$V_{IN} = 0.8\text{ V}$		1.5	5.0		1.5	5.0		1.5	10.0	$\mu\text{A}$
TURN-ON TIME	$t_{ON}$	See Switching Time Test Circuit <sup>4, 6</sup>		340	500		340	600		340	700	ns
TURN-OFF TIME	$t_{OFF}$	See Switching Time Test Circuit <sup>4, 6</sup>		200	400		200	400		200	500	ns
BREAK-BEFORE-MAKE TIME	$t_{ON}-t_{OFF}$	Note 7	50	140		50	140		50	140		ns
SOURCE CAPACITANCE	$C_{S(OFF)}$	$V_S = 0\text{ V}^3$		7.0			7.0			7.0		pF
DRAIN CAPACITANCE	$C_{D(OFF)}$	$V_S = 0\text{ V}^3$		5.5			5.5			5.5		pF
CHANNEL “ON” CAPACITANCE	$C_{D(ON)+}$ $C_{S(ON)}$	$V_S = V_D = 0\text{ V}^3$		15			15			15		pF
“OFF” ISOLATION	$I_{SO(OFF)}$	$V_S = 5\text{ V rms}$ , $R_L = 680\ \Omega$ , $C_L = 7\text{ pF}$ , $f = 500\text{ kHz}^3$		58			58			58		dB
CROSSTALK	$C_T$	$V_S = 5\text{ V rms}$ , $R_L = 680\ \Omega$ , $C_L = 7\text{ pF}$ , $f = 500\text{ kHz}^3$		70			70			70		dB
POSITIVE SUPPLY CURRENT	$I_+$	All Channels “OFF”, DIS = “0” <sup>3</sup>	5.0	6.0		5.0	9.0		6.0	9.0		mA
NEGATIVE SUPPLY CURRENT	$I_-$	All Channels “OFF”, DIS = “0” <sup>3</sup>	3.0	5.0		4.0	7.0		4.0	7.0		mA
GROUND CURRENT	$I_G$	All Channels “ON” or “OFF” <sup>3</sup>	3.0	4.0		3.0	4.0		3.0	5.0		mA

**ELECTRICAL CHARACTERISTICS** (@  $V_+ = +15\text{ V}$ ,  $V_- = -15\text{ V}$ ,  $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$  for SW06BQ,  $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$  for SW06FQ and  $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$  for SW06GP/GS, unless otherwise noted)

Parameter	Symbol	Conditions	SW06B			SW06F			SW06G			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
TEMPERATURE RANGE	$T_A$	Operating	-55		+125	-25		+85	0		70	$^\circ\text{C}$
“ON” RESISTANCE	$R_{ON}$	$V_S = 0\text{ V}$ , $I_S = 1.0\text{ mA}$ $V_S = \pm 10\text{ V}$ , $I_S = 1.0\text{ mA}$	75	110		75	125		75	175		$\Omega$
$\Delta R_{ON}$ MATCH BETWEEN SWITCHES	$R_{ON}$ Match	$V_S = 0\text{ V}$ , $I_S = 100\ \mu\text{A}^1$	6	20		6	25		10			%
ANALOG VOLTAGE RANGE	$V_A$	$I_S = 1.0\text{ mA}^2$ $I_S = 1.0\text{ mA}^2$	+10	+11		+10	+11		+10	+11		V
ANALOG CURRENT RANGE	$I_A$	$V_S = \pm 10\text{ V}$	7	12		5	11		11			mA
$\Delta R_{ON}$ WITH APPLIED VOLTAGE	$\Delta R_{ON}$	$-10\text{ V} \leq V_S \leq 10\text{ V}$ , $I_S = 1.0\text{ mA}$	10			12			15			%
SOURCE CURRENT IN “OFF” CONDITION	$I_{S(OFF)}$	$V_S = 10\text{ V}$ , $V_D = -10\text{ V}$ $T_A = \text{Max Operating Temp}^{3,9}$		60			30			60		nA
DRAIN CURRENT IN “OFF” CONDITION	$I_{D(OFF)}$	$V_S = 10\text{ V}$ , $V_D = -10\text{ V}$ $T_A = \text{Max Operating Temp}^{3,9}$		60			30			60		nA
LEAKAGE CURRENT IN “ON” CONDITION	$I_{S(ON)+}$ $I_{D(ON)}$	$V_S = V_D = \pm 10\text{ V}$ $T_A = \text{Max Operating Temp}^{3,9}$		100			30			60		nA
LOGICAL “1” INPUT CURRENT	$I_{INH}$	$V_{IN} = 2.0\text{ V to } 15.0\text{ V}^5$		10			10			15		$\mu\text{A}$
LOGICAL “0” INPUT CURRENT	$I_{INL}$	$V_{IN} = 0.8\text{ V}$	4	10		4	10		5	15		$\mu\text{A}$
TURN-ON TIME	$t_{ON}$	See Switching Time Test Circuit <sup>4,8</sup>	440	900		500	900			1000		ns
TURN-OFF TIME	$t_{OFF}$	See Switching Time Test Circuit <sup>4,8</sup>	300	500		330	500			500		ns
BREAK-BEFORE-MAKE TIME	$t_{ON}-t_{OFF}$	Note 7	70			70			50			ns
POSITIVE SUPPLY CURRENT	$I_+$	All Channels “OFF,” DIS = “0” <sup>3</sup>		9.0			13.5			13.5		mA
NEGATIVE SUPPLY CURRENT	$I_-$	All Channels “OFF,” DIS = “0” <sup>3</sup>		7.5			10.5			10.5		mA
GROUND CURRENT	$I_G$	All Channels “ON” or “OFF” <sup>3</sup>		6.0			7.5			7.5		mA

NOTES

<sup>1</sup> $V_S = 0\text{ V}$ ,  $I_S = 100\ \mu\text{A}$ . Specified as a percentage of  $R_{AVERAGE}$  where:  $R_{AVERAGE} = \frac{R_{ON1} + R_{ON2} + R_{ON3} + R_{ON4}}{4}$ .

<sup>2</sup>Guaranteed by  $R_{ON}$  and leakage tests. For normal operation maximum analog signal voltages should be restricted to less than  $(V_+) - 4\text{ V}$ .

<sup>3</sup>Switch being tested ON or OFF as indicated,  $V_{INH} = 2.0\text{ V}$  or  $V_{INL} = 0.8\text{ V}$ , per logic truth table.

<sup>4</sup>Also applies to disable pin.

<sup>5</sup>Current tested at  $V_{IN} = 2.0\text{ V}$ . This is worst case condition.

<sup>6</sup>Sample tested.

<sup>7</sup>Switch is guaranteed by design to provide break-before-make operation.

<sup>8</sup>Guaranteed by design.

<sup>9</sup>Parameter tested only at  $T_A = +125^\circ\text{C}$  for military grade device.

Specifications subject to change without notice.

# SW06

## WAFER TEST LIMITS (@ $V_+ = +15\text{ V}$ , $V_- = -15\text{ V}$ , $T_A = +25^\circ\text{C}$ , unless otherwise noted)

Parameter	Symbol	Conditions	SW06N Limit	SW06G Limit	Units
“ON” RESISTANCE	$R_{ON}$	$-10\text{ V} \leq V_A \leq 10\text{ V}$ , $I_S \leq 1\text{ mA}$	80	100	$\Omega$ max
$R_{ON}$ MATCH BETWEEN SWITCHES	$R_{ON}$ Match	$V_A = 0\text{ V}$ , $I_S \leq 100\text{ }\mu\text{A}$	15	20	% max
$\Delta R_{ON}$ VS. $V_A$	$\Delta R_{ON}$	$-10\text{ V} \leq V_A \leq 10\text{ V}$ , $I_S \leq 1\text{ mA}$	10	20	% max
POSITIVE SUPPLY CURRENT	$I_+$	Note 1	6.0	9.0	mA max
NEGATIVE SUPPLY CURRENT	$I_-$	Note 1	5.0	7.0	mA max
GROUND CURRENT	$I_G$	Note 1	4.0	4.0	mA max
ANALOG VOLTAGE RANGE	$V_A$	$I_S = 1\text{ mA}$	$\pm 10.0$	$\pm 10.0$	V min
LOGIC “1” INPUT VOLTAGE	$V_{INH}$	Note 2	2.0	2.0	V min
LOGIC “0” INPUT VOLTAGE	$V_{INL}$	Note 2	0.8	0.8	V max
LOGIC “0” INPUT CURRENT	$I_{INL}$	$0\text{ V} \leq V_{IN} \leq 0.8\text{ V}$	5.0	5.0	$\mu\text{A}$ max
LOGIC “1” INPUT CURRENT	$I_{INH}$	$2.0\text{ V} \leq V_{IN} \leq 15\text{ V}^3$	5	5	$\mu\text{A}$ max
ANALOG CURRENT RANGE	$I_A$	$V_S = \pm 10\text{ mV}$	10	7	mA min

### NOTE

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

## TYPICAL ELECTRICAL CHARACTERISTICS (@ $V_+ = +15\text{ V}$ , $V_- = -15\text{ V}$ , $T_A = +25^\circ\text{C}$ , unless otherwise noted)

Parameter	Symbol	Conditions	SW06N Typical	SW06G Typical	Units
“ON” RESISTANCE	$R_{ON}$	$-10\text{ V} \leq V_A \leq 10\text{ V}$ , $I_S \leq 1\text{ mA}$	60	60	$\Omega$
TURN-ON TIME	$t_{ON}$		340	340	ns
TURN-OFF TIME	$t_{OFF}$		200	200	ns
DRAIN CURRENT IN “OFF” CONDITION	$I_{D(OFF)}$	$V_S = 10\text{ V}$ , $V_D = -10\text{ V}$	0.3	0.3	nA
“OFF” ISOLATION	$I_{SO(OFF)}$	$f = 500\text{ kHz}$ , $R_L = 680\text{ }\Omega$	58	58	dB
CROSSTALK	$C_T$	$f = 500\text{ kHz}$ , $R_L = 680\text{ }\Omega$	70	70	dB

### NOTES

<sup>1</sup>Power supply and ground current specified for switch “ON” or “OFF.”

<sup>2</sup>Guaranteed by  $R_{ON}$  and leakage tests.

<sup>3</sup>Current tested at  $V_{IN} = 2.0\text{ V}$ . This is worst case condition.

## ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

Operating Temperature Range  
 SW06BQ, BRC ..... -55°C to +125°C  
 SW06FQ ..... -40°C to +85°C  
 SW06GP, GS ..... -40°C to +85°C  
 Storage Temperature Range ..... -65°C to +150°C  
 Lead Temperature (Soldering, 60 sec) ..... +300°C  
 Maximum Junction Temperature ..... +150°C  
 V+ Supply to V- Supply ..... +36 V  
 V+ Supply to Ground ..... +36 V  
 Logic Input Voltage ..... (-4 V or V-) to V+ Supply  
 Analog Input Voltage Range  
 Continuous ..... V- Supply to V+ Supply +20 V  
 Maximum Current Through  
 Any Pin Including Switch ..... 30 mA

Package Type	$\theta_{JA}$ <sup>2</sup>	$\theta_{JC}$	Units
16-Pin Hermetic DIP (Q)	100	16	°C/W
16-Pin Plastic DIP (P)	82	39	°C/W
20-Contact LCC (RC)	98	38	°C/W
16-Pin SOL (S)	98	30	°C/W

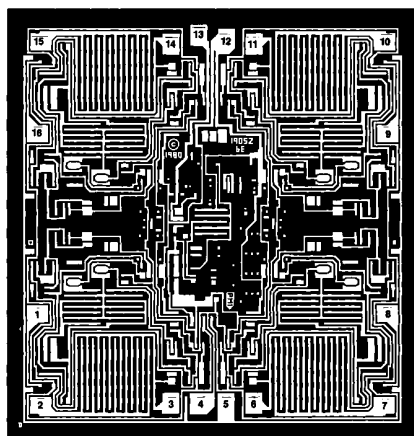
## NOTES

<sup>1</sup>Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

<sup>2</sup> $\theta_{JA}$  is specified for worst case mounting conditions, i.e.,  $\theta_{JA}$  is specified for device in socket for Cerdip, P-DIP, and LCC packages;  $\theta_{JA}$  is specified for device soldered to printed circuit board for SO package.

## DICE CHARACTERISTICS

Die Size 0.101 × 0.097 inch, 9797 sq. mils  
 (2.565 × 2.464 mm, 6320 sq. mm)



## ORDERING GUIDE

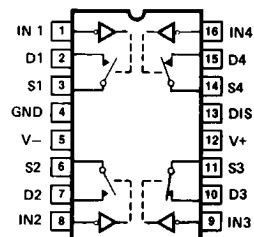
Model	Temperature Range	Package Description	Package Option
SW06BQ	-55°C to +125°C	Cerdip	Q-16
SW06BRC	-55°C to +125°C	LCC	E-20A
SW06FQ	-40°C to +85°C	Cerdip	Q-16
SW06GP	-40°C to +85°C	Plastic DIP	N-16
SW06GS	-40°C to +85°C	SOL	R-16

## TRUTH TABLE

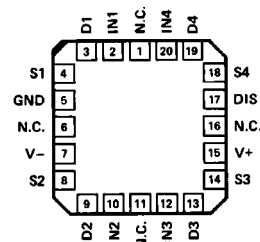
Disable Input	Logic Input	Switch State	
		Channels 1 & 2	Channels 3 & 4
0	X	OFF	OFF
1 or NC	0	OFF	ON
1 or NC	1	ON	OFF

## PIN CONNECTIONS

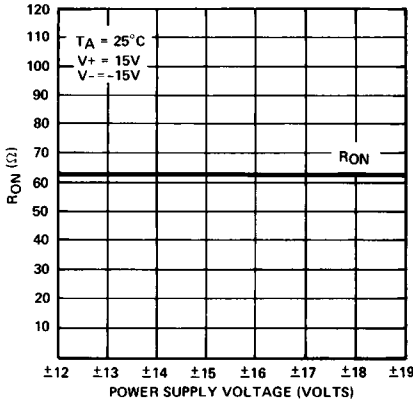
16-Pin DIP (Q or P-Suffix)  
 16-Pin SOL (S-Suffix)



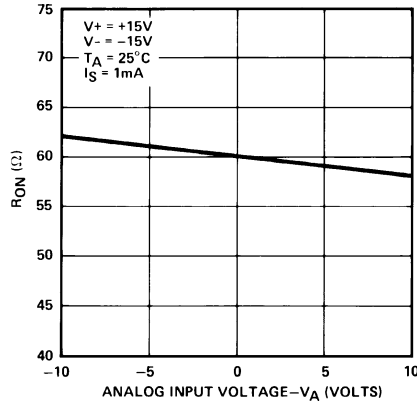
SW06BRC/883  
 LCC Package  
 (RC-Suffix)



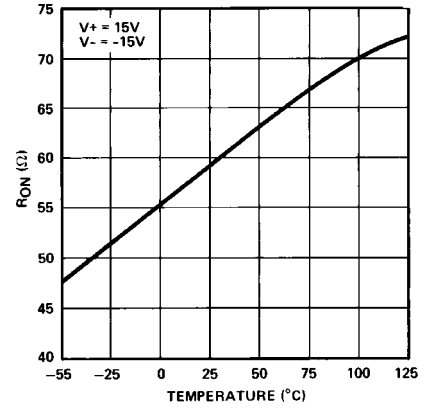
# SW06—Typical Performance Characteristics



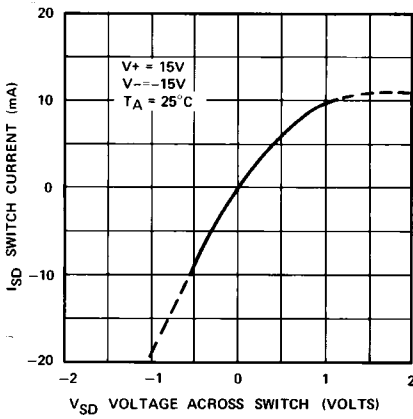
“ON” Resistance vs. Power Supply Voltage



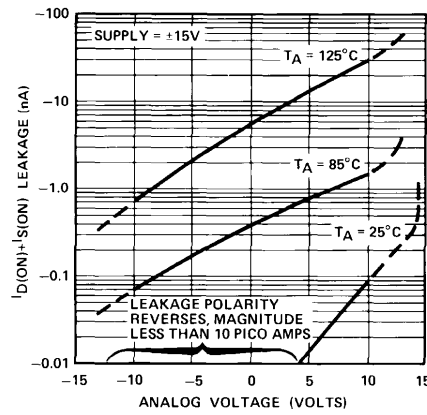
“ON” Resistance vs. Analog Voltage



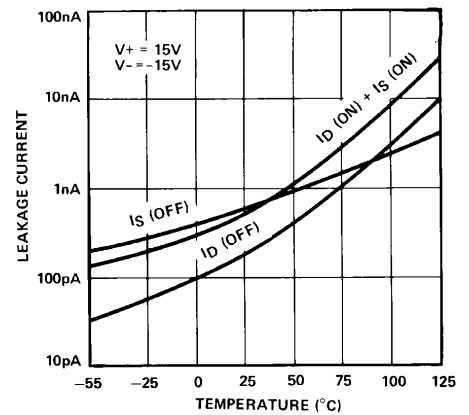
$R_{ON}$  vs. Temperature



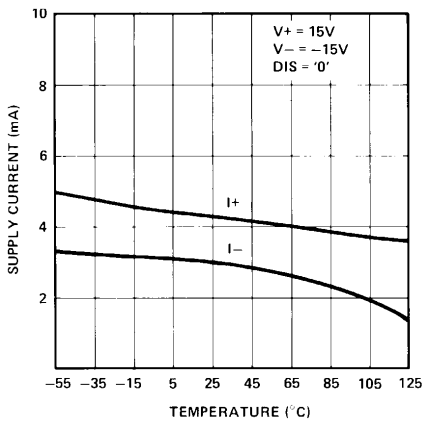
Switch Current vs. Voltage



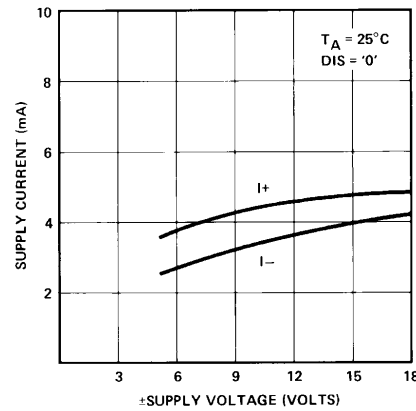
Leakage Current vs. Analog Voltage



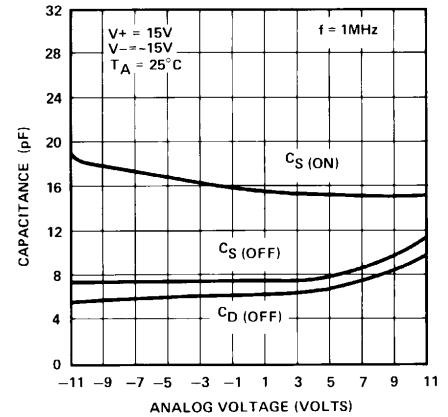
Leakage Current vs. Temperature



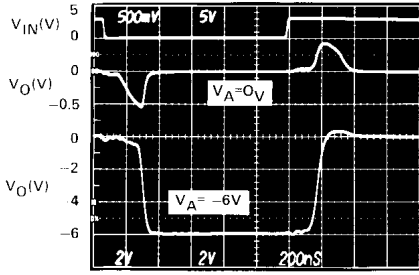
Supply Current vs. Temperature



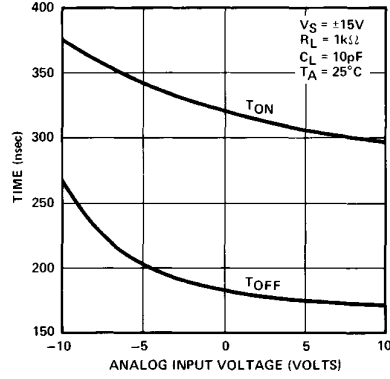
Supply Current vs. Supply Voltage



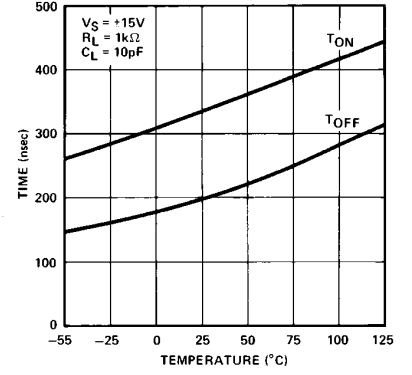
Switch Capacitance vs. Analog Voltage



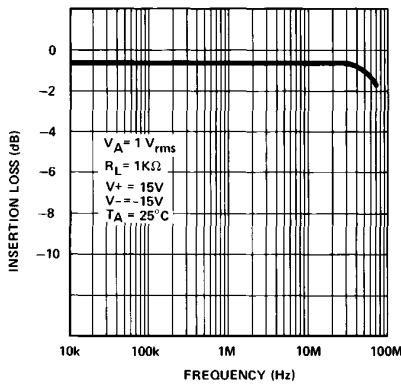
$T_{ON}/T_{OFF}$  Switching Response



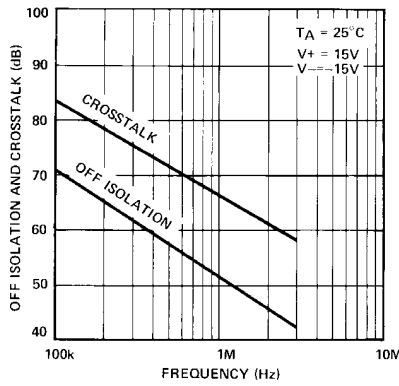
Switching Time vs. Analog Voltage



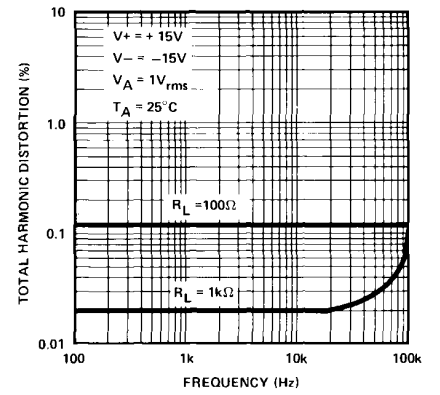
Switching Time vs. Temperature



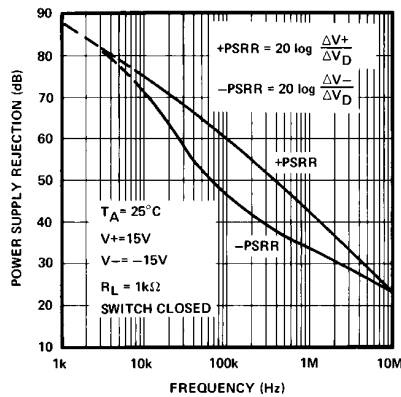
Insertion Loss vs. Frequency



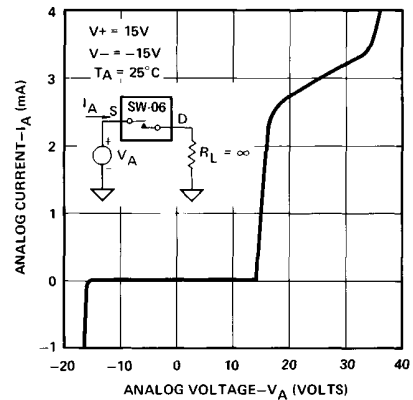
Crosstalk and "OFF" Isolation vs. Frequency



Total Harmonic Distortion

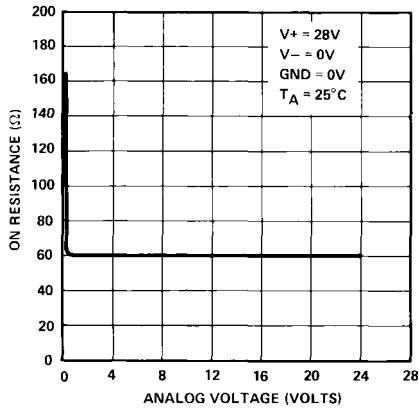


Power Supply Rejection vs. Frequency

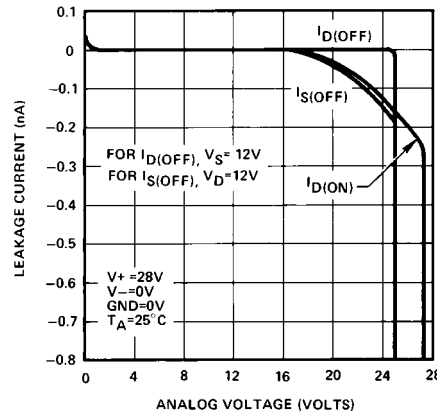


Overvoltage Characteristics

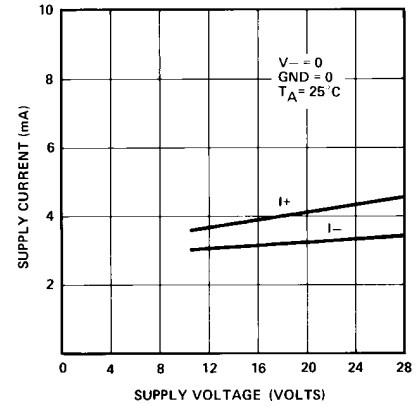
# SW06—Typical Performance Characteristics (Operating and Single Supply)



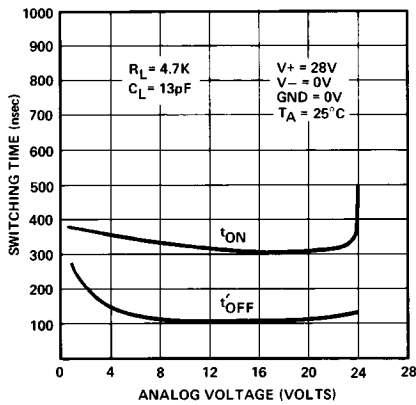
“On” Resistance vs. Analog Voltage



Leakage Current vs.  $V_{ANALOG}$



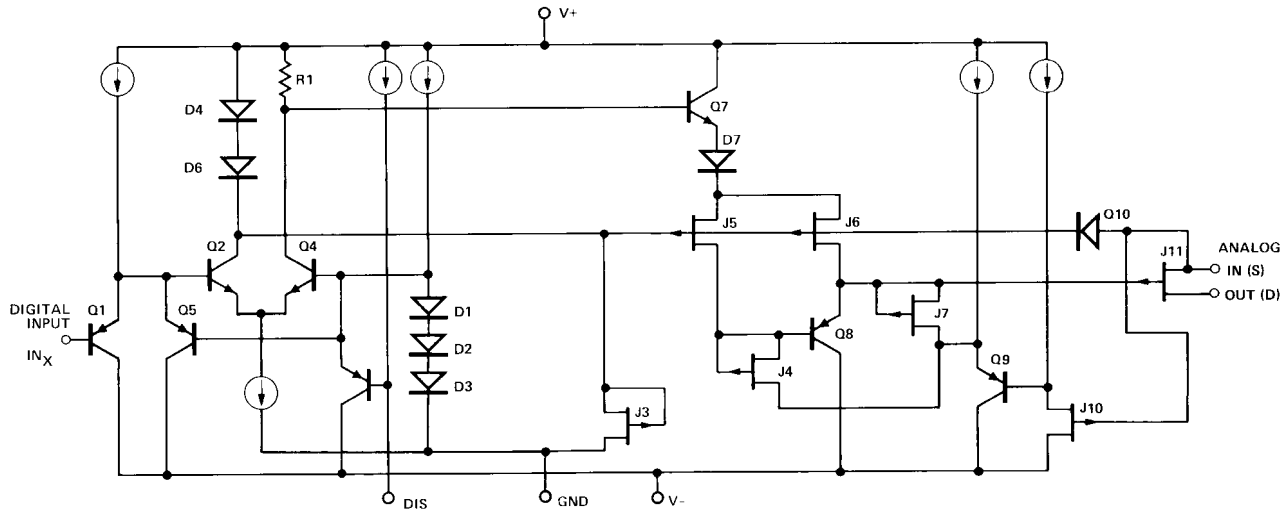
Supply Current vs. Supply Voltage



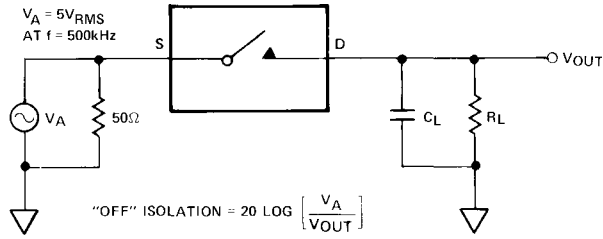
Switching Time vs. Supply Voltage

### NOTE

These single-supply-operation characteristic curves are valid when the negative power supply  $V_-$  is tied to the logic ground reference pin “GND.” TTL input compatibility is still maintained when “GND” is the same potential as the TTL ground.  $t_{OFF}$  is measured from 50% of logic input waveform to 0.9  $V_O$ . The analog voltage range extends from 0 V to  $V_+ - 4$  V; the switch will no longer respond to logic control when  $V_A$  is within 4 volts of  $V_+$ .

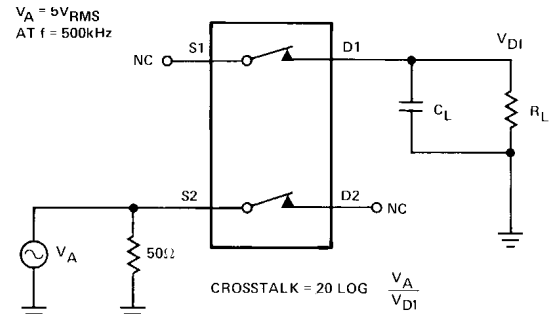


Simplified Schematic Diagram (Typical Switch)



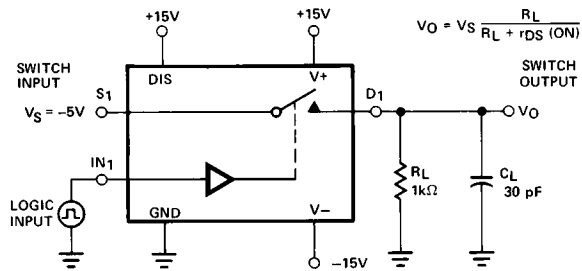
"OFF" ISOLATION =  $20 \text{ LOG} \left[ \frac{V_A}{V_{OUT}} \right]$

"Off" Isolation Test Circuit



CROSSTALK =  $20 \text{ LOG} \left[ \frac{V_A}{V_{DI}} \right]$

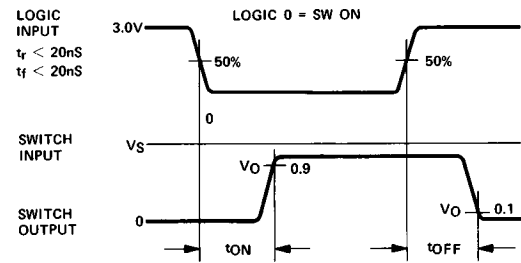
Crosstalk Test Circuit



$V_O = V_S \frac{R_L}{R_L + r_{DS(ON)}}$

REPEAT TEST FOR  $IN_2$ ,  $IN_3$  AND  $IN_4$ .

Switching Time Test Circuit



SWITCH OUTPUT WAVEFORM SHOWN FOR  $V_S = \text{CONSTANT}$  WITH LOGIC INPUT WAVEFORM AS SHOWN.  $V_O$  IS THE STEADY STATE OUTPUT WITH SWITCH ON. LOGIC INPUT IS INVERTED FOR SWITCH 1 & 2

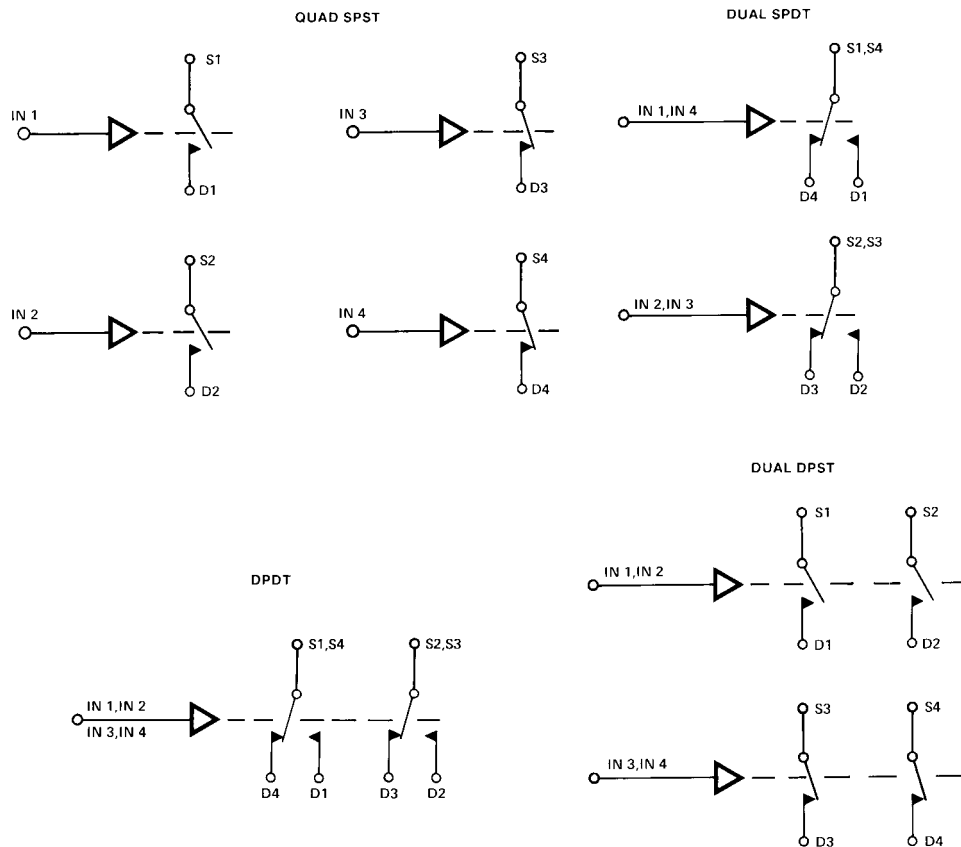


Figure 1. Functional Applications of SW06

## APPLICATIONS INFORMATION

The single analog switch product configures, by appropriate pin connections, into four switch applications. As shown in Figure 1, the SW06 connects as a QUAD SPST, a DUAL SPDT, a DUAL DPST, or a DPDT analog switch. This versatility increases further when taking advantage of the disable input (DIS) which turns all switches OFF when taken active low.

Ion-implantation of the JFET analog switch achieves low ON resistance and tight channel-to-channel matching. Combining the low ON resistance and low leakage currents results in a worst case voltage error figure  $V_{\text{ERROR}} @ +125^{\circ}\text{C} = I_{\text{D(ON)}} \times R_{\text{SD(ON)}} = 100 \text{ nA} \times 100 \Omega = 11 \text{ microvolts}$ . This amount of error is negligible considering dissimilar-metal thermally-induced offsets will be in the 5 to 15 microvolt range.

## LOGIC INPUTS

The logic inputs ( $\text{IN}_X$ ) and disable input (DIS) are referenced to a TTL logic threshold value of two forward diode drops (1.4 V at  $+25^{\circ}\text{C}$ ) above the GND terminal. These inputs use PNP transistors which draw maximum current at a logic "0" level and drops to a leakage current of a reverse biased diode as the logic input voltage raises above 1.4 volts. Any logic input voltage greater than 2.0 volts becomes logic "1," less than 0.8 volts becomes logic "0" resulting in full TTL noise immunity not available from similar CMOS input analog switches. The PNP transistor inputs require such low input current that the SW06 approaches fan-ins of CMOS input devices. These bipolar logic inputs exceed any CMOS input circuit in resistance to static voltage and radiation susceptibility. No damage will occur to the SW06 if logic high voltages are present when the SW06 power

supplies are OFF. When the  $V+$  and  $V-$  supplies are OFF, the logic inputs present a reverse bias diode loading to active logic inputs. Input logic thresholds are independent of  $V+$  and  $V-$  supplies making single  $V+$  supply operation possible by simply connecting GND and  $V-$  together to the logic ground supply.

## ANALOG VOLTAGE AND CURRENT

### ANALOG VOLTAGE

These switches have constant ON resistance for analog voltages from the negative power supply ( $V-$ ) to within 4 volts of the positive power supply. This characteristic shown in the plots results in good total harmonic distortion, especially when compared to CMOS analog switches that have a 20 to 30 percent variation in ON resistance versus analog voltage. Positive analog input voltage should be restricted to 4 volts less than  $V+$  assuring the switch remains open circuit in the OFF state. No increase in switch ON resistance occurs when operating at supply voltages less than  $\pm 15$  volts (see plot). Small signals have a 3 dB down frequency of 70 MHz (see insertion loss versus frequency plot).

### ANALOG CURRENT

The analog switches in the ON state are JFETs biased in their triode region and act as switches for analog current up to the  $I_A$  specification (see plot of  $I_{\text{DS}}$  vs  $V_{\text{DS}}$ ). Some applications require pulsed currents exceeding the  $I_A$  spec. For example, an integrator reset switch discharging a shunt capacitor will produce a peak current of  $I_{\text{A(PEAK)}} = V_{\text{CAP}}/R_{\text{DS(ON)}}$ . In this application, it is best to connect the source to the most positive end of the capacitor, thereby achieving the lowest switch resistance and

fastest reset times. The switch can easily handle any amount of capacitor discharge current subject only to the maximum heat dissipation of the package and the maximum operating junction temperature from which repetition can be established.

**SWITCHING**

Switching time  $t_{ON}$  and  $t_{OFF}$  characteristics are plotted versus  $V_{ANALOG}$  and temperature. In all cases,  $t_{OFF}$  is designed faster than  $t_{ON}$  to ensure a break-before-make interval for SPDT and DPDT applications. The disable input (DIS) has the same switching times ( $t_{ON}$  and  $t_{OFF}$ ) as the logic inputs ( $IN_X$ ).

Switching transients occurring at the source and drain contacts results from ac coupling of the switching FET's gate-to-source and gate-to-drain coupling capacitance. The switch turn ON will cause a negative going spike to occur and the turn OFF will cause a positive spike to occur. These spikes can be reduced by additional capacitance loading, lower values of  $R_L$ , or switching an additional switch (with its extra contact floating) to the opposite state connected to the spike sensitive node.

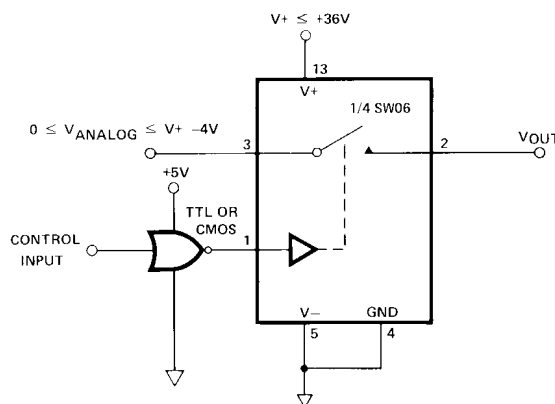
**DISABLE NODE**

This TTL compatible node is similar to the logic inputs  $IN_X$  but has an internal  $2 \mu A$  current source pull-up. If disable is left unconnected, it will assume the logic "1" state, then the state of the switches is controlled only by the logic inputs  $IN_X$ .

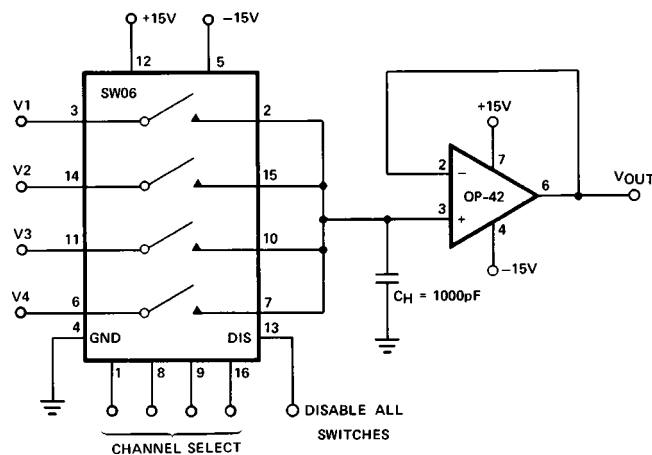
**POWER SUPPLIES**

This product operates with power supply voltages ranging from  $\pm 12$  to  $\pm 18$  volts; however, the specifications only guarantee device parameters with  $\pm 15$  volt  $\pm 5\%$  power supplies. The power supply sensitive parameters have plots to indicate effects of supply voltages other than  $\pm 15$  volts.

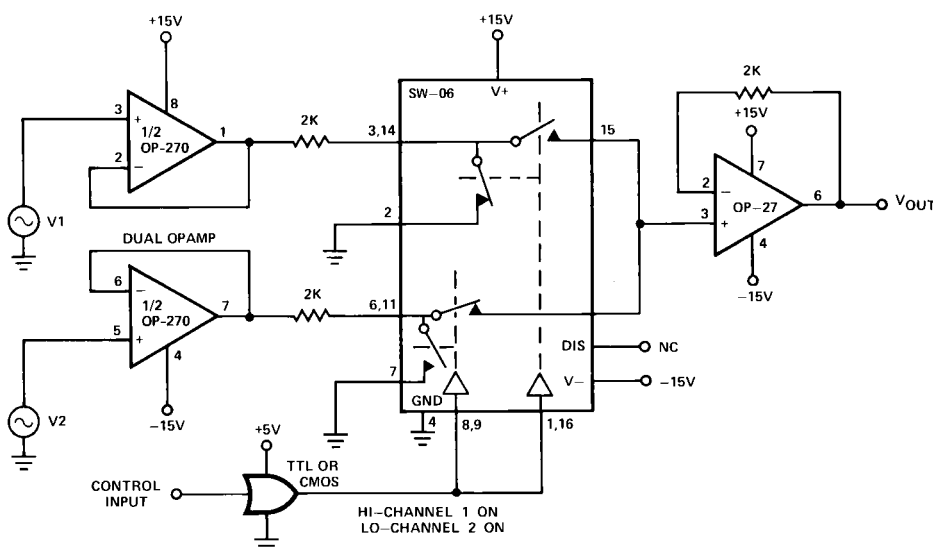
**Typical Applications**



Operation from Single Positive Power Supply

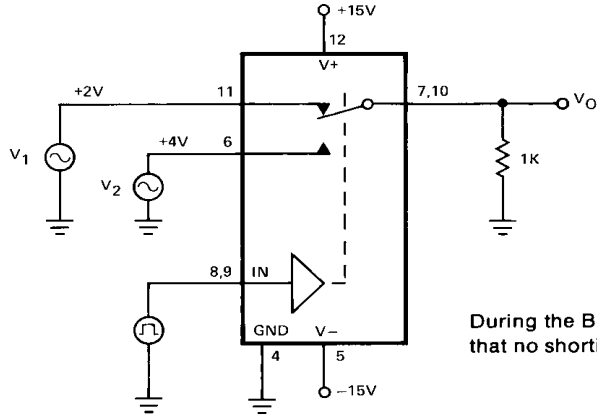


4-Channel Sample Hold Amplifier

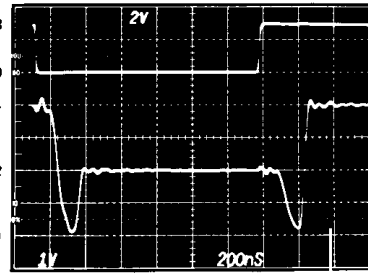


THIS SWITCH ARRANGEMENT IMPROVES OFF ISOLATION BY 30dB

High Off Isolation Selector Switch (Shunt-Series Switch)



LOGIC IN (VOLTS)  
V<sub>O</sub> (VOLTS)



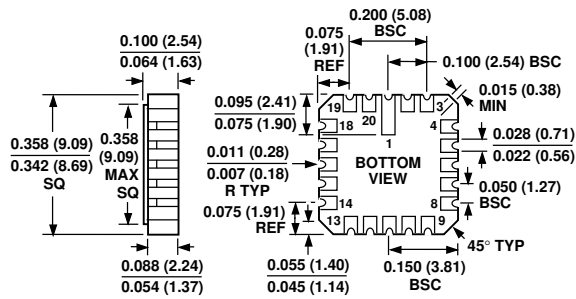
During the BBM interval the 1kΩ resistor pulls the output to ground assuring that no shorting between V<sub>1</sub> and V<sub>2</sub> occurs.

Single Pole Double Throw Selector Switch with Break-Before-Make Interval

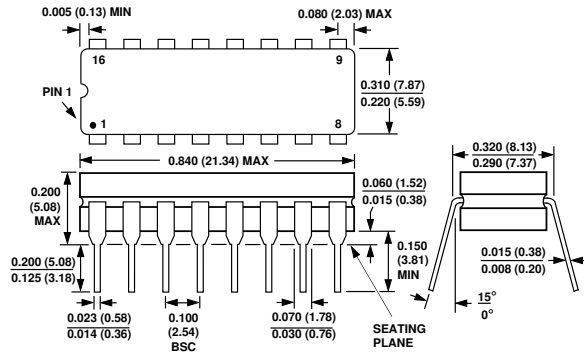
**OUTLINE DIMENSIONS**

Dimensions shown in inches and (mm).

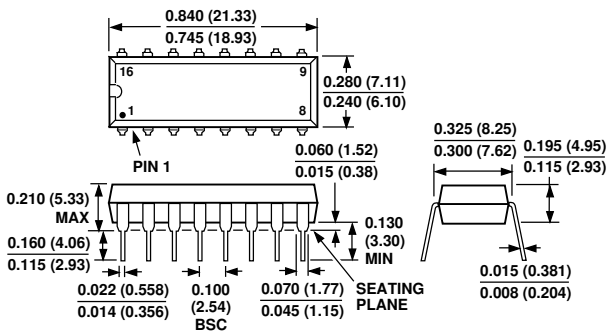
**20-Terminal Leadless Chip Carrier  
(RC-Suffix)  
E-20A**



**16-Lead Cerdip  
(Q-Suffix)  
Q-16**



**16-Lead Plastic DIP  
(P-Suffix)  
N-16**



**16-Lead Wide Body SOL  
(S-Suffix)  
R-16/SOL-16**

