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SX1213 Receiver
Ultra-Low Power Integrated UHF Receiver

General Description

The SX1213 is a low cost single-chip receiver operating in the frequency ranges from 300MHz to 510MHz. The SX1213 is optimized for very low power consumption (3mA). It incorporates a baseband demodulator with data rates up to 200 kb/s. Data handling features include a sixty-four byte FIFO, packet handling, CRC and data whitening processing. Its highly integrated architecture allows for minimum external component count whilst maintaining design flexibility. All major RF communication parameters are programmable and most of them may be dynamically set. It complies with European (ETSI EN 300-220 V2.1.1) and North American (FCC part 15.247 and 15.249) regulatory standards.

Ordering Information

Table 1: Ordering Information

Part number	Delivery	Minimum Order Quantity / Multiple
SX1213IWLTRT	Tape & Reel	3000 pieces

-
- TQFN-32 package – Operating range [-40;+85°C]
- T refers to Lead Free packaging
- This device is WEEE and RoHS compliant

Features

- Low Rx power consumption: 3mA
- Good reception sensitivity: down to -104 dBm at 25 kb/s in FSK, -110 dBm at 2kb/s in OOK
- Packet handling feature with data whitening and CRC processing
- RSSI (Received Signal Strength Indicator) range from Rx noise floor to 0 dBm
- Bit rates up to 200 kb/s, NRZ coding
- On-chip frequency synthesizer
- FSK and OOK modulation
- Incoming sync word recognition
- Built-in Bit-Synchronizer for incoming data and clock synchronization and recovery
- 5 x 5 mm TQFN package
- Optimized Circuit Configuration for Low-cost applications
- Pin to pin compatible with SX1212 Transceiver

Applications

- Wireless alarm and security systems
- Wireless sensor networks
- Automated Meter Reading
- Home and building automation
- Industrial monitoring and control
- Remote Wireless Control

Application Circuit Schematic

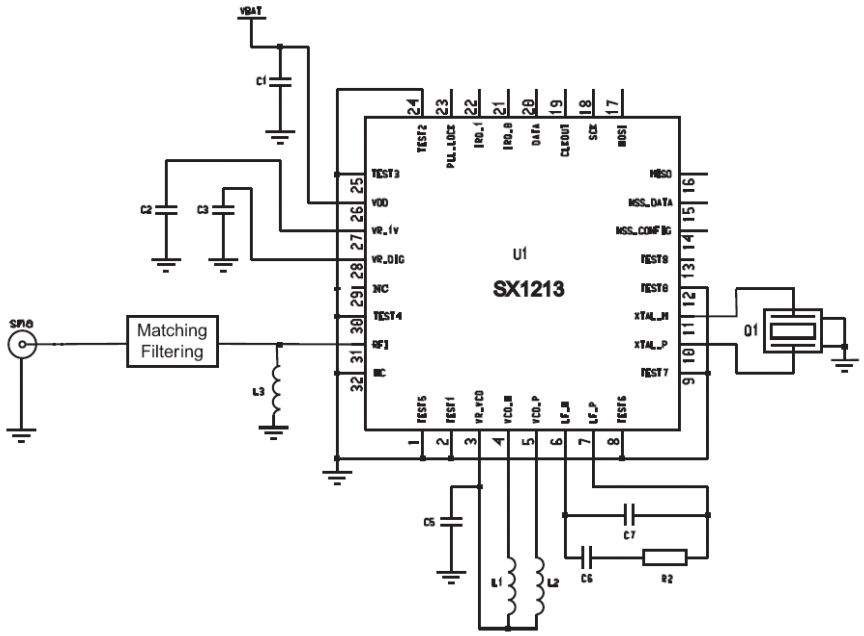

Table of Contents

Index of Figures

Index of Tables

Acronyms

BOM	Bill Of Materials
BR	Bit Rate
BW	Bandwidth
CCITT	Comité Consultatif International Téléphonique et Télégraphique - ITU
CP	Charge Pump
CRC	Cyclic Redundancy Check
DAC	Digital to Analog Converter
DDS	Direct Digital Synthesis
DLL	Dynamically Linked Library
ERP	Equivalent Radiated Power
ETSI	European Telecommunications Standards Institute
FCC	Federal Communications Commission
Fdev	Frequency Deviation
FIFO	First In First Out
FS	Frequency Synthesizer
FSK	Frequency Shift Keying
GUI	Graphical User Interface
IC	Integrated Circuit
ID	IDentificator
IF	Intermediate Frequency
IRQ	Interrupt ReQuest
ITU	International Telecommunication Union
LFSR	Linear Feedback Shift Register
LNA	Low Noise Amplifier
LO	Local Oscillator
LSB	Least Significant Bit
MSB	Most Significant Bit
NRZ	Non Return to Zero
NZIF	Near Zero Intermediate Frequency
OOK	On Off Keying
PA	Power Amplifier
PCB	Printed Circuit Board
PFD	Phase Frequency Detector
PLL	Phase-Locked Loop
POR	Power On Reset
RBW	Resolution BandWidth
RF	Radio Frequency
RSSI	Received Signal Strength Indicator
Rx	Receiver
SAW	Surface Acoustic Wave
SPI	Serial Peripheral Interface
SR	Shift Register
Stby	Standby
Tx	Transmitter
uC	Microcontroller
VCO	Voltage Controlled Oscillator
XO	Crystal Oscillator
XOR	eXclusive OR

This product datasheet contains a detailed description of the SX1213 performance and functionality. Please consult the Semtech website for the latest updates or errata.

1. General Description

The SX1213 is a single chip FSK and OOK receiver capable of operation in the 300 to 510 MHz license free ISM frequency bands. It complies with both the relevant European and North American standards, EN 300-220 V2.1.1 (June 2006 release) and FCC Part 15 (10-1-2006 edition). A unique feature of this circuit is its extremely low current consumption in full active mode of only 3mA (typ). The SX1213 is available in a 5x5 mm TQFN-32 package.

1.1. Simplified Block Diagram

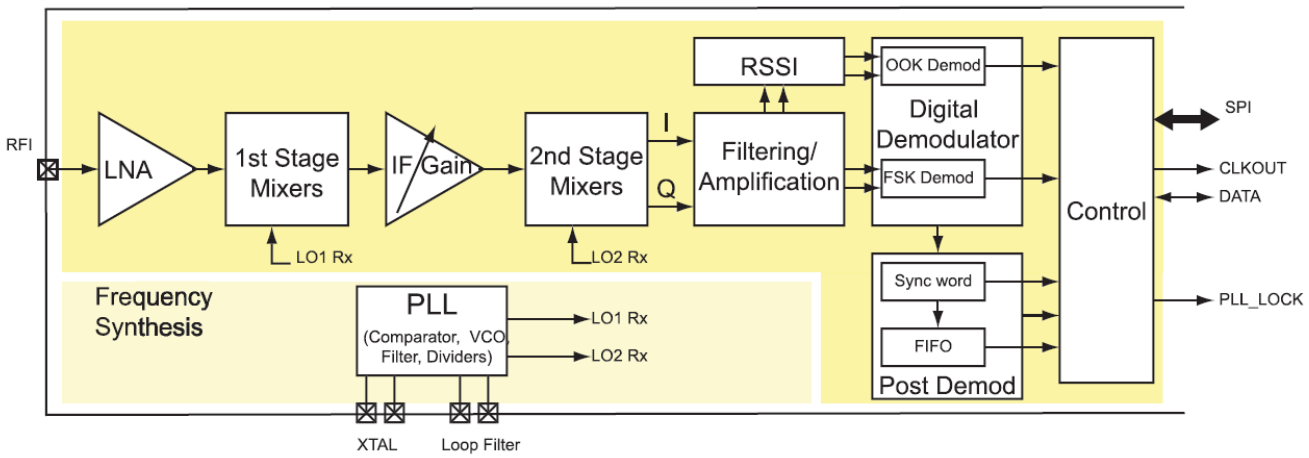

Figure 1: SX1213 Simplified Block Diagram

1.2. Pin Diagram

The following diagram shows the pins arrangement of the QFN package, top view.

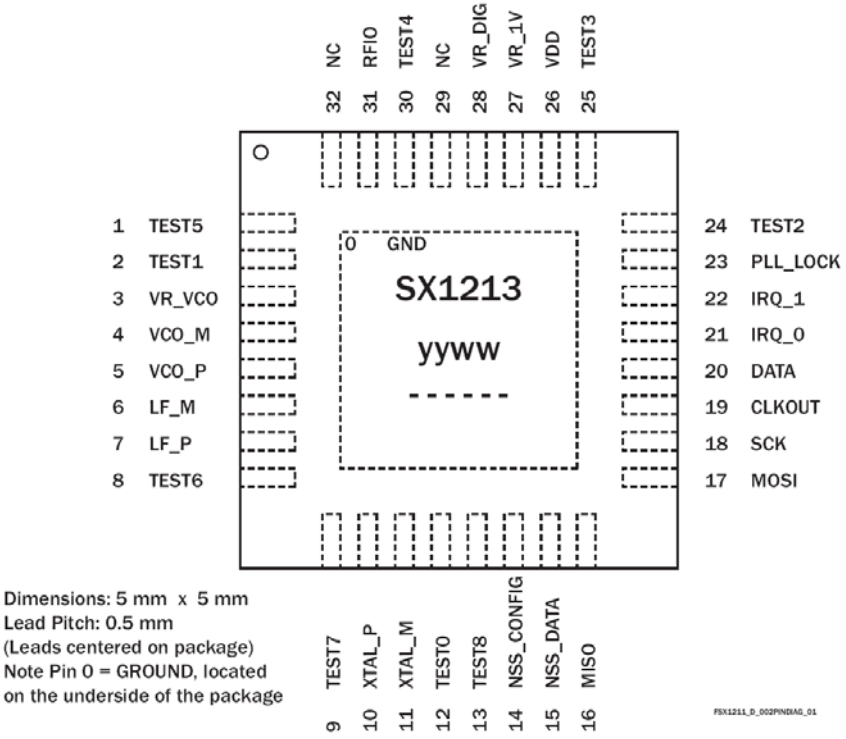

Figure 2: SX1213 Pin Diagram

Notes:

- yyww refers to the date code
- ------ refers to the lot number

1.3. Pin Description

Table 2: SX1213 Pinouts

Number	Name	Type	Description
0	GND	I	Exposed ground pad
1	TEST5	I/O	Connect to GND
2	TEST1	I/O	Connect to GND
3	VR_VCO	O	Regulated supply of the VCO
4	VCO_M	I/O	VCO tank
5	VCO_P	I/O	VCO tank
6	LF_M	I/O	PLL loop filter
7	LF_P	I/O	PLL loop filter
8	TEST6	I/O	Connect to GND
9	TEST7	I/O	Connect to GND
10	XTAL_P	I/O	Crystal connection
11	XTAL_M	I/O	Crystal connection
12	TEST0	I	Connect to GND
13	TEST8	I/O	POR. Do not connect if unused
14	NSS_CONFIG	I	SPI CONFIG enable
15	NSS_DATA	I	SPI DATA enable
16	MISO	O	SPI data output
17	MOSI	I	SPI data input
18	SCK	I	SPI clock input
19	CLKOUT	O	Clock output
20	DATA	O	NRZ data output (Continuous mode)
21	IRQ_0	O	Interrupt output
22	IRQ_1	O	Interrupt output
23	PLL_LOCK	O	PLL lock detection output
24	TEST2	I/O	Connect to GND
25	TEST3	I/O	Connect to GND
26	VDD	I	Supply voltage
27	VR_1V	O	Regulated supply of the analog circuitry
28	VR_DIG	O	Regulated supply of digital circuitry
29	NC	-	Connect to GND
30	TEST4	I/O	Connect to GND
31	RFI	I	RF input
32	NC	-	Connect to GND

Note: pin 13 (Test 8) can be used as a manual reset trigger. See section 7.4.2 for details on its use.

2. Electrical Characteristics

2.1. ESD Notice

The SX1213 is a high performance radio frequency device. It satisfies:

- Class 2 of the JEDEC standard JESD22-A114-B (Human Body Model), except on pins 3-4-5-27-28-31-where it satisfies Class 1A.
- Class III of the JEDEC standard JESD22-C101C (Charged Device Model) on all pins.

It should thus be handled with all the necessary ESD precautions to avoid any permanent damage.

2.2. Absolute Maximum Ratings

Stresses above the values listed below may cause permanent device failure. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Table 3: Absolute Maximum Ratings

Symbol	Description	Min	Max	Unit
VDDmr	Supply voltage	-0.3	3.7	V
Tmr	Storage temperature	-55	125	°C
Pmr	Input level	-	0	dBm

2.3. Operating Range

Table 4: Operating Range

Symbol	Description	Min	Max	Unit
VDDop	Supply Voltage	2.1	3.6	V
Trop	Temperature	-40	+85	°C
ML	Input Level	-	0	dBm

2.4. Chip Specification

Conditions: Temp = 25 °C, VDD = 3.3 V, crystal frequency = 12.8 MHz, carrier frequency = 315 or 434 MHz, modulation FSK, data rate = 25 kb/s, Fdev = 50 kHz, fc = 100 kHz, unless otherwise specified.

2.4.1. Power Consumption

Table 5: Power Consumption Specification

Symbol	Description	Conditions	Min	Typ	Max	Unit
IDDSL	Supply current in sleep mode		-	0.1	2	µA
IDDST	Supply current in standby mode, CLKOUT disabled	Crystal oscillator running	-	65	95	µA
IDDFS	Supply current in FS mode	Frequency synthesizer running	-	1.3	1.7	mA
IDDR	Supply current in receiver mode		-	3.0	3.5	mA

(1) Information from design and characterization

2.4.2. Frequency Synthesis

Table 6: Frequency Synthesizer Specification

Symbol	Description	Conditions	Min	Typ	Max	Unit
FR	Frequency ranges	Programmable (may require specific BOM)	300 320 350 390 430 470	- - - - - -	330 350 390 430 470 510	MHz MHz MHz MHz MHz MHz
BR_F	Bit rate (FSK)	NRZ	1.56	-	200	Kb/s
BR_O	Bit rate (OOK)	NRZ	1.56	-	32	Kb/s
FDA	Frequency deviation (FSK)		33	50	200	kHz
XTAL	Crystal oscillator frequency		9	12.8	15	MHz
FSTEP	Frequency synthesizer step	Variable, depending on the frequency.	-	2	-	kHz
TS_OSC	Oscillator wake-up time	From Sleep mode(1)	-	1.5	5	ms
TS_FS	Frequency synthesizer wake-up time at most 10 kHz away from the target	From Stby mode	-	500	800	µs
TS_HOP	Frequency synthesizer hop time at most 10 kHz away from the target	200 kHz step	-	180	-	µs
		1 MHz step	-	200	-	µs
		5 MHz step	-	250	-	µs
		7 MHz step	-	260	-	µs
		12 MHz step	-	290	-	µs
		20 MHz step	-	320	-	µs
		27 MHz step	-	340	-	µs

(1) Information from design and characterization

2.4.3. Receiver

- On the following table, fc and fo describe the bandwidth of the active channel filters as described in section 3.3.4.2. All sensitivities are measured receiving a PN15 sequence, for a BER of 0.1.%

Table 7: Receiver Specification

Symbol	Description	Conditions	Min	Typ	Max	Unit
RFS_F	Sensitivity (FSK)	434 MHz, BR=25 kb/s, Fdev =50 kHz, fc=100 kHz	-	-104	-	dBm
RFS_O	Sensitivity (OOK)	434 MHz, 2kb/s NRZ fc-fo=50 kHz, fo=50 kHz	-	-110	-	dBm
CCR	Co-channel rejection	Modulation as wanted signal	-	-12	-	dBc
ACR	Adjacent channel rejection	Offset = 300 kHz, unwanted tone is not modulated	-	27	-	dB
		Offset = 600 kHz, unwanted tone is not modulated	-	52	-	dB
		Offset = 1.2 MHz, unwanted tone is not modulated	-	57	-	dB
BI	Blocking immunity	Offset = 1 MHz, unmodulated	-	-48	-	dBm
		Offset = 2 MHz, unmodulated, no SAW	-	-37	-	dBm
		Offset = 10 MHz, unmodulated, no SAW	-	-33	-	dBm
RXBW_F(1,2)	Receiver bandwidth in FSK mode	Single side BW Polyphase Off	50	-	250	kHz
RXBW_O(1,2)	Receiver bandwidth in OOK mode	Single side BW Polyphase On	50	-	400	kHz
IIP3	Input 3rd order intercept point	Interferers at 1MHz and 1.950 MHz offset	-	-28	-	dBm
TS_RE(1)	Receiver wake-up time	From FS to Rx ready	-	280	500	µs
TS_RE2(1)	Receiver wake-up time	From Stby to Rx ready	-	600	900	µs
TS_RE_HOP	Receiver hop time from Rx ready to Rx ready with a frequency hop	200 kHz step	-	400	-	µs
		1MHz step	-	400	-	µs
		5MHz step	-	460	-	µs
		7MHz step	-	480	-	µs
		12MHz step	-	520	-	µs
		20MHz step	-	550	-	µs
		27MHz step	-	600	-	µs
TS_RSSI	RSSI sampling time	From Rx ready	-	-	1/Fdev	s
DR_RSSI	RSSI dynamic Range	Ranging from sensitivity	-	70	-	dB

(1) Information from design and characterization
(2) This reflects the whole receiver bandwidth, as described in sections 3.3.4.1 and 3.3.4.2

2.4.4. Digital Specification

Conditions: Temp = 25 °C, VDD = 3.3 V, crystal frequency = 12.8 MHz, unless otherwise specified.

Table 8: Digital Specification (1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
VIH	Digital input level high		0.8*VDD	-	-	V
VIL	Digital input level low		-	-	0.2*VDD	V
VOH	Digital output level high	Imax=1mA	0.9*VDD	-	-	V
VOL	Digital output level low	Imax=-1mA	-	-	0.1*VDD	V
SCK_CONFIG	SPI Config. clock frequency		-	-	6	MHz
SCK_DATA	SPI data clock frequency		-	-	1	MHz
T_DATA	DATA hold and setup time		2	-	-	µs
T_MOSI_C	MOSI setup time for SPI Config.		250	-	-	ns
T_MOSI_D	MOSI setup time for SPI Data.		312	-	-	ns
T_NSSC_L	NSS_CONFIG low to SCK rising edge. SCK falling edge to NSS_CONFIG high.		500	-	-	ns
T_NSSD_L	NSS_DATA low to SCK rising edge. SCK falling edge to NSS_DATA high.		625	-	-	ns
T_NSSC_H	NSS_CONFIG rising to falling edge.		500	-	-	ns
T_NSSD_H	NSS_DATA rising to falling edge.		625	-	-	ns

(1) Information from design and characterization

Note: on pin 10 (XTAL_P) and 11 (XTAL_N), maximum voltages of 1.8V can be applied.

3. Architecture Description

This section describes in depth the architecture of this ultra low-power receiver:

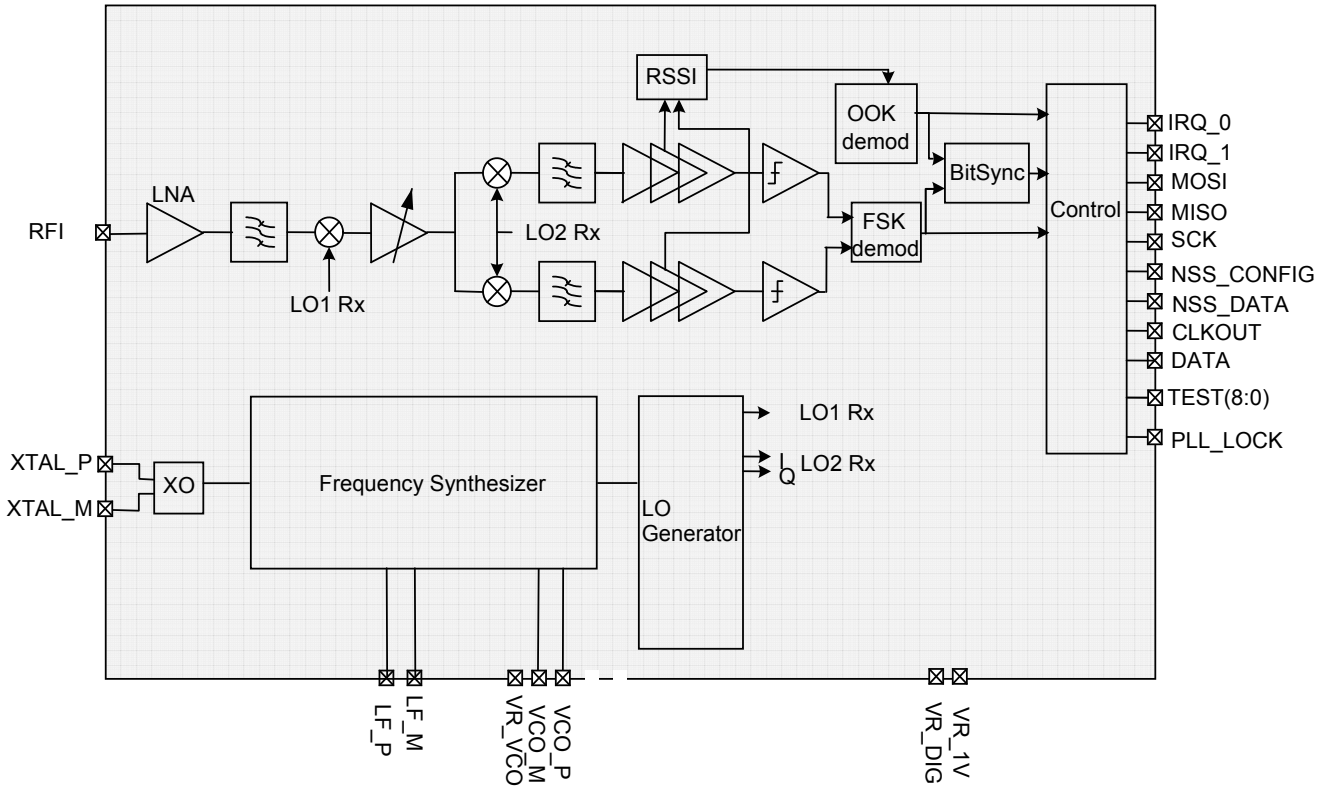

Figure 3: SX1213 Detailed Block Diagram

3.1. Power Supply Strategy

To provide stable sensitivity and linearity characteristics over a wide supply range, the SX1213 is internally regulated. This internal regulated power supply structure is described below:

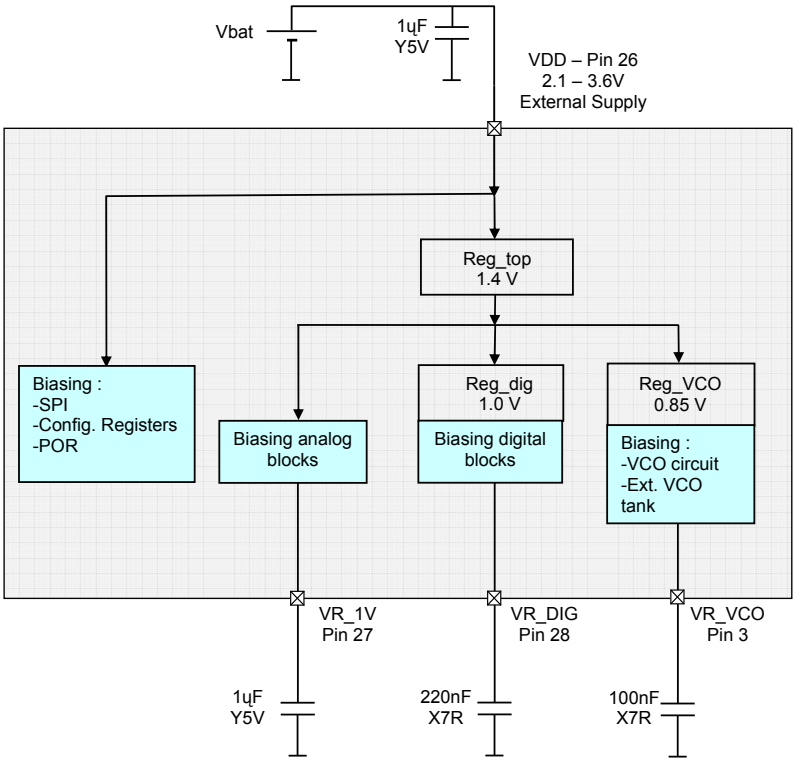

Figure 4: Power Supply Breakdown

To ensure correct operation of the regulator circuit, the decoupling capacitor connection shown in Figure 4 is required. These decoupling components are recommended for any design.

3.2. Frequency Synthesis Description

The frequency synthesizer of the SX1213 is a fully integrated integer-N type PLL. The PLL circuit requires only five external components for the PLL loop filter and the VCO tank circuit.

3.2.1. Reference Oscillator

The SX1213 embeds a crystal oscillator, which provides the reference frequency for the PLL. The recommended crystal specification is given in section 7.1.

3.2.2. CLKOUT Output

The reference frequency, or a sub-multiple of it, can be provided on CLKOUT (pin 19) by activating the bit OSCParam_Clkout_on. The division ratio is programmed through bits OSCParam_Clkout_freq. The two applications of the CLKOUT output are:

- To provide a clock output for a companion uC, thus saving the cost of an additional oscillator. CLKOUT can be made available in any operation mode, except Sleep mode, and is automatically enabled at power-up.
- To provide an oscillator reference output. Measurement of the CLKOUT signal enables simple software trimming of the initial crystal tolerance.

Note: To minimize the current consumption of the SX1213, ensure that the CLKOUT signal is disabled when unused.

3.2.3. PLL Architecture

The crystal oscillator (XO) forms the reference oscillator of an Integer-N Phase Locked Loop (PLL), whose operation is discussed in the following section. Figure 5 shows a block schematic of the SX1213 PLL. Here the crystal reference frequency and the software controlled dividers R, P and S determine the output frequency of the PLL.

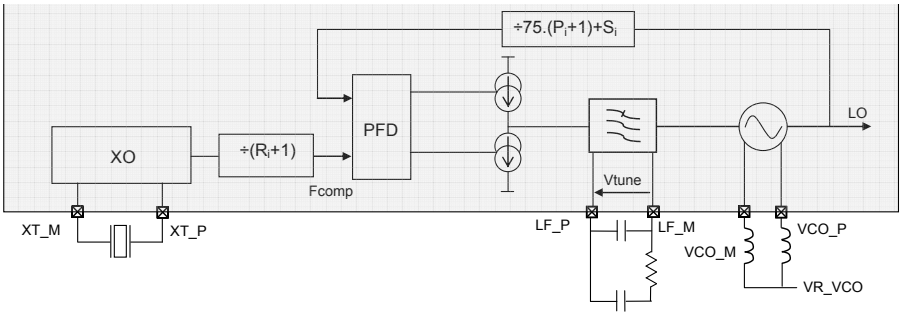

Figure 5: Frequency Synthesizer Description

The VCO tank inductors are connected on an external differential input. Similarly, the loop filter is also located externally. However, there is an internal 8pF capacitance at VCO input that should be subtracted from the desired loop filter capacitance.

The output signal of the VCO is used as the input to the local oscillator (LO) generator stage, illustrated in Figure 6. The VCO frequency is subdivided and used in a series of up (down) conversions for transmission (reception).

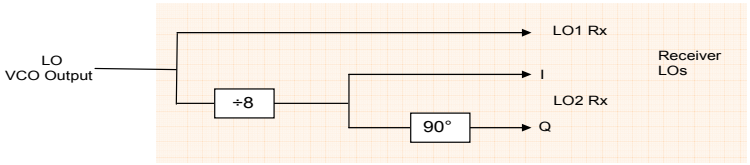

Figure 6: LO Generator

3.2.4. PLL Tradeoffs

With an integer-N PLL architecture, the following criterion must be met to ensure correct operation:

- The comparison frequency, Fcomp, of the Phase Frequency Detector (PFD) input must remain higher than six times the PLL bandwidth (PLLBW) to guarantee loop stability and to reject harmonics of the comparison frequency Fcomp. This is expressed in the inequality:

$$PLLBW \leq \frac{Fcomp}{6}$$

- However the PLLBW has to be sufficiently high to allow adequate PLL lock times
- Because the divider ration R determines Fcomp, it should be set close to 119, leading to Fcomp≈100 kHz which will ensure suitable PLL stability and speed.

With the recommended Bill Of Materials (BOM) of the reference design of section 7.5.3, the PLL prototype is the following:

- 64 ≤ R ≤ 169
- S < P+1
- PLLBW = 15 kHz nominal
- Startup times and reference frequency spurs as specified.

3.2.5. Voltage Controlled Oscillator

The integrated VCO requires only two external tank circuit inductors. As the input is differential, the two inductors should have the same nominal value. The performance of these components is important for both the phase noise and the power consumption of the PLL. It is recommended that a pair of high Q factor inductors is selected. These should be mounted orthogonally to other inductors (in particular the LNA biasing inductor) to reduce spurious coupling between the LNA input and VCO.

For best performance wound type inductors, with tight tolerance, should be used as described in section 7.5.3.

3.2.5.1. SW Settings of the VCO

To guarantee the optimum operation of the VCO over the SX1213's frequency and temperature ranges, the following settings should be programmed into the SX1213:

Freq_band [MHz]	300MHz - 330MHz				320MHz - 350MHz			
L1 and L2	39nH				33 nH			
Subbband	1st quarter	2nd quarter	3rd quarter	4th quarter	1st quarter	2nd quarter	3rd quarter	4th quarter
fo [MHz]	303.75MHz	311.25MHz	318.75MHz	326.25MHz	323.75MHz	331.25MHz	338.75MHz	346.25MHz

Freq_band [MHz]	350MHz - 390MHz				390MHz - 430MHz			
L1 and L2	27nH				22nH			
Subbband	1st quarter	2nd quarter	3rd quarter	4th quarter	1st quarter	2nd quarter	3rd quarter	4th quarter
fo [MHz]	355.00MHz	365.00MHz	375.00MHz	385.00MHz	395.00MHz	405.00MHz	415.00MHz	425.00MHz

Freq_band [MHz]	430MHz - 470MHz				470MHz - 510MHz			
L1 and L2	18nH				15nH			
Subbband	1st quarter	2nd quarter	3rd quarter	4th quarter	1st quarter	2nd quarter	3rd quarter	4th quarter
fo [MHz]	435.00MHz	445.00MHz	455.00MHz	465.00MHz	475.00MHz	485.00MHz	495.00MHz	505.00MHz

Table 9: MCParam_Freq_band and MCParam_Subband Setting

3.2.5.2. Trimming the VCO Tank by Hardware and Software

To ensure that the frequency band of operation may be accurately addressed by the R, P and S dividers of the synthesizer, it is necessary to ensure that the VCO is correctly centered. Note that for the reference design (see section 7.5) no centering is necessary. However, any deviation from the reference design may require the optimization procedure, outlined below, to be implemented. This procedure is simplified thanks to the built-in VCO trimming feature which is controlled over the SPI interface. This tuning does not require any RF test equipment, and can be achieved by simply measuring Vtune, the voltage between pins 6 (LFM) and 7 (LFP).

The VCO is centered if the voltage is within the range:

$$50 \le Vtune(mV) \le 150mV$$

If this inequality is not satisfied then adjust the Trim_band bits from 11 (default value) to 00 whilst monitoring Vtune. This allows the VCO voltage to be trimmed by adding additional capacitance to the VCO tank. Should the desired voltage range be inaccessible, the voltage may be adjusted further by changing the tank circuit inductance value. Note that an increase in capacitance will result in a decrease of Vtune (approximately ~60 mV per step).

Note for mass production: The VCO capacitance is piece to piece dependant. As such, the optimization proposed above should be verified on several prototypes, to ensure that the population is centered on 100 mV.

3.2.6. PLL Loop Filter

To adequately reject spurious components arising from the comparison frequency Fcomp, an external 2nd order loop filter is employed.

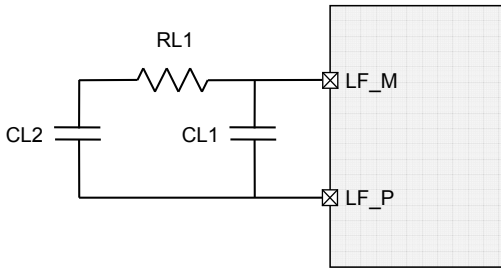

Figure 7: Loop Filter

Following the recommendations made in section 3.2.4, the loop filter proposed in the reference design's bill of material on section 7.5.3 should be used. The loop filter settings are frequency band independent and are hence relevant to all implementations of the SX1213.

3.2.7. PLL Lock Detection Indicator

The SX1213 also features a PLL lock detect indicator. This is useful for optimizing power consumption, by adjusting the synthesizer wake up time (TS_FS), since the PLL startup time is lower than specified under nominal conditions. The lock status can be read on bit IRQParam_PLL_lock, and must be cleared by writing a "1" to this same register. In addition, the lock status can be reflected in pin 23 PLL_LOCK, by setting the bit IRQParam_Enable_lock_detect.

3.2.8. Frequency Calculation

As shown in Figure 5 the PLL structure comprises three different dividers, R, P and S, which set the output frequency through the LO. A second set of dividers is also available to allow rapid switching between a pair of frequencies: R1/P1/S1 and R2/P2/S2. These six dividers are programmed by six bytes of the register MCParam from addresses 6 to 11.

3.2.8.1. FSK Mode

The following formula gives the relationship between the local oscillator, and R, P and S values, when using FSK modulation.

$$Frf, fsk = \frac{9}{8} Flo$$

$$Frf, fsk = \frac{9}{8} \frac{Fxtal}{R+1} \left[75(P+1) + S\right]$$

3.2.8.2. OOK Mode

Due to the low intermediate frequency (Low-IF) architecture of the SX1213 the frequency should be configured so as to ensure the correct low-IF receiver baseband center frequency, IF2.

$$Frf,ook = \frac{9}{8} Flo - IF2$$

$$Frf,ook = \frac{9}{8} \frac{Fxtal}{R+1} \left[75(P+1) + S \right] - IF2$$

Note that from Section 3.3.4, it is recommended that IF2 be set to 100 kHz.

3.3. Receiver Description

The SX1213 is set to receive mode when MCParam_Chip_mode = 011.

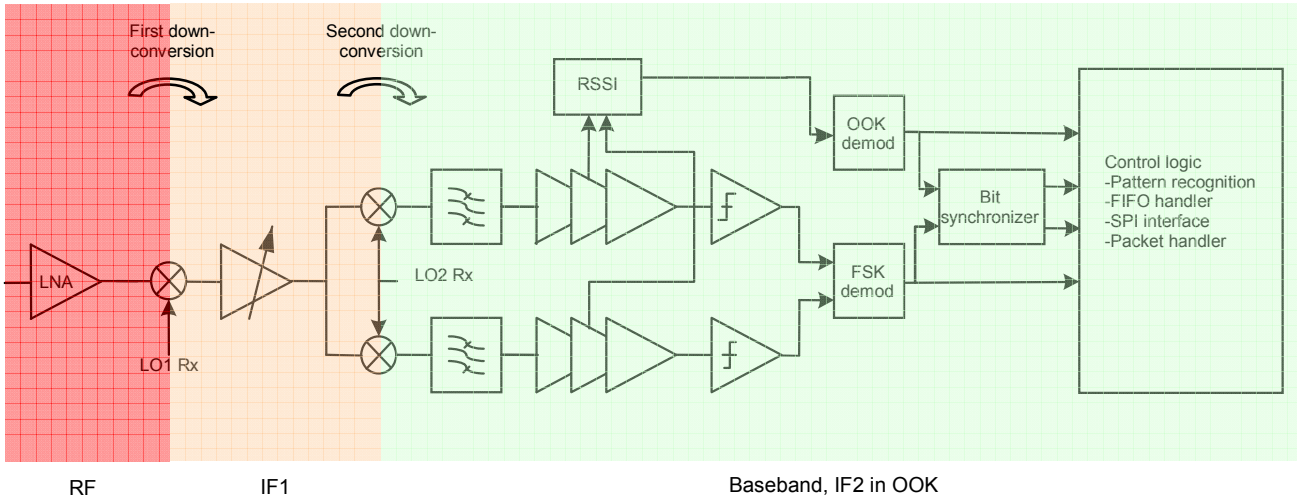

Figure 8: Receiver Architecture

3.3.1. Architecture

The SX1213 receiver employs a super-heterodyne architecture. Here, the first IF is 1/9th of the RF frequency (approximately 100MHz). The second down-conversion down-converts the I and Q signals to base band in the case of the FSK receiver (Zero IF) and to a low-IF (IF2) for the OOK receiver.

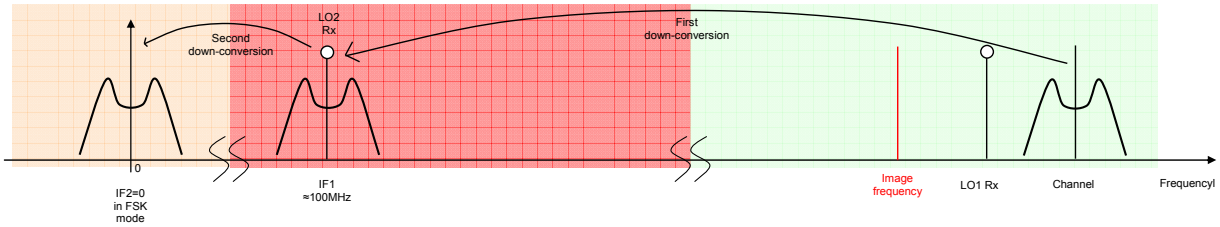

Figure 9: FSK Receiver Setting

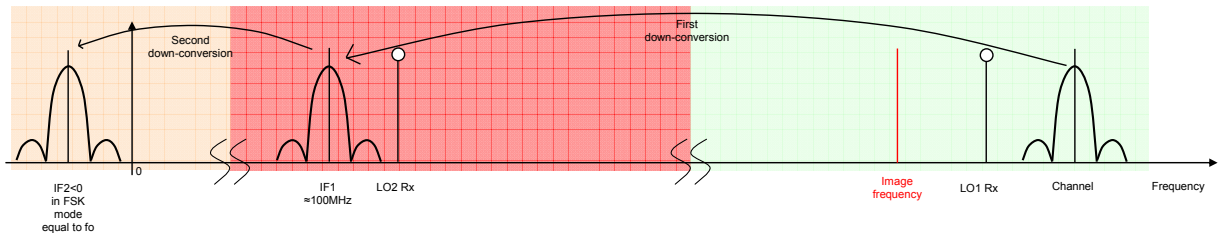

Figure 10: OOK Receiver Setting

After the second down-conversion stage, the received signal is channel-select filtered and amplified to a level adequate for demodulation. Both FSK and OOK demodulation are available. Finally, an optional Bit Synchronizer (BitSync) is provided, to be supply a synchronous clock and data stream to a companion uC in Continuous mode,

or to fill the FIFO buffers with glitch-free data in Buffered mode. The operation of the receiver is now described in detail.

Note: Image rejection is achieved by the SAW filter.

3.3.2. LNA and First Mixer

The performance of this amplifier is such that the Noise Figure (NF) of the receiver can be estimated to be ≈7 dB.

3.3.3. IF Gain and Second I/Q Mixer

Following the LNA and first down-conversion, there is an IF amplifier whose gain can be programmed from -13.5 dB to 0 dB in 4.5 dB steps, via the register MCParam_IF_gain. The default setting corresponds to 0 dB gain, but lower values can be used to increase the RSSI dynamic range. Refer to section 3.3.7 for additional information.

3.3.4. Channel Filters

The second mixer stages are followed by the channel select filters. The channel select filters have a strong influence on the noise bandwidth and selectivity of the receiver and hence its sensitivity. Each filter comprises a passive and active section.

3.3.4.1. Passive Filter

Each channel select filter features a passive second-order RC filter, with a bandwidth programmable through the bits RXParam_PassiveFilt. As the wider of the two filters, its effect on the sensitivity is negligible, but its bandwidth has to be setup instead to optimize blocking immunity. The value entered into this register sets the single side bandwidth of this filter. For optimum performance it should be set to 3 to 4 times the cutoff frequency of the active Butterworth (or polyphase) filter described in the next section.

$$3 * Fc_{ButterfFilt} \leq BW_{passive,filter} \leq 4 * Fc_{ButterFilt}$$

3.3.4.2. Active Filter

The 'fine' channel selection is performed by an active, third-order, Butterworth filter, which acts as a low-pass filter for the zero-IF configuration (FSK), or a complex polyphase filter for the Low-IF (OOK) configuration. The RXParam_PolypFilt_on bit enables/disables the polyphase filter.

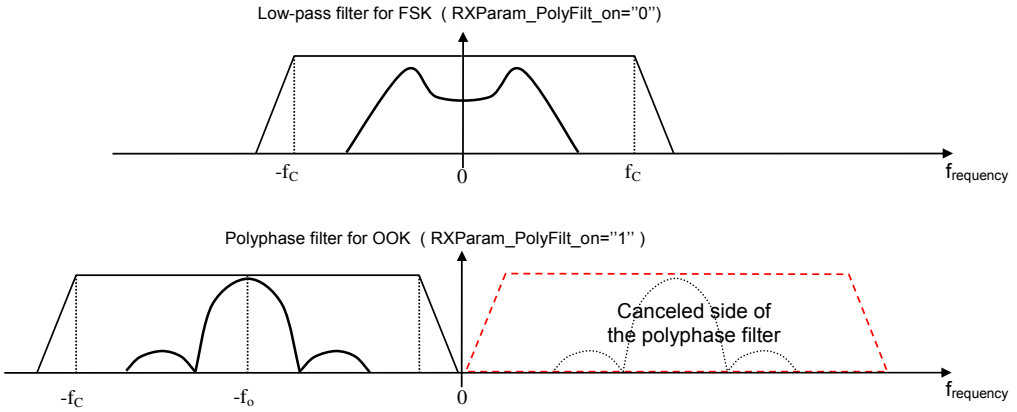

Figure 11: Active Channel Filter Description

As can be seen from Figure 11, the required bandwidth of this filter varies between the two demodulation modes.

- FSK mode: The 99% energy bandwidth of an FSK modulated signal is approximated to be:

$$BW_{99\%,FSK} = 2 * \left[Fdev + \frac{BR}{2} \right]$$

The bits RXParam_ButterFilt set fc, the cutoff frequency of the filter. As we are in a Zero-IF configuration, the FSK lobes are centered around the virtual "DC" frequency. The choice of fc should be such that the modulated signal falls in the filter bandwidth, anticipating the Local Oscillator frequency drift over the operating temperature and aging of the device:

$$2 * fc > BW_{99\%,FSK} + LO_{drifts}$$

Please refer to the charts in section 3.3.5 for an accurate overview of the filter bandwidth vs. setting.

- OOK mode: The 99% energy bandwidth of an OOK modulated signal is approximated to be:

$$BW_{99\%,OOK} = \frac{2}{Tbit} = 2.BR$$

The bits RXParam_PolypFilt_center set fo, the center frequency of the polyphase filter when activated. fo should always be chosen to be equal to the low Intermediate Frequency of the receiver (IF2). This is why, in the GUI described in section 7.2.1 of this document, the low IF frequency of the OOK receiver denoted IF2 has been replaced by fo.

The following setting is recommended:

$$fo = 100kHz$$
$$RXParam\_PolypFilt = "0011"$$

The value stored in RXParam_ButterFilt determines fc, the filter cut-off frequency. So the user should set fc according to:

$$2 * (fc - fo) > BW_{99\%,OOK} + LO_{drifts}$$

Again, fc as a function of RXParam_ButterFilt is given in the section 3.3.6.

3.3.5. Channel Filters Setting in FSK Mode

Fc, the 3dB cutoff frequency of the Butterworth filter used in FSK reception, is programmed through the bit RXParam_ButterFilt. However, the whole receiver chain influences this cutoff frequency. Thus the channel select and resultant filter bandwidths are summarized in the following chart:

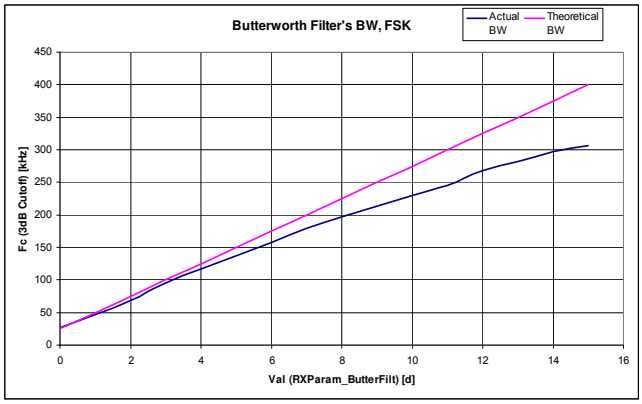

Figure 12: Butterworth Filter's Actual BW

Error! Reference source not found. suggests filter settings in FSK mode, along with the corresponding passive filter bandwidth and the accepted tolerance on the crystal reference.

3.3.6. Channel Filters Setting in OOK Mode

The center frequency, fo, is always set to 100kHz. The following chart shows the receiver bandwidth when changing RXParam_Butterfilt bits, whilst the polyphase filter is activated.

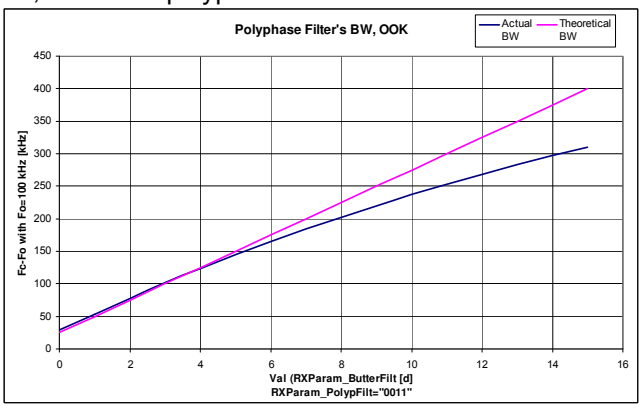

Figure 13: Polyphase Filter's Actual BW

Error! Reference source not found. suggests a few filter settings in OOK mode, along with the corresponding passive filter bandwidth and the accepted tolerance on the crystal reference.

3.3.7. RSSI

After filtering, the In-phase and Quadrature signals are amplified by a chain of 11 amplifiers, each with 6dB gain. The outputs of these amplifiers are used to evaluate the Received Signal Strength (RSSI).

3.3.7.1. Resolution and Accuracy

Whilst the RSSI resolution is 0.5 dB, the absolute accuracy is not expected to be better than +/- 3dB due to process and external component variation. Higher accuracy whilst performing absolute RSSI measurements will require additional calibration.

3.3.7.2. Acquisition Time

In OOK mode, the RSSI evaluates the signal strength by sampling I(t) and Q(t) signals 16 times in each period of the chosen IF2 frequency (refer to section 3.3.1). In FSK mode, the signals are sampled 16 times in each Fdev period, Fdev being the frequency deviation of the companion transmitter. An average is then performed over a sliding window of 16 samples. Hence, the RSSI output register RXParam_RSSI is updated 16 times in each Fdev or IF2 period.

The following settings should be respected:

- FSK Mode: Ensure that the Fdev parameter (as described in MCParam_Fdev) remains consistent with the actual frequency deviation of the companion transmitter.
- OOK reception: Ensure that the Fdev parameter (as described in MCParam_Fdev) is equal with the frequency of I(t) and Q(t) signals, i.e. the second Intermediate Frequency, IF2, of the receiver (Note that this equals Fo, the center frequency of the polyphase filter).

3.3.7.3. Dynamic Range

The dynamic range of the RSSI is over 70 dB, extending from the nominal sensitivity level. The IF gain setting available in MCParam_IF_gain is used to achieve this dynamic range:

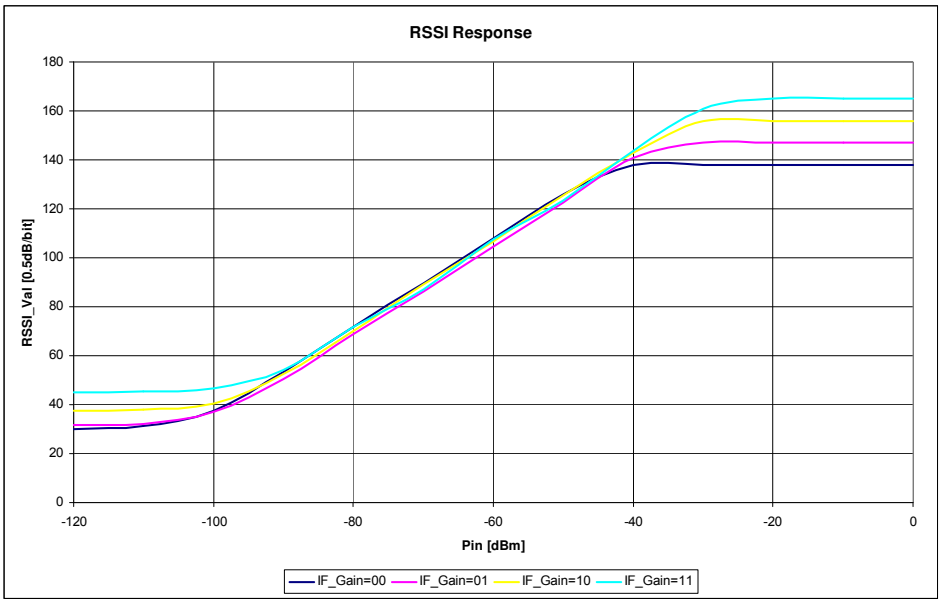

Figure 14: RSSI Dynamic Range

The RSSI response versus input signal is independent of the receiver filter bandwidth. However in the absence of any input signal, the minimum value directly reflects upon the noise floor of the receiver, which is dependant on the filter bandwidth of the receiver.

3.3.7.4. RSSI IRQ Source

The SX1213 can also be used to detect a RSSI level above a pre-configured threshold. The threshold is set in IRQParam_RSSI_irq_thresh and the IRQ status stored in IRQParam_RSSI_irq (cleared by writing a “1”).

An interrupt can be mapped to the IRQ0 or IRQ1 pins via bits IRQParam_Rx_stby_irq0 or IRQParam_Rx_stby_irq1. Figure 15 shows the timing diagram of the RSSI interrupt source, with IRQParam_RSSI_irq_thresh set to 28.

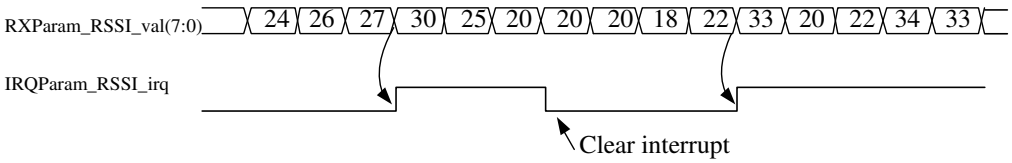

Figure 15: RSSI IRQ Timings

3.3.8. Fdev Setting in Receive Mode

The effect of the Fdev setting is different between FSK and OOK modes:

3.3.8.1. FSK Rx Mode

In FSK mode the Fdev setting, as configured by MCParam_Freq_Dev, sets sampling frequencies on the receiver. The user should make it consistent with the frequency deviation of the FSK signal that is received.

3.3.8.2. OOK Rx Mode

The frequency deviation Fdev, as described above, sets the sampling rate of the RSSI block. It is therefore necessary to set Fdev to the recommended low-IF frequency, IF2, of 100 kHz:

$$Fdev = IF2 = 100kHz$$
$$MCParam\_Freq\_dev = "00000011"$$

3.3.9. FSK Demodulator

The FSK demodulator provides data polarity information, based on the relative phase of the input I and Q signals at the baseband. Its outputs can be fed to the Bit Synchronizer to recover the timing information. The user can also use the raw, unsynchronized, output of the FSK demodulator in Continuous mode.

The FSK demodulator of the SX1213 operates most effectively for FSK signals with a modulation index greater than or equal to two:

$$\beta = \frac{2 * Fdev}{BR} \geq 2$$

3.3.10. OOK Demodulator

The OOK demodulator performs a comparison of the RSSI output and a threshold value. Three different threshold modes are available, programmed through the RXParam_OOK_thresh_type register.

The recommended mode of operation is the “Peak” threshold mode, illustrated below in Figure 16:

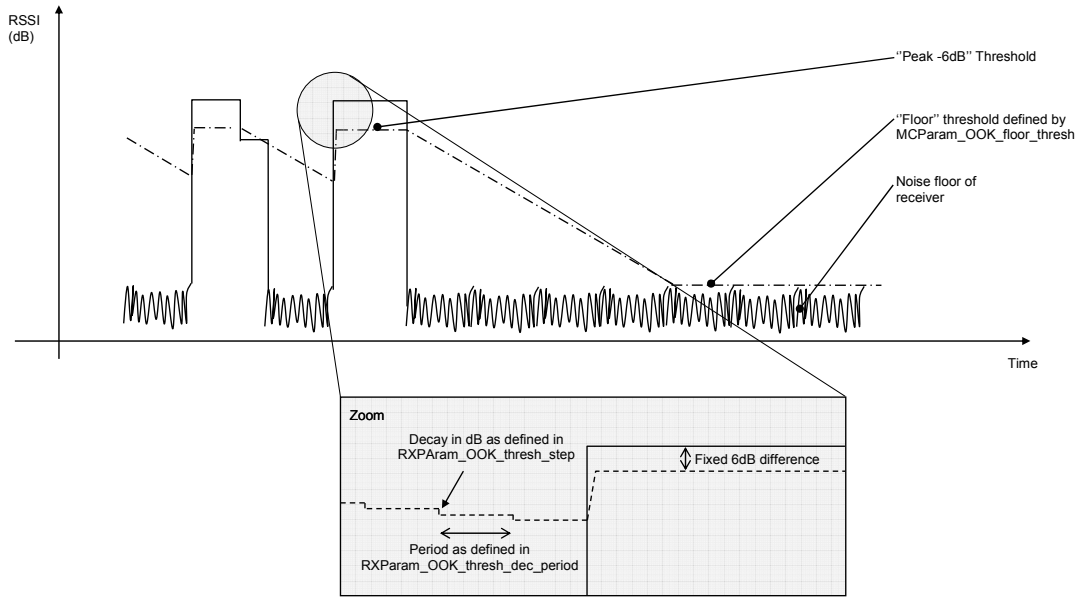

Figure 16: OOK Demodulator Description

In peak threshold mode the comparison threshold level is the peak value of the RSSI, reduced by 6dB. In the absence of an input signal or during the reception of a logical "0", the acquired peak value is decremented by one RXPAram_OOK_thresh_step every RXParam_OOK_thresh_dec_period.

When the RSSI output is null for a long time (for instance after a long string of "0" received, or if no transmitter is present), the peak threshold level will continue falling until it reaches the "Floor Threshold" that is programmed through the register MCParam_OOK_floor_thresh.

The default settings of the OOK demodulator lead to the performance stated in the electrical specification. However, in applications in which sudden signal drops are awaited during a reception, the three parameters shall be optimized accordingly.

3.3.10.1. Optimizing the Floor Threshold

MCParam_OOK_floor_thres determines the sensitivity of the OOK receiver, as it sets the comparison threshold for weak input signals (i.e. those close to the noise floor). Significant sensitivity improvements can be generated if configured correctly.

Note that the noise floor of the receiver at the demodulator input depends on:

- The noise figure of the receiver.
- The gain of the receive chain from antenna to base band.
- The matching - including SAW filter.
- The bandwidth of the channel filters.

It is therefore important to note that the setting of MCParam_OOK_floor_thresh will be application dependant. The following procedure is recommended to optimize MCParam_OOK_floor_thresh.

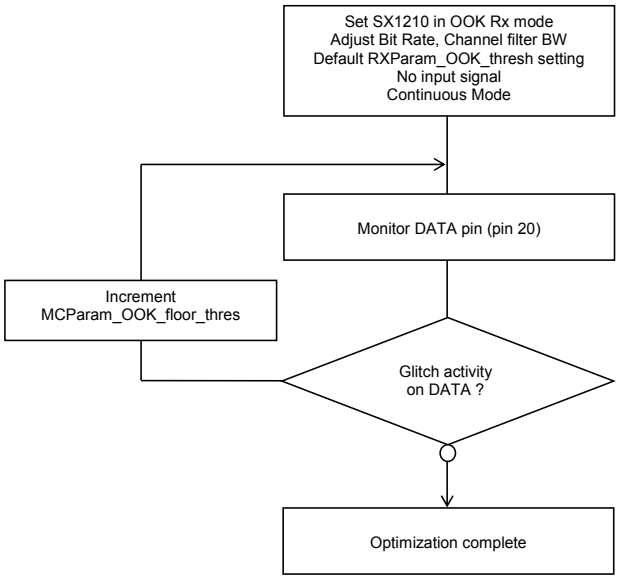

Figure 17: Floor Threshold Optimization

The new floor threshold value found during this test should be the value used for OOK reception with those receiver settings.

Note that if the output signal on DATA is logic “1”, the value of MCParam_OOK_floor_thres is below the noise floor of the receiver chain. Conversely, if the output signal on DATA is logic “1”, the value of MAParam_floor_thres is several dB above the noise floor.

3.3.10.2. Optimizing OOK Demodulator Response for Fast Fading Signals

A sudden drop in signal strength can cause the bit error rate to increase. For applications where the expected signal drop can be estimated the following OOK demodulator parameters RXParam_OOK_thresh_step and RXParam_OOK_thresh_dec_period can be optimized as described below for a given number of threshold decrements per bit RXParam_OOK_thresh_dec_period:

- 000 → once in each chip period (d)
- 001 → once in 2 chip periods
- 010 → once in 4 chip periods
- 011 → once in 8 chip periods
- 100 → twice in each chip period
- 101 → 4 times in each chip period
- 110 → 8 times in each chip period
- 111 → 16 times in each chip period

For each decrement of RXParam_OOK_thresh_step:

- 000 → 0.5 dB (d)
- 001 → 1.0 dB
- 010 → 1.5 dB
- 011 → 2.0 dB
- 100 → 3.0 dB
- 101 → 4.0 dB
- 110 → 5.0 dB
- 111 → 6.0 dB