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SX1233SKA

USER GUIDE



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SX1233SKA USER GUIDE



1 Introduction

The SX1233 is a single-chip integrated circuit ideally suited for today's high performance ISM band RF applications. The advanced feature set, including state of the art packet engine greatly simplifies system design whilst the high level of integration reduces the external BOM to a handful of passive decoupling and matching components. It is intended for use as high-performance, low-cost FSK and OOK RF transceiver for robust frequency agile, half-duplex bi-directional RF links, and where stable and constant RF performance is required over the full operating range of the device down to 1.8V.

The SX1233 is intended for applications over a wide frequency range, including the 433 MHz and 868 MHz European and the 902-928 MHz North American ISM bands. Coupled with a link budget in excess of 135 dB, the advanced system features of the SX1233 include a 66 byte TX/RX FIFO, configurable automatic packet handler, listen mode, temperature sensor and configurable DIOs which greatly enhance system flexibility whilst at the same time significantly reducing MCU requirements.

The SX1233 complies with both ETSI and FCC regulatory requirements and is available in a 5x5 mm QFN 24 lead package

The SX1233-33SKA is a USB based evaluation tool designed to allow simple and easy evaluation of the suitability of the SX1233 for a given application. The low component count reference design implemented in the SM1233 reference design is illustrated below in Figure 1.

It is recommended that this user guide be read in conjunction with the SX1233 datasheet (<u>http://www.semtech.com/images/datasheet/sx1233.pdf</u>)



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ADVANCED COMMUNICATIONS & SENSING



Figure 1: SM1233 with Antenna Diversity Application Schematic



2 Getting Started

2.1 Evaluation Kit Contents

The SX1233SKA evaluation kit consists of:

- 1 x SM1233EXXXB module
- 1 x SM12XX <-> USB-Bridge module
- 1 x ¹/₄ wave monopole antenna
- Installation CD or insert sheet
- 1 x Mini USB cable



Figure 2: SM1233 Module Mounted on USB Bridge

2.2 Installation

- 1. Put the CDROM in your computer and browse the contents of the CD, open the "sx1233starterkitsetup.exe" manually. It can be found in the \Installers sub directory of the CD-ROM
- 2. If the evaluation kit is supplied with an insert sheet, follow the instruction on the insert sheet and download the latest version of the software from the weblink provided
- 3. Follow the on-screen installation guidelines until the process is completed. Please note that .NET Framework 3.5 and the FTDI USB driver will be automatically installed if not detected on your computer
- 4. Connect the SX1233SKA board to the PC via the USB interface. The SM1233 module and USB bridge are powered via the USB
- 5. Launch "SX1233SKA" from the Start menu
- 6. Click on "Connect" button in toolbar or in File menu
- 7. SX1233SKA is now installed and ready to be used

2.3 SX1233SKA Overview

The SX1233SKA features the SM1233 reference design and is also interfaced via the FTDI USB Bridge to the USB type 'A' interface of a host PC.

Transmission and reception is indicated by a pair of LEDs on the USB Bridge.

3 SX1233 Quick Start Guide

It is recommended that this user guide is read in conjunction with the SX1233 datasheet.

- 1. Plug the SX1233SKA into the USB port of the computer. The USB power LED on the bridge should be illuminated
- 2. Run the SX1233 User Interface software: Start > All Programs > SX1233SKA > SX1233SKA
- The SX1233SKA should connect automatically to the User Interface Software. If not, click on the USB connect button, located in the top left hand corner of the window toolbar, as illustrated in Figure 4, below
- 4. Once connected the SX1233SKA shows the default configuration of the SX1233 register settings upon power-up, as illustrated in Figure 3. If the EVK is not connected, the GUI screen is grayed out and an error message is displayed in the bottom left hand corner of the status bar.

4 SX1233SKA Software Description

4.1 Overview

Figure 3 illustrates the SX1233SKA graphical user interface (GUI). Each of the numbered captions corresponds to a proceeding chapter within the sections which corresponds to the description of that GUI feature.





Figure 3: SX1233SKA GUI Overview

4.2 Menu Tool Bar

The Menu toolbar contains four drop down menus, File Menu, Action Menu, Tools Menu and Help Menu.

4.2.1 File Menu

Connect / Disconnect allows for the connection or disconnection of the USB bridge from the host PC. This functionality may also be accessed through the short cut buttons of the Window Toolbar (see Section 4.3).

Open Config... allows for the opening of SX1233SKA configuration files (.cfg). This is implemented through a standard Windows file dialog box and may also be accessed through the short cut buttons of the Window Toolbar.

Save Config allows for SX1233SKA configuration files (.cfg) to be saved. This is implemented through a standard Windows file dialog box. The default file name is the last config file saved.



Save Config as... prompts for a new file name before saving, allowing for multiple configuration files to be saved and may also be accessed through the short cut buttons of the Window Toolbar.

Exit closes the application.

File	
-\$₽	Disconnect
2	Open Config
	Save Config
ø	Save Config As
	Exit

Figure 4: File Menu Options

4.2.2 Action Menu

Reset resets the SX1233 configuration registers to the recommended default values.

Refresh reads the status of the all registers.

Show registers toggles the SX1233 Registers display window and may also be accessed through the short cut buttons of the Window Toolbar. The register display window indicates the status of SX1233 configuration registers as detailed in the SX1233 datasheet. Refer to Section for further information.

Monitor ON allows the GUI to constantly scan the status of the Irq registers RegIrqFlags1 and RegIrgFlags2 at addresses 0x27 and 0x28 respectively, and displays the status on the right hand side of the GUI (see Section 4.6 for further details). Monitor OFF disables the monitor function.



Figure 5: Action Menu Options

4.2.3 Tools Menu

RSSI analyzer provides a graphical representation of the signal level at the antenna port measured within the RX filter channel bandwidth, RxBw, at the programmed RF frequency. Refer to See Section 7.4 for further details.



Spectrum Analyzer provides a simple spectrum analyzer function based upon RSSI level within the programmable RX filter channel bandwidth, RxBw. Please refer to Section 7.5 for further details.

	Tool	s
		RSSI analyser
		Spectrum analyser

Figure 6: Tools Menu Options

4.2.4 Help Menu

Help provides an online description of GUI commands

User's Guide... opens a PDF version of this document.

About... provides details of the GUI revision. The latest version of the SX1233 GUI can be downloaded from the Semtech website.

Help	Help
Help	Image: P
User's Guide	Ļ
About SX1231 Evaluation Kit	₽ e

Figure 7: Help Menu Options

4.3 Window Toolbar

The Windows Toolbar provides three buttons that provide shortcuts to some of the functions accessed from the File drop-down menu.







Open Config button opens a Windows file dialog box to allow access to a previously saved SX1233SKA configuration file (.cfg). Note that saved configuration files are designed to be a useful tool for embedded software development. The file can be opened in any text editor or within a spreadsheet to display the programmed register name, address and contents, as illustrated below in Figure 9.

SX12335	15.cfg - Notepad	
Ele Edit Fg	Yew Help	
Type Reg Reg Reg Reg Reg Reg Reg Reg Reg Re	Yew (Mo) Stor Name Address [Hex] Vai 1fo 0x00 0x01 0x10 0x10 pMode 0x01 0x10 0x10 araModul 0x02 0x00 0x10 itratedmbb 0x03 0x1A 0x10 0x10 itratedmbb 0x05 0x00 0x00 0x1A itratelsb 0x05 0x00 0x52 rfMsb 0x07 0x64 rfMid 0x06 0x40 0x92 1ster1 0x06 0x42 scl 0x0A 0x41 0x40 0x92 1ster1 0x06 0x42 ister1 0x06 0x42 0x44 0x40 0x40 0x92 ister1 0x06 0x42 0x45 1ster3 0x06 0x92 ister1 0x06 0x42 0x44 0x40 0x40 orved15 0x15 0x15 0x40 0x40 0x40 rved14 0x14 0x40 0x	Value[Hex]

Figure 9: Example Configuration File Text Editor Output

Save Config button saves and will prompt if overwriting an existing configuration file.

Connect / Disconnect button allows the user to manage manually connection and disconnection of the kit.

Reset resets the SX1233 configuration registers to the recommended default values.

Refresh reads the status of all registers.

Register Window Toggle toggles the SX1233 Registers display window and may also be accessed through the short cut buttons of the Window Toolbar. The register display window indicates the status of SX1233 configuration registers as detailed in the SX1233 datasheet. Refer to Section 6 for further information.

IRQ Monitor Toggle toggles the scanning of the status of Irq registers *RegIrqFlags1* and *RegIrqFlags2* at addresses 0x27 and 0x28 respectively, and displays the status on the right hand side of the GUI (see Section 4.6 for further details).

Help provides an online description of GUI commands.



4.4 Status Bar

The Status Bar provides details of the SX1233 revision version and current user configuration file. For further information concerning the IC revision, please refer to the SX1233 datasheet.



Figure 10: Status Bar

4.5 Operating Modes Control Box

The Operating Mode control box allows the user to change the operating mode of the SX1233 by clicking on the radio button corresponding to the desired mode. Note that the transition between modes is applied as soon as the radio button is accessed.

When the SX1233 is configured to RX operating mode LED 2 on the USB Bridge is illuminated. When the SX1233 is configured to TX mode both LED 2 and LED 3 are illuminated.

 Sleep Standby Synthesizer Receiver Transmitter 	Operating mode
 Standby Synthesizer Receiver Transmitter 	🚫 Sleep
🔿 Receiver 🔿 Transmitter	💿 Standby 🛛 🔿 Synthesizer
	🔘 Receiver 🛛 🔿 Transmitter

Figure 11: Operating Modes Control Window

4.6 Irq Status Indicator

The Irq Status Flag indicator provides an indication of the status of the Irq registers. When the indicator next to the Irq description is illuminated, the Irq condition is true.

Please refer to the SX1233 datasheet for further information and a more detailed description of the Irq register flags.



Iro flags	
ing nago	ModeReady
	RxReady
	TxReady
	PIILock
	Rssi
	Timeout
. 0	AutoMode
	SyncAddressMatch
	FifoFull
	FifoNotEmpty
	FifoLevel
	Fifo0verrun
	PacketSent
	PayloadReady
	CrcOk
. 0	LowBat

Figure 12: Irq Status Indicator

4.7 Antenna Switch Control Box

The Antenna Switch Control Box allows users to select the RF path between the SX1233 pins and the SMA connectors of the board; as illustrated in figure 13. Practically, RX input and TX outputs could be connected to either SMA connector according to the user's selection. Pins 18 and 20 of the POD_IN header allow external control of the switch logic.

Antenna switch control Selection: Pin PA_BOOST Pin RFI0 Pin PA_BOOST Pin PA_BOOST Pin PA_BOOST Pin PA_BOOST Pin PA_BOOST Pin RF_IO Pin RFIO Pin RFIO

Figure 13: Antenna Switch Control Window



5 Configuration Registers Tabs

Unless otherwise stated all registers are updated as soon as they are written. It is recommended to cycle through Standby Mode when changing the contents of configuration registers.

5.1 Common Configuration Registers Tab

The Common Configuration Registers tab is illustrated on the following page in Figure 14. Please refer to the SX1233 for a full description of the configuration register functions.

General		Listen mode	
RF frequency: Bitrate: Fdev: • Sequencer: Bit synchronizer / data mode	115000000	Listen mode: Listen resolution idle: Listen resolution Rx: Listen criteria:	O N O DFF 4100 μs 64 μs •> RssiThreshold >> RssiThreshold Rix & Mode after IRQ
Modulation	O DFF- Continous	Listen Rx time:	2.048 Sms
Modulation: Modulation shaping:	 FSK 0 DDK DFF Gaussian filter, BT = 1.0 Gaussian filter, BT = 0.5 Gaussian filter, BT = 0.3 	Antenna switch control	Pin PA_BOOST <=> RF_PA Pin RFIO <=> RF_IO O Pin PA_BOOST <=> RF_IO Pin RFIO <=> RF_PA
Ossillators XO Frequency: RC oscillator calibration:	32'000'000 🔷 Hz	Battery management Low battery detector: Low battery threshold trim: Low battery indicator	ON OFF

Figure 14: Common Configuration Register Tab

Configuration register value entries can be selected from the drop down menus within the tab or entered manually within the tab fields. Note that an invalid register entry will be highlighted by an orange background and the GUI will automatically flag a warning exclamation. A valid register entry that leads to an incorrect operating setting will result in that entry to be highlighted in red. Hovering a mouse or cursor over the warning provides an explanation for the flag, as illustrated in Figure 15.

Values entered manually that do not coincide with an exact configuration will be automatically updated by the GUI to the next valid register configuration and write that value to the appropriate configuration register.



General							
RF frequency:		915,000,000	•	Hz			
Bitrate:		4,800	*	bps			
Fdev:	+/-	1,160	*	Hz 🚺			
Sequencer:		💿 ON 🔿 OFF		The m The v	odulation index is (alid range is [0.5, 1	out of range. [0]	
General				,			
General RF frequency:		915,000,000	*	Hz			
General RF frequency: Bitrate:		915,000,000	* *	Hz bps			
General RF frequency: Bitrate: Fdev:	+/-	915,000,000 4,800 488	<>	Hz bps Hz 📵			

Figure 15: Dialog Box Error Messages

5.1.1 Modulation Mode Window

Clicking on the OOK radio button within the Modulation window will access the modulation shaping options for the OOK modulation mode.

Modulation		Modulation	
Modulation:	💿 FSK 🔿 OOK	Modulation:	🔿 FSK 💿 OOK
Modulation shaping:	OFF	Modulation shaping:	OFF
	🔘 Gaussian filter, BT = 1.0		Filtering with fCutOff = BR
	🔘 Gaussian filter, BT = 0.5		Filtering with fCutOff = 2 * BR
	🔘 Gaussian filter, BT = 0.3		



5.2 Transmitter Configuration Register Tab

The Transmitter Configuration Register Tab is illustrated below in Figure 17. Please refer to the SX1233 datasheet for a full description of the configuration register functions. Configuration register value entries can be selected from the drop down menus within the tab or entered manual within the tab fields. If values are entered manually that do not coincide with an exact configuration, the GUI will automatically update the displayed value to the next valid register configuration and write that value to the appropriate configuration register.

It should be noted that the output power settings are the nominal values determined by the configuration registers and does not refer to measured output power. Please refer to the Application Information within the SX1230 datasheet for further information concerning measured output power vs. programmed power.



Transmitter				
	- Power Amplifier			
	PA0 -> Trans	mits on pin RFIO		
	○ PA1 -> Trans	smits on pin PA_BOOS	т	
	○ PA1 + PA2 -	> Transmits on pin PA	_BOOST	
	PA ramp:	40	μs	
	Output power			
		13	dBm	
	Overload current protection			
		💿 ON (OFF	
	Trimming:	95	🗢 mA	

Figure 17: Transmitter Configuration Register Tab

5.3 Receiver Configuration Register Tab

The Transmitter Configuration Register Tab is illustrated below. Please refer to the SX1233 for a full description of the configuration register functions.

Configuration register value entries can be selected from the drop down menus within the tab or entered manual within the tab fields. If values are entered manually that do not coincide with an exact configuration, the GUI will automatically update the displayed value to the next valid register configuration and write that value to the appropriate configuration register.

		5.3.3
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Receiver Lna sensitivitu AFC low beta: O ON 💿 OFF 0 50 DCC frequency: 207 🗘 Hz Input impedance: ohms 200 AFC low beta offset: 0 * Hz 5,208 🗘 Hz Rx filter bandwidth: Sensitivity boost: 🔘 ON 💿 OFF AFC auto clear: 🔿 ON 💿 OFF AFC auto: 🔘 ON 💿 OFF AFC bandwidth AFC: Start Clear 0 🕘 Hz DCC frequency: 249 🗘 Hz DAGC: 💿 ON 🔘 OFF Read 0 Hz FEI: 25.000 🗘 Hz Bx filter bandwidth: 5.3.5 5.3.1 -Timeout Bx start: ms Threshold type: Peak ~ Timeout threshold: 0 \$ ms Peak threshold step: 0.5 🗢 dB Auto threshold: 💿 ON 🔿 OFF Peak threshold dec: Once per chip ~ Threshold: dBm Avg threshold cutoff: 5.3.4 -117.0**a** dBr Value 😂 dB Fixed threshold: 6 5.3.2 Restart Rx 💿 Auto 🔘 Manual Phase Reference Threshold 1 Threshold 2 Threshold 3 Threshold 4 Threshold 5 AGC -111 -95 -88 -77 -68 -57 -> Pin [dBm] G2 G5 G1 G3 G4 G6 Gain: 💿 Auto 🔘 Manual

Figure 18: Receiver Configuration Register Tab

5.3.1 Rx Bandwidth

The Rx Bandwidth, RxBw, window is illustrated below. For optimum performance in FSK mode when operating with a modulation index \geq 2, the DCC frequency is recommended to be approximately 4% of the receiver bandwidth, RxBw. The GUI will automatically set the appropriate DCC frequency based upon the setting of RX filter bandwidth.

Rx bandwidth		
DCC frequency:	414	🗘 Hz
Rx filter bandwidth:	10,417	🗘 Hz
AFC bandwidth		
DCC frequen <mark>cy:</mark>	497	🗘 Hz
Rx filter bandwidth:	50,000	🗘 Hz

Figure 19: Rx Bandwidth Window

For operation with low modulation index signals, it is recommended that the user follows the recommendations for setting the correct DCC bandwidth that can be found in the SX1233 datasheet.

5.3.2 LNA Gain Window

The LNA gain window provides the status of the configured LNA gain. The gain can be configured automatically or manually. In automatic mode the LNA gain is set based upon the RSSI value. In manual mode, the gain should be set according to the expected signal power.

Note that the AGC reference threshold is set according to:

AgcRef = [-174 + NF + 10*log(2*RxBw) + DemodSNR + FadingMargin] dBm



Figure 20: LNA Gain Window

5.3.3 AFC / FEI

The AFC / FEI (Frequency Error Indicator) window is illustrated below. Note that when AFC is activated (either AFC auto "ON" or manually), the RF frequency in the General window of the Common Configuration Register Tab does not update, although a measure of frequency error can be obtained by clicking on the FEI Read button to verify correct AFC operation.

Enabling AFC low beta implements a double AFC function to offset the local oscillator of the SX1233 to ensure that the central tone at f_0 associated with low modulation index signals is not unduly attenuated by the cut-off frequency of the DCC.

Please refer to the optimized set up for low modulation index systems section of the SX1233 datasheet for further details.

AFC / FEI				
AFC low beta:	🔿 ON	💿 OFF		
AFC low beta offset:	0	*		Hz
AFC auto clear:	🔿 ON	📀 OFF		
AFC auto:	🔘 ON	💿 OFF		
AFC: Start Clear	0		۲	Hz
FEI: Read	0		0	Hz

Figure 21: AFC / FEI Window

5.3.4 RSSI

The RSSI window provides access to the RSSI timeout and timeout threshold functions and enable either automatic or manual RSSI detection threshold values to be programmed. Note that the RSSI threshold (which should not be confused with the LNA or AGC threshold) can be calculated from and equates to the effective noise floor of the receiver for a given filter bandwidth.

RSSIthres = [-174 + NF + 10*log(2*RxBw) + DemodSNR] dBm



RSSI		
Timeout Rx start:	0	ms
Timeout threshold:	0	ms
Auto threshold:	💿 ON 🔘 OFF	
Threshold:	-116.0	dBm
Value:	-127.5 📀	dBm
Phase: Restart Rx	💿 Auto i 🔘 Manual	

Figure 22: RSSI Window

5.3.5 Continuous-Time Digital AGC

The AGC dynamic range can be enhanced in V2c silicon (chip version 2.3) with the default mode of operation of DAGC enabled. Note that the DAGC mode of operation is automatically configured by the GUI depending upon whether AFC low beta is enabled (see section 5.3.3).

Pease refer to the SX1233 datasheet for further information on the implementation of the continuous-time DAGC function.

-DAGC	
DAGC:	💿 ON 🔘 OFF

Figure 23: DAGC Window

5.4 Irq & Mapping Configuration Register Tab

The Irq & Mapping Configuration Register Tab is illustrated in Figure 24. Please refer to the SX1233 for a full description of the irq and mappings for each mode of operation of the SX1233.

Configuration register value entries can be selected from the drop down menus besides each DIO listed.

Note that when necessary the GUI will automatically re-configure DIO mappings (i.e. Packet Handler operation).

Please refer to Table 1 and Table 2, below, for the available DIO mappings of the SX1233 in continuous and packet mode, respectively.

Mode	DIOx	DIO5	DIO4	DIO3	DIO2	DIO1	DIO0
	Mapping						



Sloop	00	-	-	-	-	-	-
	01	-	-	-	-	-	-
Sleep	10	LowBat	LowBat	AutoMode	-	LowBat	LowBat
	11	ModeReady	-	-	-	-	ModeReady
	00	ClkOut	-	-	-	-	-
Standby	01	-	-	-	-	-	-
Stanuby	10	LowBat	LowBat	AutoMode	-	-	LowBat
	11	ModeReady	-	-	-	LowBat	ModeReady
	00	ClkOut	-	-	-	-	PIILock
EQ	01	-	-	-	-	-	-
F3	10	LowBat	LowBat	AutoMode	-	LowBat	LowBat
	11	ModeReady	PIILock	-	-	PIILock	ModeReady
	00	ClkOut	Timeout	Rssi	Data	Dclk	SyncAddr
DV	01	Rssi	RxReady	RxReady	Data	RxReady	Timeout
	10	LowBat	SyncAddr	AutoMode	Data	LowBat	Rssi
	11	ModeReady	PIILock	Timeout	Data	SyncAddr	ModeReady
	00	ClkOut	TxReady	TxReady	Data	Dclk	PIllock
ту	01	ClkOut	TxReady	TxReady	Data	LowBat	TxReady
	10	LowBat	LowBat	AutoMode	Data	LowBat	LowBat
	11	ModeReady	PIILock	TxReady	Data	PIILock	ModeReady

Table 1: Continuous Mode DIO Mappings

Mode	DIOx	DIO5	DIO4	DIO3	DIO2	DIO1	DIO0
	Mapping						
Clean	00	-	-	FifoFull	FifoNotEmpty	FifoLevel	-
	01	-	-	-	-	FifoFull	-
Sleep	10	LowBat	LowBat	LowBat	LowBat	FifoNotEmpty	LowBat
	11	ModeReady	-	-	AutoMode	-	-
	00	Clkout	-	FifoFull	FifoNotEmpty	FifoLevel	-
Standby	01	-	-	-	-	FifoFull	-
Stanuby	10	LowBat	LowBat	LowBat	LowBat	FifoNotEmpty	LowBat
	11	ModeReady	-	-	AutoMode	-	-
	00	Clkout	-	FifoFull	FifoNotEmpty	FifoLevel	-
ES	01	-	-	-	-	FifoFull	-
го	10	LowBat	LowBat	LowBat	LowBat	FifoNotEmpty	LowBat
	11	ModeReady	PIILock	PIILock	AutoMode	PIILock	PIILock
	00	Clkout	Timeout	FifoFull	FifoNotEmpty	FifoLevel	CrcOk
DV	01	Data	Rssi	Rssi	Data	FifoFull	PayloadReady
	10	LowBat	RxReady	SyncAddr	LowBat	FifoNotEmpty	SyncAddr
	11	ModeReady	PIILock	PIILock	AutoMode	Timeout	Rssi
	00	Clkout	ModeReady	FifoFull	FifoNotEmpty	FifoLevel	PacketSent
ту	01	Data	TxReady	TxReady	Data	FifoFull	TxReady
	10	LowBat	LowBat	LowBat	LowBat	FifoNotEmpty	LowBat
	11	ModeReady	PIILock	PIILock	AutoMode	PLLlock	PIILock

Table 2: Packet Mode DIO Mappings



IRQ & Map		
Device status		
Bit Synchronizer:	ON	
Data mode:	Packet	
Uperating mode:	Receiver	
DIO mapping		
DIU5:	Timout	
DI04:		
DIO3:	FitoFull 🗸	
D102:	FifoNotEmpty V	
DIO1:	FifoLevel	
D100:	CrcOk 🗸	
Clock out		
Frequency:	OFF 🖌 Hz	

Figure 24: Irq & Mapping Configuration Register Tab

5.5 Packet Handler Configuration Register Tab

The Packet Handler Configuration Register Tab is shown below. Please refer to the SX1233 for a full description of the packet engine message format and operation of the SX1233.

551	_	Packet	Handler							
0.0.1	Preamble size:	3		bytes Ac	ldress based filtering:	💿 OFF	Node 🔿 Node or Broadcast			
	Sync word:	💿 ON 🔿 OFF		No	ode address:	0	0x00			
	FIFO fill condition:	💿 Sync address 🔘	Always	Br	oadcast address:	0	\$ 0x00			
	Sync word size:	4		bytes D0	C-free:	💿 OFF	Manchester 🔘 Whitening			
	Sync word tolerance:	0		bits CF	RC calculation:	💿 ON	◯ OFF			
	Sync word value:	01-01-01-01		CF	RC auto clear:	📀 ON	O OFF			
	Packet format:	🔿 Variable 💿 Fixed		AE	S:	🔿 ON	⊙ OFF			
	Payload length:	20 💲 0x14		bytes AE	S key:	00-0	00-00-00-00-00-00-00-00-00-00-00-00-00-			
	Intermediate mode enter:	None (Auto Modes OF	F) 💊	Z Tx	: start:	🔘 Fifo	Level 💿 FifoNotEmpty			
	Intermediate mode exit:	None (Auto Modes OF	F) 📘	E FIF	FO Threshold:	15	\$			
	Intermediate mode:	Sleep	1	/ Int	er packet Rx delay:	0.208	ms			
5.5.2	Packet									
	Preamble	Sync	Length	Node Addres	s Message	CRC	Bit Synchronizer: ON			
	55-55-55	01-01-01-01				AD-F8	Data mode: Packet	553		
	Message						Control	5.5.5		
	53 65 6D 74 65 6	HEXADECIMAL 53 65 6D 74 65 63 68 20 54 65 73 74 20 50 6 6C 6F 61 64					Start Log			
	6C 6F 61 64						By packets:			
						~				
	0							l		

Figure 25: Packet Handler Configuration Register Tab



5.5.1 Sync Word

For correct packet mode operation, the sync word needs to be set to at least one byte. Note that 0x00 can not be set as for the first byte of the sync word. The GUI will prompt with an error message should the user attempt to set 0x00 in the first byte of the sync word.

5.5.2 AutoMode Operation

Auto Modes defines the enter conditions to start the packet handler and exit conditions to terminate packet handler operation, as defined in the SX1233 datasheet.

5.5.3 Packet Log

Clicking on the Log button within the Control Window enables the payload logging function, available in both TX and RX modes whenever the Packet Handler is enabled.

Status Bar Log control Max samples: 10 Browse Start		5 Packet Log
	Status Bar	Log control Max samples: 10 Browse Start

Figure 26: Packet Logger Window

In the Packet Logger window enter the number of packets to be logged and press the Start button. Then press the Start button in the Control Window of the main Packet Handler Tab to start packet transmission or reception. When the status bar indicates full, the log can be saved by clicking on the Browse button.

The log file can be viewed in Notepad or opened in Excel as a .CSV file

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1	# 3	SX1231	packet	log ge	enerated t	he 1/2	5/2011 at 05:46	PM											-
2	# "	Time	Mode	Rssi	Pkt Max	Pkt #	Preamble Size	Sync	Length	Node Address	Message							CRC	
3		46:52.3	Τ×		10	0	3	01-01-01-01	14		53-65-6D-	74-65-63	68-20-54-	35-73-74	1-20-50-6	I-79-6C	-6F-61-64	AD-F8	
4		46:52.4	Tx		10	1	3	01-01-01-01	14		53-65-6D-	74-65-63	68-20-54-	65-73-74	1-20-50-61	I-79-6C	-6F-61-64	AD-F8	
5		46:52.5	Τx		10	2	3	01-01-01-01	14		53-65-6D-	74-65-63-	68-20-54-	35-73-74	1-20-50-61	I-79-6C	-6F-61-64	AD-F8	
6		46:52.6	Τx		10	3	3	01-01-01-01	14		53-65-6D-	74-65-63-	68-20-54-	35-73-74	1-20-50-6	-79-6C	-6F-61-64	AD-F8	
. 7.		46:52.7	Tx		10	4	3	01-01-01-01	14		53-65-6D-	74-65-63	68-20-54-	35-73-74	1-20-50-61	-79-6C	-6F-61-64	AD-F8	
8		46:52.8	Τx		10	5	3	01-01-01-01	14		53-65-6D	74-65-63	68-20-54-	35-73-74	1-20-50-6	-79-6C	-6F-61-64	AD-F8	
9		46:53.0	Tx		10	6	3	01-01-01-01	14		53-65-6D-	74-65-63	68-20-54-	35-73-74	1-20-50-61	-79-6C	-6F-61-64	AD-F8	
10		46:53.1	Tx		10	7	3	01-01-01-01	14		53-65-6D-	74-65-63	68-20-54-	35-73-74	1-20-50-6	I-79-6C	-6F-61-64	AD-F8	
11		46:53.2	Тx		10	8	3	01-01-01-01	14		53-65-6D-	74-65-63-	68-20-54-	65-73-74	1-20-50-61	-79-6C	-6F-61-64	AD-F8	
12		46:53.3	Τx		10	9	3	01-01-01-01	14		53-65-6D-	74-65-63	68-20-54-	35-73-74	1-20-50-6	-79-6C	-6F-61-64	AD-F8	
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Figure 27: Packet Log CSV File Format

Packet Log Parameter	Description
Time	Local (CPU) timestamp in MM:SS.S format for TX / RX packets
Mode	SX1233 Packet Mode
RSSI	Indicated RSSI level (RX mode only)
Pkt Max	Number of repeated packets set in GUI Control Window (0 = infinite)
Pkt #	Transmitted or received packet number
Preamble Size	Size of transmitted or received preamble sequence
Sync	Sync Address
Length	Payload length of TX / RX packet
Node Address	node Address (optional)
Message	Transmitted / received packet (can be viewed in GUI Message Window)
CRC	Transmitted / received CRC (optional)

Table 3: Packet Log Descriptors

5.5.4 Packet Handler GUI Limitations

When operating the packet handler via the SKA GUI, the user should be aware of the following limitations associated with the GUI:

- Minimum Preamble Size = 2 bytes
- Maximum Packet Length = 66 bytes (64 bytes of data + Length byte + Address byte)

5.6 Temperature Configuration Register Tab

The Temperature Configuration Register Tab is illustrated below in Figure 29. Note that user is prompted to calibrate the SX1233 temperature sensor by clicking on the Calibrate button to access the temperature calibration dialog box.



Figure 28: Temperature Calibration Dialog Box

When the temperature sensor has been calibrate the temperature, as computed by the SX1233, will be displayed, as illustrated in Figure 29.





Figure 29: Calibrated Temperature Sensor Tab