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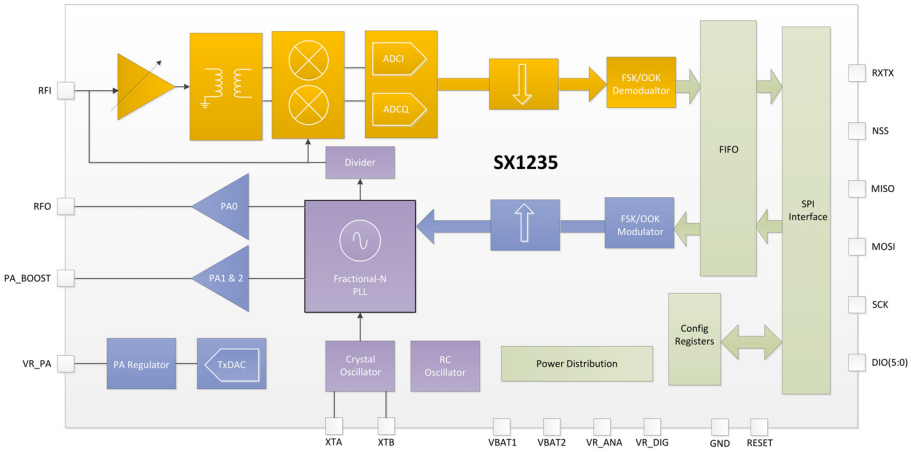
SX1235 Transceiver

EN300 220 Category 1 Compliant Transceiver



GENERAL DESCRIPTION

The SX1235 is a highly integrated RF transceiver optimized for operation compliant with ETSI EN 300 220 receiver category 1. In conjunction with an external SAW filter the SX1235 is designed to pass the category 1 testing with substantial regulatory margin, simplifying end-user production test requirements. The SX1235 retains the highly integrated architecture of the SX123x family, minimizing external components while delivering the highest level of performance. For hybrid systems with non category 1 elements within an alarm system the SX1235 offers the advantage of programmable narrow-band and wide-band communication modes without the need tomodify external components. This makes the SX1235 suitable for integrated home automation, security and alarm systems that require legacy compatibility.

APPLICATIONS

- Category 1 Social Alarm Systems
- Category 1 Fire, Smoke and Toxic Gas Detection
- Category 1 Lone Worker Systems
- Home and Building Automation
- Wireless Alarm and Security Systems
- Industrial Monitoring and Control

MARKETS

- Optimised for the EN 300-220-1 Category 1
- North America: FCC Part 15 and Japan: ARIB T-108

KEY PRODUCT FEATURES

- High sensitivity: down to -123 dBm at 1.2 kbps
- High selectivity: 60 dB typ. ACR
- High linearity: 50 dB typ. of adjacent channel saturation
- 80 dB Blocking immunity, 100 dB with SAW
- Image rejection of over 45 dB
- Low current: Rx = 9.3 mA, 100nA register retention
- Programmable output power +20 dBm in 1 dB steps
- Optional high efficiency or fully regulated PA connections for reliable M2M performance and optimal battery lifetime
- Voltage operation from 1.8 to 3.7 V
- Narrowband integrated synthesizer with a resolution of 61 Hz
- FSK, GFSK, MSK, GMSK and OOK modulation
- Automated, fast frequency correction & timing recovery
- Over 115 dB Dynamic Range RSSI
- Packet engine with CRC 64 byte FIFO
- Preamble and RSSI based channel activity detection

ORDERING INFORMATION

Part Number	Package	Delivery	MOQ / Multiple
SX1235IMLTRT	QFN24	Tape & Reel	3000 pieces

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This product datasheet contains a detailed description of the SX1235 performance and functionality. Please consult the Semtech website for the latest updates or errata.

1. General Description

The SX1235 is a single-chip integrated transceiver circuit that is optimized for EN 300 220-1 category 1 receiver applications. The fully integrated architecture of the transceiver is combined with an automated packet engine and top level sequencer. In conjunction with a 64 byte FIFO these automate the entire process of packet transmission, reception and acknowledgement without incurring the consumption penalty common to many transceivers that feature an on-chip MCUs. Being easily configurable, it greatly simplifies system design and reduces external MCU workload to a minimum. The small external BOM is limited to a quartz crystal frequency reference, passive decoupling, matching and filtering components.

SX1235 is intended for use as a high-performance, low-cost, FSK and OOK RF transceiver for robust, frequency agile, half-duplex, bidirectional RF links. Where stable and constant RF performance is required over the full operating range of the device down to 1.8 V the receiver and PA are fully regulated. For transmit intensive applications - a high efficiency PA can be selected to optimize the current consumption.

The SX1235 features high receiver sensitivity and low receive current, equating to a high link budget, 143dB (-123dBm sensitivity in conjunction with +20dBm Pout) and long battery life. The SX1235 complies with both ETSI and FCC regulatory requirements and is available in a 5 x 5 mm QFN 24 lead package.

1.1. Simplified Block Diagram

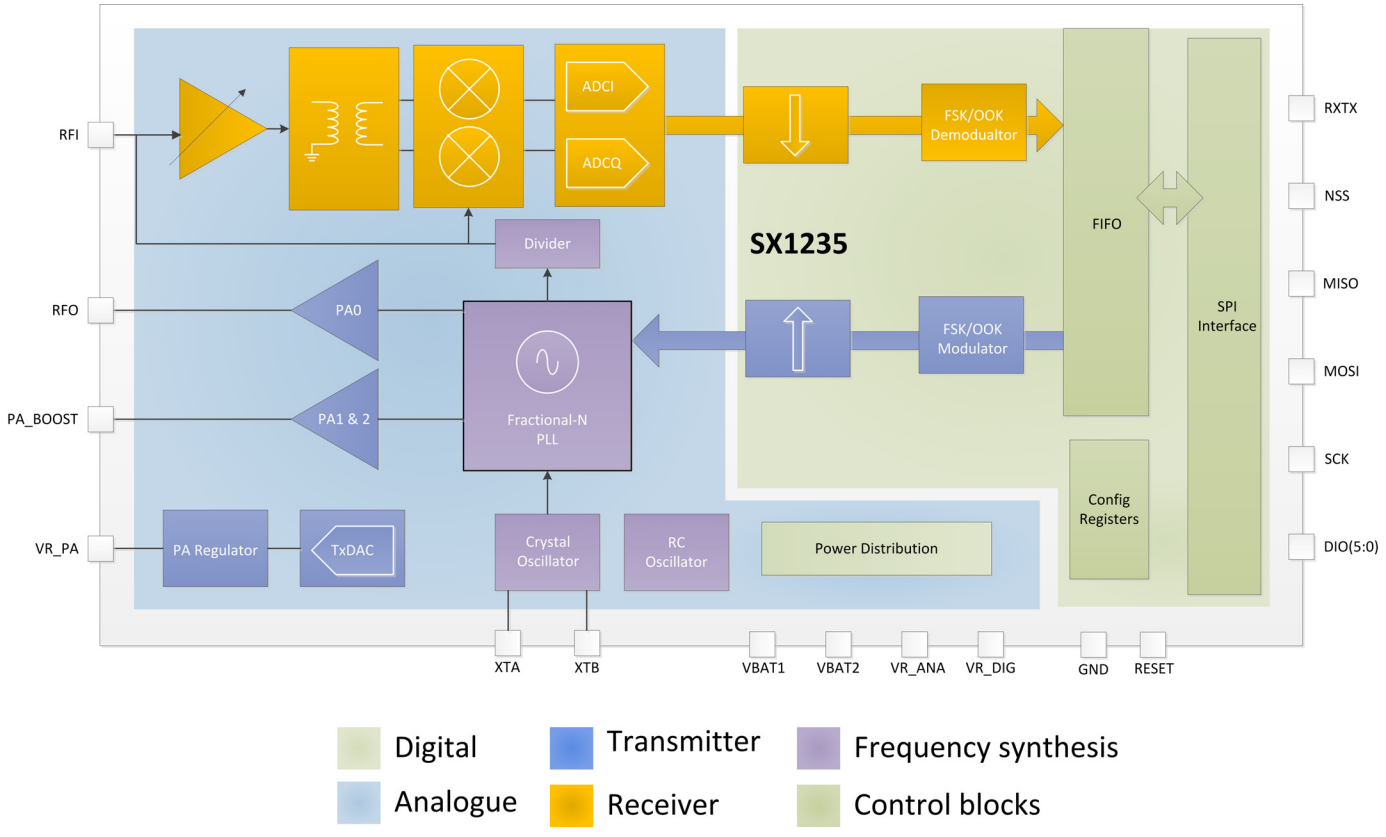

Figure 1. Block Diagram

1.2. Pin and Marking Diagram

The following diagram shows the pin arrangement of the QFN package, top view.

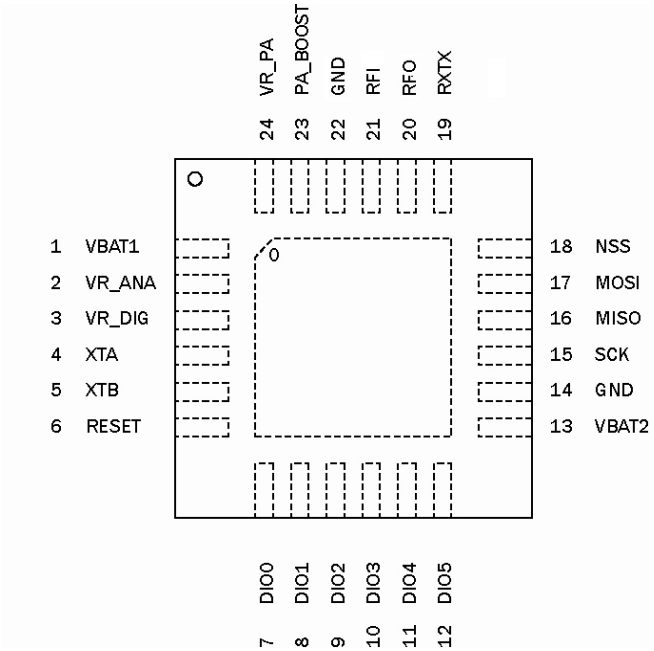

Figure 2. Pin Diagram

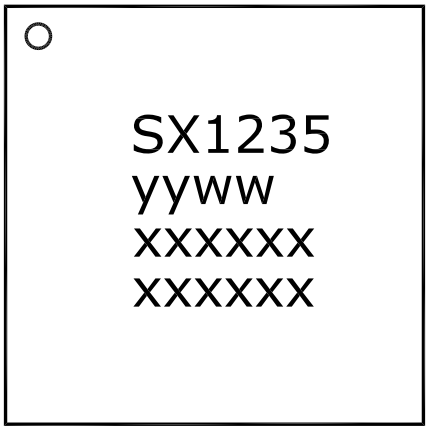

Figure 3. Marking Diagram

Notes yyww indicates the date code

xxxxxx.xxxxxx refers to the lot number

1.3. Pin Description

Table 1 SX1235 Pinouts

Number	Name	Type	Description
0	GROUND	-	Exposed ground pad
1	VBAT1	-	Supply voltage
2	VR_ANA	-	Regulated supply voltage for analogue circuitry
3	VR_DIG	-	Regulated supply voltage for digital blocks
4	XTA	I/O	XTAL connection or TCXO input
5	XTB	I/O	XTAL connection
6	RESET	I/O	Reset trigger input
7	DIO0	I/O	Digital I/O, software configured
8	DIO1/DCLK	I/O	Digital I/O, software configured
9	DIO2/DATA	I/O	Digital I/O, software configured
10	DIO3	I/O	Digital I/O, software configured
11	DIO4	I/O	Digital I/O, software configured
12	DIO5	I/O	Digital I/O, software configured
13	VBAT2	-	Supply voltage
14	GND	-	Ground
15	SCK	I	SPI Clock input
16	MISO	O	SPI Data output
17	MOSI	I	SPI Data input
18	NSS	I	SPI Chip select input
19	RXTX	O	Rx/Tx switch control: high in Tx
20	RFO	O	RF output
21	RFI	I	RF input
22	GND	O	Ground
23	PA_BOOST	O	Optional high-power PA output
24	VR_PA	O	Regulated supply for the PA

2. Electrical Characteristics

2.1. ESD Notice

The SX1235 is a high performance radio frequency device. It satisfies:

- Class 2 of the JEDEC standard JESD22-A114-B (Human Body Model) on all pins.
- Class B of the JEDEC standard JESD22-A115-A (Machine Model) on all pins.
- Class IV of the JEDEC standard JESD22-C101C (Charged Device Model) on pins VR_ANA, VR_DIG, RFIO, PA_BOOST, VR_PA, Class III on all other pins.

ESD Precautions must be taken to avoid permanent damage.

2.2. Absolute Maximum Ratings

Stresses above the values listed below may cause permanent device failure. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Table 2 Absolute Maximum Ratings

Symbol	Description	Min	Max	Unit
VDDmr	Supply Voltage	-0.5	3.9	V
Tmr	Temperature	-55	+115	° C
Tj	Junction temperature	-	+125	° C
Pmr	RF Input Level	-	+10	dBm

2.3. Operating Range

Table 3 Operating Range

Symbol	Description	Min	Max	Unit
VDDop	Supply voltage	1.8	3.7	V
Top	Operational temperature range	-40	+85	°C
Clop	Load capacitance on digital ports	-	25	pF
ML	RF Input Level	-	+10	dBm

2.4. ETSI Category 1 Specification

Functionality that complies with the ETSI EN300 220 Category 1 is only possible in conjunction with an external SAW filter. To this end the specification of the SAW filter and the corresponding overall system performance is given here.

2.4.1. SAW Filter Specification

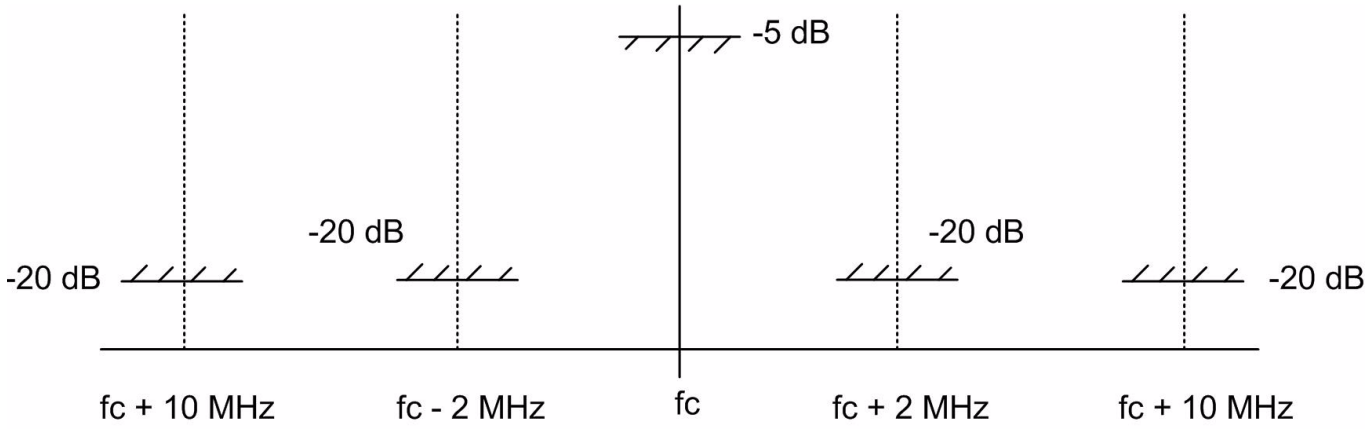

Figure 4. SAW Filter Performance Mask for Guaranteed Category 1 Compliance.

2.4.2. Category 1 Test Conditions

All receiver tests are performed with receiver bandwidth = 3.9 kHz (Single Side Bandwidth) as programmed in RegRxBw, an AFC SSBW of 7.81 kHz (corresponds to a declared 18.7 kHz $DSBW_{-20\ dB}$) receiving a 3 kbps PN15 sequence with 2 kHz frequency deviation for a BER of 1% (bit synchronizer is enabled). The RF centre frequency is 869.21250 MHz.

Blocking tests are performed with an unmodulated interferer. The wanted signal power for the Blocking Immunity and ACR tests is set to -103.3 dBm (3 dB above the calculated sensitivity limit of -106.3 dBm). Saturation testing in both the adjacent channel and higher offsets is performed at -63.3 dBm (43 dB above the sensitivity limit of -106.3 dBm). PLL settings are as described in Section 7.8.1.

The reference circuit of Section 2.4.6 is used with a SAW filter for all measurements that respects the mask requirements of Figure 4. Category 1 performances are specified with a regulated 3.3 V supply and for operation at room temperature only.

2.4.3. System Performance (Absolute Units) with a SAW as Defined in 2.4.1

Table 4 Absolute Performance of the SX1235 Reference Design.

Symbol	Description	Conditions	Min	Typ	Max	Unit
C1_RFS_F	RF Sensitivity FSK		-	-110	-	dBm
C1_ACR	Adjacent Channel Rejection	±25 kHz	-47	-44	-	dBm
C1_ACS	Adjacent Channel Saturation	±25 kHz	-16.3	-13.3	-	dBm
C1_BI	Blocking Immunity	±2 MHz ±10 MHz	-16.3 -14.3	-7.5 -7.5	- -	dBm dBm

Symbol	Description	Conditions	Min	Typ	Max	Unit
C1_BS	Receiver Saturation	±2 MHz ±10 MHz	-14.3 -9.3	-7.5 -7.5	- -	dBm dBm
C1_IMG	Image Rejection	(BW= 3.9 kHz or 7.81 kHz) -500 kHz	-58.3	-	-	dBm

2.4.4. System Performance (Regulatory Margin)

Table 5 SX1235 Reference Design Regulatory Margin to the Category 1 Test Limits.

Symbol	Description	Conditions	Min	Typ	Max	Unit
MC1_RFS_F	Margin to Sensitivity Limit		-	3.7	-	dB
MC1_ACR	Margin to ACR Limit	±25 kHz	3	6	-	dB
MC1_ACS	Margin to ACS Limit	±25 kHz	3	6	-	dB
MC1_BI	Margin to Blocking Limit	±2 MHz ±10 MHz	3 5	12.5 12.5	- -	dB dB
MC1_BS	Margin to Saturation Limit	±2 MHz ±10 MHz	5 10	12.5 12.5	- -	dB dB
MC1_IMG	Margin to Image Rejection Limit	(BS = 3.9 kHz or 7.81 kHz) -500 kHz	10	-	-	dB

2.4.5. Measurement Configuration for Category 1 Testing

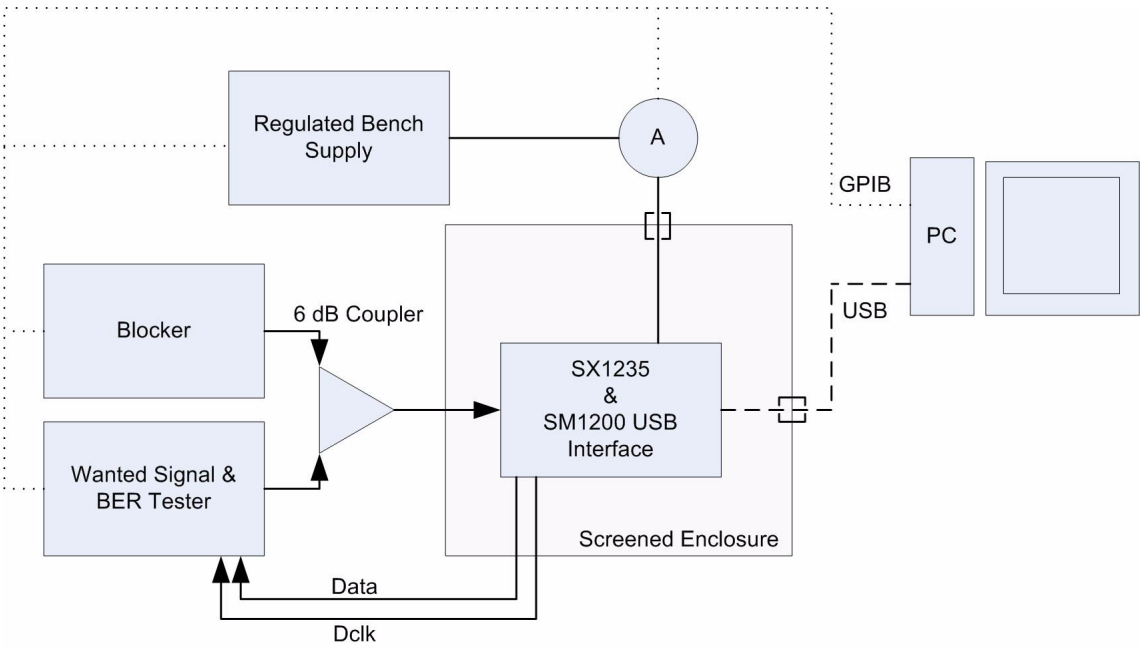

Figure 5. Measurement configuration used for testing of the SX1235 reference design.

2.4.6. 869 MHz Category 1 Reference Design Module SM1235

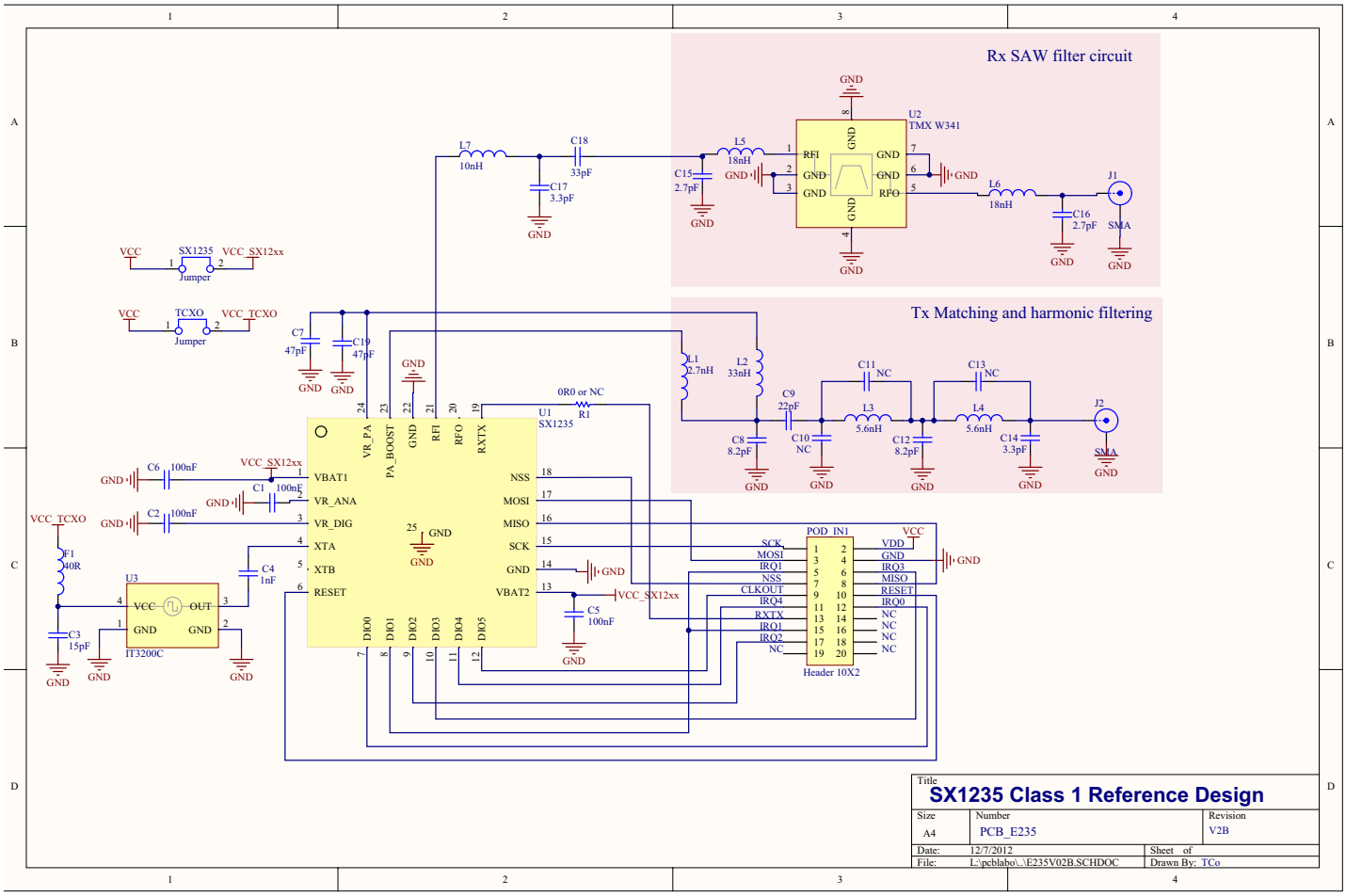

Figure 6. Circuit schematic of the SX1235 reference design used for regulatory testing.

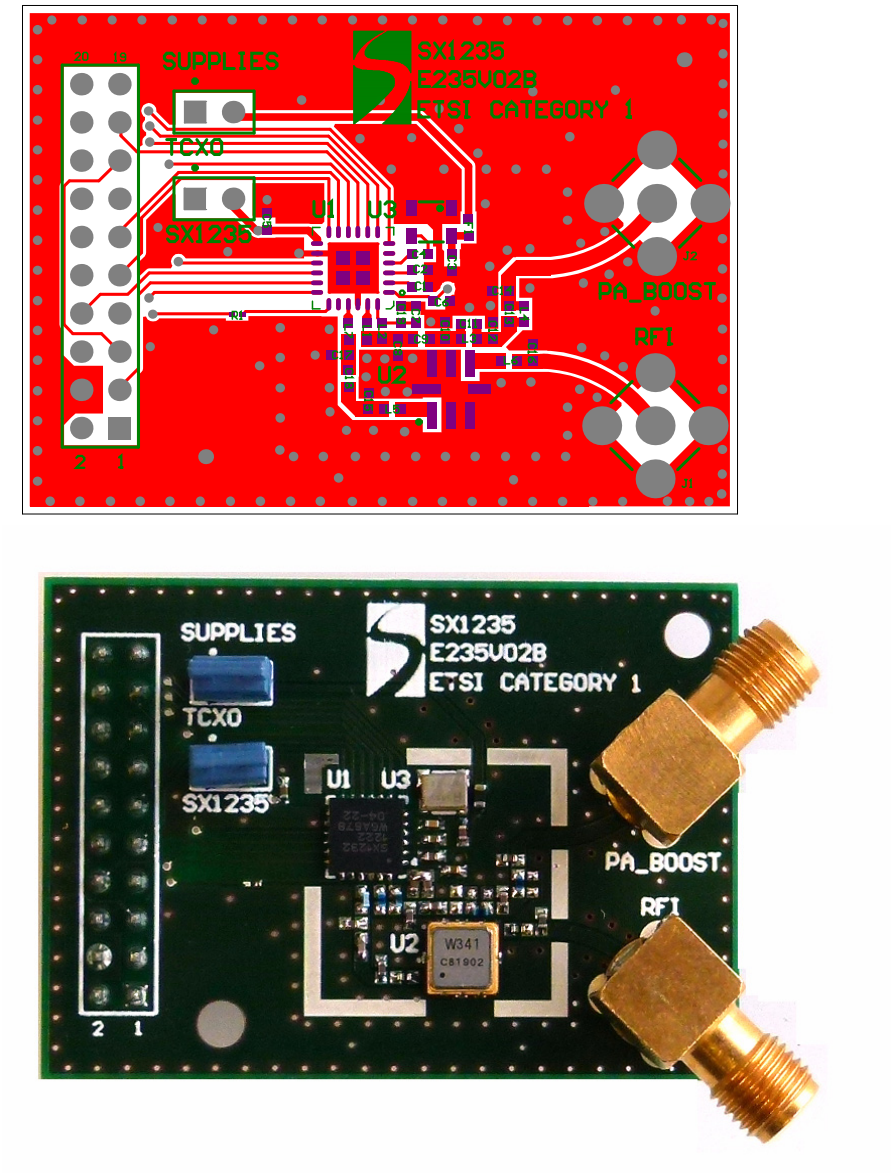

Figure 7. SX1235 Reference Design PCB Layout, Gives both +20 dBm RF Output Tx and Category 1 Rx.

2.5. Circuit Specification

The tables below give the electrical specifications of the transceiver under the following conditions: Supply voltage VBAT1= VBAT2 = VDD = 3.3 V, temperature = 25 °C, F_{XOSC} = 32 MHz, F_{RF} = 868 MHz, Pout = +13 dBm, 2-level FSK modulation without pre-filtering, FDA = 5 kHz, Bit Rate = 4.8 kbps and terminated in a matched 50 ohm impedance, unless otherwise specified.

Note Unless otherwise specified, the performance in the 915 MHz band is identical.

2.5.1. Power Consumption

Table 6 Power Consumption Specification

Symbol	Description	Conditions	Min	Typ	Max	Unit
IDDSL	Supply current in Sleep mode		-	0.1	1	uA
IDDIDLE	Supply current in Idle mode	RC oscillator enabled	-	1.2	-	uA
IDDST	Supply current in Standby mode	Crystal oscillator enabled	-	1.3	1.5	mA
IDDFS	Supply current in Synthesizer mode	FSRx	-	4.5	-	mA
IDDR	Supply current in Receive mode	*LnaBoost* = 00	-	9.3	-	mA
IDDT	Supply current in Transmit mode with impedance matching	RFOP = +20 dBm, on PA_BOOST RFOP = +17 dBm, on PA_BOOST RFOP = +13 dBm, on RFO pin RFOP = + 7 dBm, on RFO pin	- - - -	125 93 28 18	- - - -	mA mA mA mA

2.5.2. Frequency Synthesis

Table 7 Frequency Synthesizer Specification

Symbol	Description	Conditions	Min	Typ	Max	Unit
FR	Synthesizer frequency range	Programmable	862	-	1020	MHz
FXOSC	Crystal oscillator frequency	See section 7.1	-	32	-	MHz
TS_OSC	Crystal oscillator wake-up time	With crystal specified in section 7.1	-	250	-	us
TS_FS	Frequency synthesizer wake-up time to Pll Lock signal	From Standby mode	-	60	-	us
TS_HOP	Frequency synthesizer hop time at most 10 kHz away from the target frequency	200 kHz step 1 MHz step 5 MHz step 7 MHz step 12 MHz step 20 MHz step 25 MHz step	- - - - - - -	20 20 50 50 50 50 50	- - - - - - -	us us us us us us us
FSTEP	Frequency synthesizer step	FSTEP = FXOSC/2^{19}	-	61.0	-	Hz
FRC	RC Oscillator frequency	After calibration	-	62.5	-	kHz

BRF	Bit rate, FSK	Programmable values (1)	1.2	-	300	kbps
BRO	Bit rate, OOK	Programmable	1.2	-	32.768	kbps
BRA	Bit Rate Accuracy	ABS (wanted BR - available BR)	-	-	250	ppm
FDA	Frequency deviation, FSK (1)	Programmable FDA + BRF/2 =< 250 kHz	0.6	-	200	kHz

Note For Maximum Bit rate the maximum modulation index is 1.

2.5.3. Receiver

All receiver tests are performed with RxBw = 10 kHz (Single Side Bandwidth) as programmed in *RegRxBw*, receiving a PN15 sequence. Sensitivities are reported for a 0.1% BER (with Bit Synchronizer enabled), unless otherwise specified. Blocking tests are performed with an unmodulated interferer. The wanted signal power for the Blocking Immunity, ACR, IIP2, IIP3 and AMR tests is set 3 dB above the receiver sensitivity level.

Table 8 Receiver Specification

Symbol	Description	Conditions	Min	Typ	Max	Unit
RFS_F	Direct tie of RFI and RFO pins, as shown in Figure 43. FSK sensitivity, highest LNA gain.	FDA = 5 kHz, BR = 1.2 kb/s FDA = 5 kHz, BR = 4.8 kb/s FDA = 40 kHz, BR = 38.4 kb/s* FDA = 20 kHz, BR = 38.4 kb/s** FDA = 62.5 kHz, BR = 250 kb/s***	- - - - -	-119 -115 -105 -106 -92	- - - - -	dBm dBm dBm dBm dBm
	Split RF paths, as shown in Figure 44, LnaBoost is turned on, the RF switch insertion loss is not accounted for.	FDA = 5 kHz, BR = 1.2 kb/s FDA = 5 kHz, BR = 4.8 kb/s FDA = 40 kHz, BR = 38.4 kb/s* FDA = 20 kHz, BR = 38.4 kb/s** FDA = 62.5 kHz, BR = 250 kb/s***	- - - - -	-123 -119 -110 -110 -97	- - - - -	dBm dBm dBm dBm dBm
RFS_O	OOK sensitivity, highest LNA gain Conditions of Figure 43	BR = 4.8 kb/s BR = 32 kb/s	- -	-117 -108	- -	dBm dBm
CCR	Co-Channel Rejection		-	-8	-	dB
ACR	Adjacent Channel Rejection	FDA = 2 kHz, BR = 1.2kb/s, RxBw = 5.2kHz Offset = +/- 25 kHz	-	54	-	dB
		FDA = 5 kHz, BR=4.8kb/s Offset = +/- 25 kHz Offset = +/- 50 kHz	- -	50 50	- -	dB dB
BI	Blocking Immunity	Offset = +/- 1 MHz Offset = +/- 2 MHz Offset = +/- 10 MHz	- - -	73 78 87	- - -	dB dB dB
AMR	AM Rejection, AM modulated interferer with 100% modulation depth, fm = 1 kHz, square	Offset = +/- 1 MHz Offset = +/- 2 MHz Offset = +/- 10 MHz	- - -	73 78 87	- - -	dB dB dB

IIP2	2nd order Input Intercept Point Unwanted tones are 20 MHz above the LO	Highest LNA gain	-	+57	-	dBm
IIP3	3rd order Input Intercept point Unwanted tones are 1MHz and 1.995 MHz above the LO	Highest LNA gain G1 LNA gain G2, 4 dB sensitivity hit	- -	-12 -8	- -	dBm dBm
BW_SSB	Single Side channel filter BW	Programmable	2.7	-	250	kHz
IMR	Image Rejection	Wanted signal 3dB over sens BER=0.1%	-	48	-	dB
IMA	Image Attenuation		-	56	-	dB
DR_RSSI	RSSI Dynamic Range	AGC enabled Min Max	- -	-127 0	- -	dBm dBm

* *RxBw = 83 kHz (Single Side Bandwidth)*

** *RxBw = 50 kHz (Single Side Bandwidth)*

*** *RxBw = 250 kHz (Single Side Bandwidth)*

2.5.4. Transmitter

Table 9 Transmitter Specification

Symbol	Description	Conditions	Min	Typ	Max	Unit
RF_OP	RF output power in 50 ohms on RFO pin (High efficiency PA).	Programmable with steps Max Min	 +11 -	 +14 -1	 - -	 dBm dBm
ΔRF_OP_V	RF output power stability on RFO pin versus voltage supply.	VDD = 2.5 V to 3.3 V VDD = 1.8 V to 3.7 V	- -	3 8	- -	dB dB
RF_OPH	RF output power in 50 ohms, on PA_BOOST pin (Regulated PA).	Programmable with 1 dB steps Max Min	- -	+17 +2	- -	dBm dBm
RF_OPH_MAX	Max RF output power, on PA_BOOST pin	High power mode	-	+20	-	dBm
ΔRF_OPH_V	RF output power stability on PA_BOOST pin versus voltage supply.	VDD = 2.4 V to 3.7 V	-	±1	-	dB
ΔRF_T	RF output power stability versus temperature on both RF pins.	From T = -40 °C to +85 °C	-	+/-1	-	dB
PHN	Transmitter Phase Noise	Low Consumption PLL, 915 MHz 50 kHz Offset 400 kHz Offset 1 MHz Offset	 - - -	 -102 -114 -120	 - - -	 dBc/Hz
		Low Phase Noise PLL, 915 MHz 50 kHz Offset 400 kHz Offset 1 MHz Offset	 - - -	 -106 -117 -122	 - - -	 dBc/Hz

ACP	Transmitter adjacent channel power (measured at 25 kHz off-set)	BT=1. Measurement conditions as defined by EN 300 220-1 V2.4.1	-	-	-37	dBm
TS_TR	Transmitter wake up time, to the first rising edge of DCLK	Frequency Synthesizer enabled, *PaRamp* = 10us, BR = 4.8 kb/s	-	120	-	us

2.5.5. Digital Specification

Conditions: Temp = 25°C, VDD = 3.3V, FXOSC = 32 MHz, unless otherwise specified.

Table 10 Digital Specification

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{IH}	Digital input level high		0.8	-	-	VDD
V_{IL}	Digital input level low		-	-	0.2	VDD
V_{OH}	Digital output level high	Imax = 1 mA	0.9	-	-	VDD
V_{OL}	Digital output level low	Imax = -1 mA	-	-	0.1	VDD
F_{SCK}	SCK frequency		-	-	10	MHz
t_{ch}	SCK high time		50	-	-	ns
t_{cl}	SCK low time		50	-	-	ns
t_{rise}	SCK rise time		-	5	-	ns
t_{fall}	SCK fall time		-	5	-	ns
t_{setup}	MOSI setup time	from MOSI change to SCK rising edge	30	-	-	ns
t_{hold}	MOSI hold time	from SCK rising edge to MOSI change	20	-	-	ns
t_{nsetup}	NSS setup time	from NSS falling edge to SCK rising edge	30	-	-	ns
t_{nhold}	NSS hold time	from SCK falling edge to NSS rising edge, normal mode	100	-	-	ns
t_{nhigh}	NSS high time between SPI accesses		20	-	-	ns
T_DATA	DATA hold and setup time		250	-	-	ns

3. Chip Description

This section describes in depth the architecture of the SX1235 low-power, highly integrated ETSI category 1 compatible transceiver. The following figure shows a simplified block diagram of the SX1235.

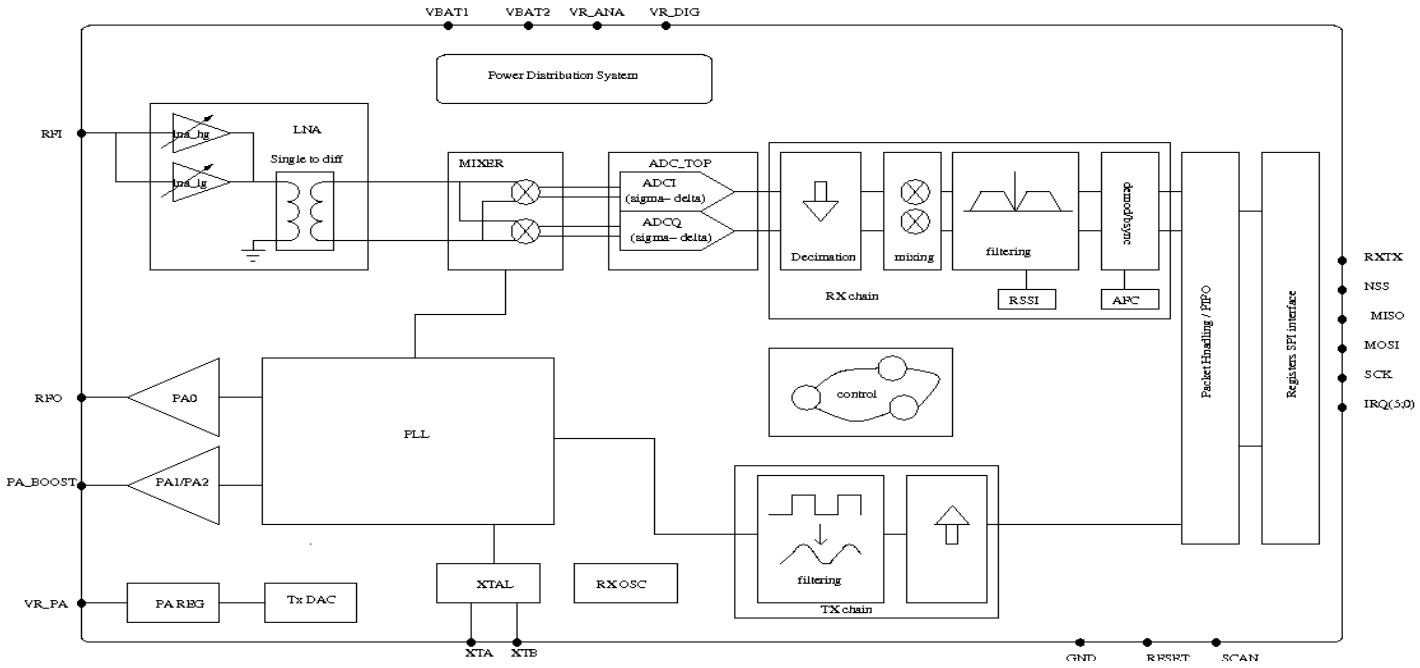

Figure 8. Simplified SX1235 Block Schematic Diagram

SX1235 is a half-duplex, low-IF transceiver. Here the received RF signal is first amplified by the LNA. The LNA input is single ended to minimise the external BoM and for ease of design. Following the LNA output the conversion to differential is made to improve the second order linearity and harmonic rejection. The signal is then down-converted to in-phase (I) and quadrature (Q) components at the intermediate frequency (IF) by the mixer stage. A pair of sigma delta ADCs then perform data conversion, with all subsequent signal processing and demodulation performed in the digital domain. The digital state machine also controls the automatic frequency correction (AFC), received signal strength indicator (RSSI) and automatic gain control (AGC). It also features the higher-level packet and protocol level functionality of the top level sequencer.

In the receiver operating mode two states of functionality are defined. Upon initial transition to receiver operating mode the receiver is in the ‘receiver-enabled’ state. In this state the receiver awaits for either the user defined valid preamble or RSSI detection criterion to be fulfilled. Once met the receiver enters ‘receiver-active’ state. In this second state the received signal is processed by the packet engine and top level sequencer.

The frequency synthesiser generates the local oscillator (LO) frequency for both receiver and transmitter. The PLL is optimized for user-transparent, low lock time, fast auto-calibrating operation. In transmission, frequency modulation is performed digitally within the PLL bandwidth. SX1235 Also features optional pre-filtering of the bit stream to improve spectral purity.

SX1235 features a pair of RF power amplifiers. The first, connected to RFO, can deliver up to +14 dBm, is unregulated for high power efficiency and can be connected directly to the RF receiver input via a pair of passive components to form a single antenna port high efficiency transceiver. The second PA, connected to the PA_BOOST pin and can deliver up to +20 dBm via a dedicated matching network.

SX1235 also includes two timing references: an RC oscillator and a 32 MHz crystal oscillator.

All major parameters of the RF front end and digital state machine are fully configurable via an SPI interface which gives access to internal registers. This includes a mode auto sequencer that oversees the transition and calibration of the SX1235 between intermediate modes of operation in the fastest time possible.

3.1. Power Supply Strategy

The SX1235 employs an advanced power supply scheme, which provides stable operating characteristics over the full temperature and voltage range of operation. This includes the full output power of +17dBm which is maintained from 1.8 to 3.7 V.

The SX1235 can be powered from any low-noise voltage source via pins VBAT1 and VBAT2. Decoupling capacitors should be connected, as suggested in the reference design, on VR_PA, VR_DIG and VR_ANA pins to ensure a correct operation of the built-in voltage regulators.

3.2. Low Battery Detector

A low battery detector is also included allowing the generation of an interrupt signal in response to passing a programmable threshold adjustable through the register *RegLowBat*. The interrupt signal can be mapped to any of the DIO pins, by programming *RegDioMapping*.

3.3. Frequency Synthesis

3.3.1. Reference Oscillator

The crystal oscillator is the main timing reference of the SX1235. It is used as a reference for the frequency synthesizer and as a clock for the digital processing.

The XO startup time, TS_OSC, depends on the actual XTAL being connected on pins XTA and XTB. The SX1232 optimizes the startup time and automatically triggers the PLL when the XO signal is stable.

An external clock can be used to replace the crystal oscillator, for instance a tight tolerance TCXO. To do so, *TcxoInputOn* in *RegTcxo* should be set to 1, and the external clock has to be provided on XTA (pin 4). XTB (pin 5) should be left open.

The peak-peak amplitude of the input signal must never exceed 1.8 V. Please consult your TCXO supplier for an appropriate value of decoupling capacitor, C_D.

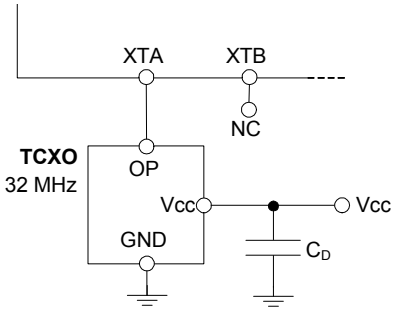

Figure 9. TCXO Connection

3.3.2. CLKOUT Output

The reference frequency, or a fraction of it, can be provided on DIO5 (pin 12) by modifying bits *ClkOut* in *RegDioMapping2*. Two typical applications of the CLKOUT output include:

- To provide a clock output for a companion processor, thus saving the cost of an additional oscillator. CLKOUT can be made available in any operation mode except Sleep mode and is automatically enabled at power on reset.
- To provide an oscillator reference output. Measurement of the CLKOUT signal enables simple software trimming of the initial crystal tolerance.

Note to minimize the current consumption of the SX1235, please ensure that the CLKOUT signal is disabled when not required.

3.3.3. PLL Architecture

The local oscillator of the SX1235 is derived from a fractional-N PLL that is referenced to the crystal oscillator circuit. Two PLLs are available for transmit mode operation - either low phase noise or low current consumption to maximize either transmit power consumption or transmit spectral purity. Both PLLs feature a programmable bandwidth setting where one of four discrete preset bandwidths may be accessed. For reference the relative performance of both low consumption and low phase noise PLL, for each programmable bandwidth setting, is shown in the following figure.

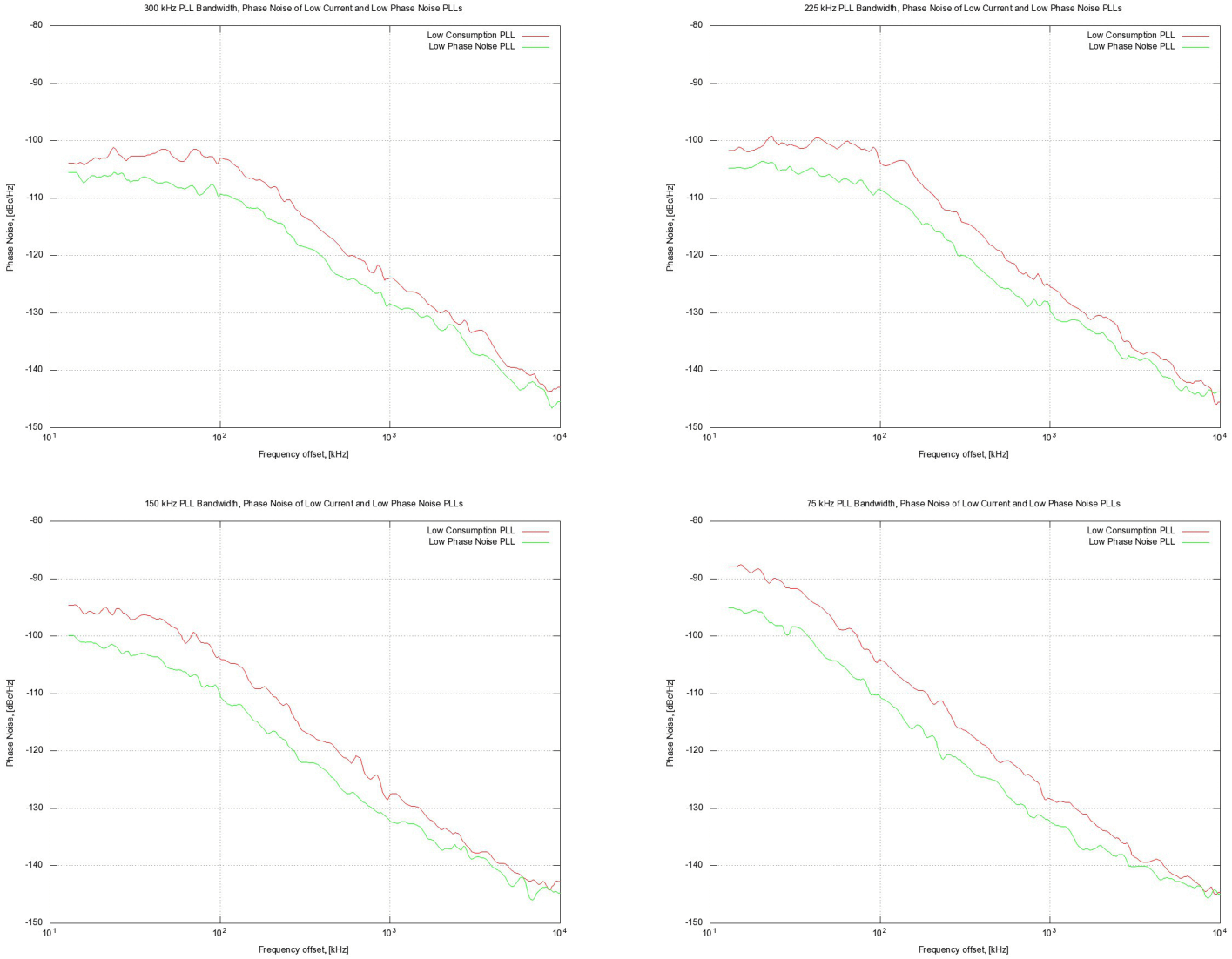

Figure 10. Typical Phase Noise Performances of the Low Consumption and Low Phase Noise PLLs.

Note in receive mode, only the low consumption PLL is available.

The SX1235 PLL embeds a 19-bit sigma-delta modulator and its frequency resolution, constant over the whole frequency range, and is given by:

$$F_{STEP} = \frac{F_{XOSC}}{2^{19}}$$