Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

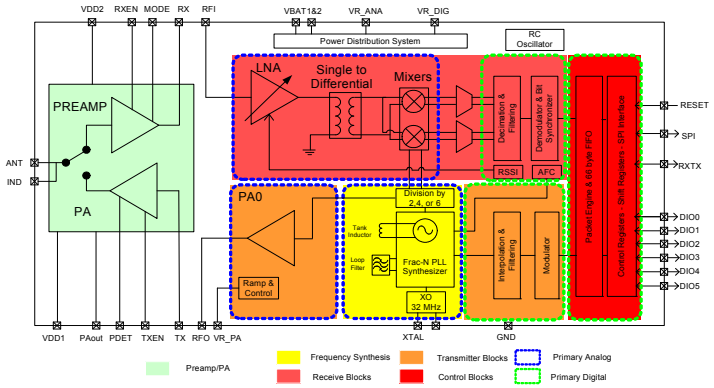
With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

SX1238 - Fully Integrated Transceiver with +27dBm TX Power



GENERAL DESCRIPTION

The SX1238 is a fully integrated ISM band transceiver optimized for use in the (FCC Part 15) 915 MHz band in the US and 868 MHz band in Europe with a minimum of external components. It offers a combination of high link budget and low current consumption in all operating modes. The 150 dB link budget is achieved by a low noise CMOS receiver front end and up to +27 dBm of transmit output power. This is made possible by a fully integrated front end consisting of a TR Switch, LNA and efficient PA. This makes SX1238 ideal for applications requiring extended range, high link budget, or operation in the presence of high interference.

The Low-IF architecture of the SX1238 sees fast transceiver start times and demodulation predicated towards low modulation index and Gaussian filtered spectrally efficient modulation formats.

APPLICATIONS

- Automated Meter Reading
- Wireless Sensor Networks
- Home and Building Automation
- Wireless Alarm and Security Systems
- Industrial Monitoring and Control

KEY PRODUCT FEATURES

- +27 dBm - 500 mW RF output power
- +27 dBm high efficiency PA
- Programmable bit rate up to 300kbps
- High sensitivity: -124 dBm at 1.2 kbps
- 863 - 870 MHz and 902 - 928 MHz
- 80 dB blocking Immunity
- Low current, 100nA register retention
- Fully integrated synthesizer with a resolution of 61 Hz
- FSK, GFSK, MSK, GMSK and OOK modulations
- Built-in bit synchronizer performing clock recovery
- Sync word recognition
- Preamble detection
- 115 dB+ dynamic range RSSI
- Automatic RF sense with ultra-fast AFC
- Packet engine up to 64 bytes with CRC
- Built-in temperature sensor and low battery indicator

ORDERING INFORMATION

Part Number	Delivery	MOQ / Multiple
SX1238IMLTRT	Tape & Reel	3000 pieces

- MLPQ 40 Package - Operating Range [-40;+85°C]
- Pb-free, Halogen free, RoHS/WEEE compliant product

Table of contents

Section **Page**

Table of contents

Section **Page**

Table of contents

Section **Page**

Acronyms

BOM	Bill Of Materials
BR	Bit Rate
BW	Bandwidth
CCITT	Comité Consultatif International Téléphonique et Télégraphique - ITU
CRC	Cyclic Redundancy Check
DAC	Digital to Analog Converter
ETSI	European Telecommunications Standards Institute
FCC	Federal Communications Commission
Fdev	Frequency Deviation
FIFO	First In First Out
FIR	Finite Impulse Response
FS	Frequency Synthesizer
FSK	Frequency Shift Keying
GUI	Graphical User Interface
IC	Integrated Circuit
ID	IDentificator
IF	Intermediate Frequency
IRQ	Interrupt ReQuest
ITU	International Telecommunication Union
LFSR	Linear Feedback Shift Register
LNA	Low Noise Amplifier
LO	Local Oscillator
LSB	Least Significant Bit
MSB	Most Significant Bit
NRZ	Non Return to Zero
OOK	On Off Keying
PA	Power Amplifier
PCB	Printed Circuit Board
PLL	Phase-Locked Loop
POR	Power On Reset
RBW	Resolution BandWidth
RF	Radio Frequency
RSSI	Received Signal Strength Indicator
Rx	Receiver
SAW	Surface Acoustic Wave
SPI	Serial Peripheral Interface
SR	Shift Register
Stby	Standby
Tx	Transmitter
uC	Microcontroller
VCO	Voltage Controlled Oscillator
XO	Crystal Oscillator
XOR	eXclusive OR

This product datasheet contains a detailed description of the SX1238 performance and functionality. Please consult the Semtech website for the latest updates or errata.

1. General Description

The SX1238 is a multi-chip integrated circuit ideally suited for today's high performance ISM band RF applications. The SX1238's advanced feature set includes a state-of-the-art packet engine and top level sequencer. In conjunction with a 64 byte FIFO, these automate the entire process of packet transmission, reception and acknowledgment without incurring the consumption penalty common to many transceivers that feature an on-chip MCU. Being easily configurable, it greatly simplifies system design and reduces external MCU workload to an absolute minimum. The high level of integration reduces the external BoM to passive decoupling and impedance matching components. It is intended for use as a high-performance, low-cost FSK and OOK RF transceiver for robust, frequency agile, half-duplex, bi-directional RF links.

The SX1238 is intended for applications requiring high sensitivity and low receive current. Coupling the digital state machine with an RF front end capable of delivering a link budget of 150dB (-124dBm sensitivity in conjunction with +27dBm Pout). The SX1238 complies with FCC and ETSI regulatory requirements and is available in a 5 x 7 mm MLPQ 40 lead package. The low-IF architecture of the SX1238 is well suited for low modulation index and narrow band operation.

1.1. Simplified Block Diagram

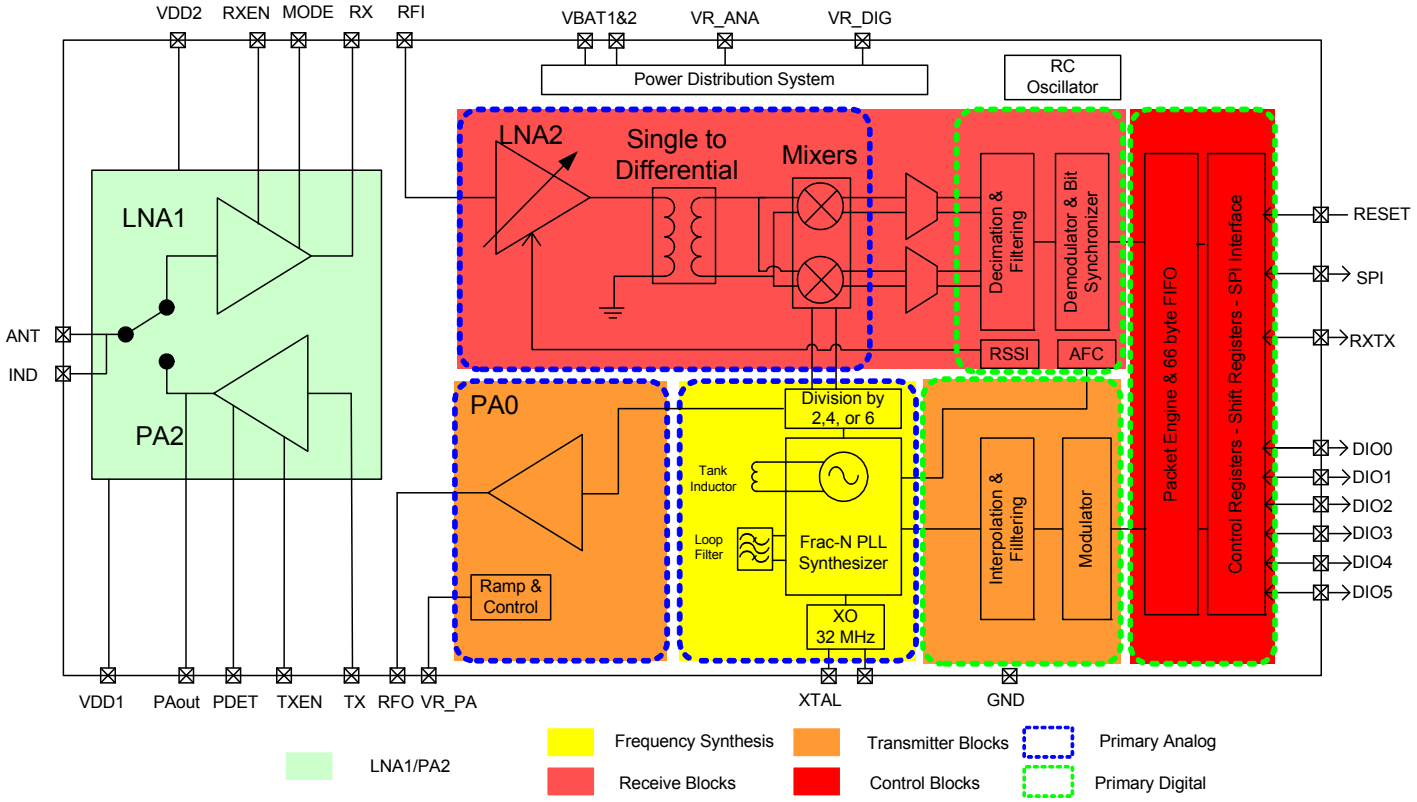


Figure 1. SX1238 Block Diagram

1.2. Pin and Marking Diagram

The following diagram shows the pin arrangement of the MLPQ package, top view.

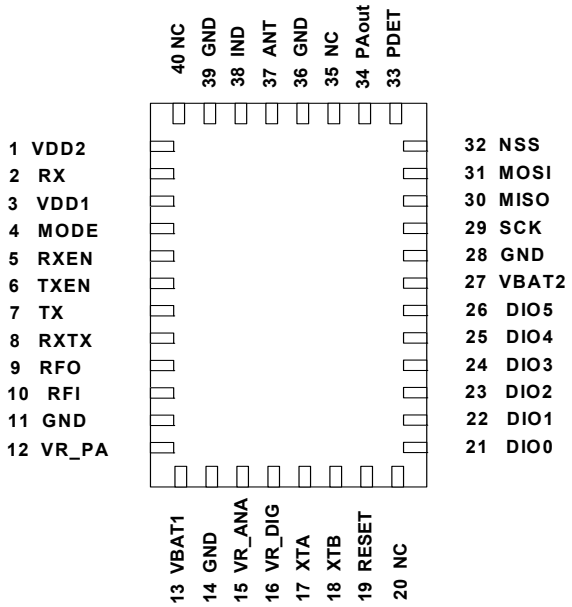


Figure 2. SX1238 Pin Diagram

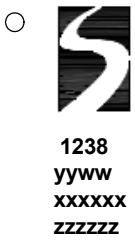


Figure 3. Marking Diagram

Notes: All package marking to be aligned about the vertical center line

Marking is for the 5 x 7 mm MLPQ 40 Lead package

nnnn	*Indicates Part Number (Example 1238)*
yyww	*indicates the date code (Example 0252)*
xxxxxx	*Semtech Lot No. for TL356 (Example 090101)*
zzzzzz	*Semtech Lot No. (Example 01-100)*

1.3. Pin Description

Table 1 SX1238 Pinouts

Number	Name	Type	Description
0	GROUND	-	Exposed ground pad
1	VDD2	-	LNA Voltage Supply
2	RX	O	LNA output (DC short to GND, use DC block)
3	VDD1	-	Driver stage Voltage Supply
4	MODE	I	Selects High or Low LNA Gain
5	RXEN	I	Enables Receive Mode
6	TXEN	I	Enables Transmit Mode
7	TX	I	PA Input (DC short to GND, use DC block)
8	RXTX	O	Rx/Tx switch control: high in Tx
9	RFO	O	RF output (connects to TX)
10	RFI	I	RF input (connects to RX LNA output)
11	GND	-	Ground
12	VR_PA	-	Regulated supply for the PA
13	VBAT1	-	Supply voltage
14	GND	-	Ground
15	VR_ANA	-	Regulated supply voltage for analogue circuitry
16	VR_DIG	-	Regulated supply voltage for digital blocks
17	XTA	I/O	XTAL connection or TCXO input
18	XTB	I/O	XTAL connection
19	RESET	I/O	Reset trigger input
20	NC	-	No Connection
21	DIO0	I/O	Digital I/O, software configured
22	DIO1/DCLK	I/O	Digital I/O, software configured
23	DIO2/DATA	I/O	Digital I/O, software configured
24	DIO3	I/O	Digital I/O, software configured
25	DIO4	I/O	Digital I/O, software configured
26	DIO5	I/O	Digital I/O, software configured
27	VBAT2	-	Supply voltage
28	GND	-	Ground
29	SCK	I	SPI Clock input
30	MISO	O	SPI Data output

Number	Name	Type	Description
31	MOSI	I	SPI Data input
32	NSS	I	SPI Chip select input
33	PDET	O	Analog voltage proportional to PA output power
34	PAout	-	Power Stage Output (connect inductor to Supply)
35	NC	-	No Connection
36	GND	-	Ground
37	ANT	I/O	Antenna Port (DC short to GND, use DC block)
38	IND	-	Antenna matching (connect inductor to GND)
39	GND	-	Ground
40	NC	-	No Connection

2. Electrical Characteristics

2.1. ESD Notice

The SX1238 is a high performance radio frequency device. It satisfies:

- Class 2 of the JEDEC standard JESD22-A114-B (Human Body Model) on all pins.
- Class III of the JEDEC standard JESD22-C101C (Charged Device Model) on all pins

This part embeds a high performance RF Power Amplifier and as such might be permanently damaged by un-proper handling. Industry-standard precautions should be taken to avoid ESD-related failures.

2.2. Absolute Maximum Ratings

Sustained operation at or above the Absolute Maximum Ratings for any one or combination of the below parameters may result in permanent damage to the device and is not recommended. All maximum RF Input Power Ratings assume 50 Ohm Terminal Impedance.

Table 2 Absolute Maximum Ratings

Symbol	Description	Min	Max	Unit
VDDmr	Supply Voltage	-0.5	3.9	V
Tmr	Ambient Temperature*	-50	+95	° C
Tj	Junction temperature	-	+125	° C
Tst	Storage Ambient Temperature**	-50	+125	° C
Pant	ANT RF Input Level	-	+5	dBm
Ptx	TX, RF Input Level	-	+7	dBm
VCmr	RXEN, TXEN, MODE DC control voltage	-	3.9	V

**For part mounted on 4 layer board per JEDEC specification.*

***No RF and DC Voltages Applied. Appropriate care required according to JEDEC Standards*

2.3. Operating Range

Table 3 Operating Range.[1]

Symbol	Description	Min	Max	Unit
VDDop	Supply voltage	2.7	3.6	V
Top	Operating Ambient Temperature*	-40	+85	°C
Clop	Load capacitance on digital ports (related only to outputs)	-	25	pF

1. *For part mounted on 4 layer board per JEDEC specification.*

2.4. Chip Specification

The tables below give the electrical specifications of the transceiver under the following conditions: Supply voltage VBAT1= VBAT2=VDDx=3.3 V, temperature = 25 °C, *FXOSC* = 32 MHz, F_{RF} = 915 MHz, Pout = as indicated, 2-level FSK modulation without pre-filtering, FDA = 5 kHz, Bit Rate = 4.8 kb/s and terminated in a matched 50 Ohm impedance, unless otherwise specified. This specification is at room temperature.

2.4.1. Power Consumption

Table 4 Power Consumption Specification

Symbol	Description	Conditions	Min	Typ	Max	Unit
IDDSL	Supply current in Sleep mode	RXEN, TXEN = 0	-	1.1	2	uA
IDDIDLE	Supply current in Idle mode	RC oscillator enabled, RXEN, TXEN = 0	-	2	-	uA
IDDST	Supply current in Standby mode	Crystal oscillator enabled, RXEN, TXEN = 0	-	1.3	1.5	mA
IDDFS	Supply current in Synthesizer mode	FSRx Modes; RXEN, TXEN = 0	-	4.5	-	mA
IDDR	Supply current in Receive mode	RXEN = 1, TXEN = 0, MODE = 0 (low gain) RXEN = 1, TXEN = 0, MODE = 1 (high gain)	- -	19.3 25.3	-	mA mA
IDDT	Supply current in Transmit mode Measured at Antenna Port	TXEN = 1 ANT = +27 dBm, (Saturation) ANT = +26 dBm ANT = +17 dBm	- - - -	- 408 389 158	- - - -	- mA mA mA

2.4.2. Frequency Synthesis

Table 5 Frequency Synthesizer Specification

Symbol	Description	Conditions	Min	Typ	Max	Unit
FR	Synthesizer frequency range	Programmable	863	-	928	MHz
FXOSC	Crystal oscillator frequency	See section [7.1]	-	32	-	MHz
TS_OSC	Crystal oscillator wake-up time		-	250	500	us
TS_FS	Frequency synthesizer wake-up time to PllLock signal	From Standby mode	-	60	-	us
TS_HOP	Frequency synthesizer hop time at most 10 kHz away from the target frequency	200 kHz step 1 MHz step 5 MHz step 7 MHz step 12 MHz step 20 MHz step 25 MHz step	- - - - - - -	20 20 50 50 50 50 50	- - - - - - -	us us us us us us us
FSTEP	Frequency synthesizer step	FSTEP = FXOSC/2^{19}	-	61.0	-	Hz
FRC	RC Oscillator frequency	After calibration	-	62.5	-	kHz

BRF	Bit rate, FSK	Programmable (1)	1.2	-	300	kbps
BRO	Bit rate, OOK	Programmable	1.2	-	32.768	kbps
BRA	Bit Rate Accuracy	ABS (wanted BR - available BR)	-	-	250	ppm
FDA	Frequency deviation, FSK (1)	Programmable FDA + BRF/2 =< 250 kHz	0.6	-	200	kHz

Note: For Maximum Bit rate the maximum modulation index is 1.

2.4.3. Receiver

All receiver tests are performed with RxBw = 10 kHz (Single Side Bandwidth) as programmed in *RegRxBw*, receiving a PN15 sequence. Sensitivities are reported for a 0.1% BER (with Bit Synchronizer enabled), unless otherwise specified. Blocking tests are performed with an unmodulated interferer. The wanted signal power for the Blocking Immunity, ACR, IIP2, IIP3 and AMR tests is set 3 dB above the receiver sensitivity level.

Table 6 Receiver Specification

Symbol	Description	Conditions	Min	Typ	Max	Unit
RFS_F	FSK sensitivity, highest LNA gain	FDA = 5 kHz, BR = 1.2 kb/s FDA = 5 kHz, BR = 4.8 kb/s FDA = 40 kHz, BR = 38.4 kb/s* FDA = 20 kHz, BR = 38.4 kb/s** FDA = 62.5 kHz, BR = 250 kb/s***	- - - - -	-124 -119 -109 -110 -96	- - - - -	dBm dBm dBm dBm dBm
RFS_O	OOK sensitivity, highest LNA gain****	BR = 4.8 kb/s BR = 32 kb/s	- -	-121 -112	- -	dBm dBm
CCR	Co-Channel Rejection		-	-8	-	dB
ACR	Adjacent Channel Rejection	Offset = +/- 25 kHz Offset = +/- 50 kHz	- -	50 50	- -	dB dB
BI	Blocking Immunity	Offset = +/- 1 MHz Offset = +/- 2 MHz Offset = +/- 10 MHz	- - -	73 78 87	- - -	dB dB dB
AMR	AM Rejection , AM modulated interferer with 100% modulation depth, fm = 1 kHz, square	Offset = +/- 1 MHz Offset = +/- 2 MHz Offset = +/- 10 MHz	- - -	73 78 87	- - -	dB dB dB
IIP2	2nd order Input Intercept Point Unwanted tones are 20 MHz above the LO	Highest LNA gain****	-	+44	-	dBm
IIP3	3rd order Input Intercept point Unwanted tones are 1MHz and 1.995 MHz above the LO	Highest LNA gain****	-	-25	-	dBm
BW_SSB	Single Side channel filter BW	Programmable	2.7	-	250	kHz
IMR	Image rejection		35	48	-	dB

TS_RE	Receiver wake-up time, from PLL locked state to *RxReady*	RXBw = 10 kHz, BR = 4.8 kb/s RXBw = 250 kHz, BR = 100 kb/s	- -	9 9	- -	T_{bit} T_{bit}
TS_RE_AGC	Receiver wake-up time, from PLL locked state, AGC enabled	RxBw = 10 kHz, BR = 4.8 kb/s RxBw = 250 kHz, BR = 100 kb/s	- -	14 19	- -	T_{bit} T_{bit}
TS_RE_AGC &AFC	Receiver wake-up time, from PLL lock state, AGC and AFC enabled	RxBw = 10 kHz, BR = 4.8 kb/s RxBw = 250 kHz, BR = 100 kb/s	- -	23 29	- -	T_{bit} T_{bit}
TS_FEI	FEI sampling time	Receiver is ready	-	4	-	T_{bit}
TS_AFC	AFC Response Time	Receiver is ready	-	4	-	T_{bit}
TS_RSSI	RSSI Response Time	Receiver is ready (*fs = 4*RxBw)*	2	-	256	1/*fs*
DR_RSSI	RSSI Dynamic Range	AGC enabled Min MODE = 1 Max	- -	-140 -13	- -	dBm dBm

* *RxBw = 80 kHz (Single Side Bandwidth)*

** *RxBw = 50 kHz (Single Side Bandwidth)*

*** *RxBw = 250 kHz (Single Side Bandwidth)*

**** *Highest LNA gain: MODE = 1, RX Gain Setting G1 (001)*

2.4.4. Transmitter

Table 7 Transmitter Specification

Symbol	Description	Conditions	Min	Typ	Max	Unit
RF_OP*	RF output power in 50 ohms on ANT pin (High Power PA).	Maximum power output achieved when PAO set to 10 dBm or greater	+26	+27	-	dBm
ΔRF_ OP_V	RF output power stability on ANT pin versus voltage supply (into 50 Ohm load)	VDD = 2.7 V to 3.6 V	- -	3	-	dB
ΔRF_T	RF output power stability versus temperature on both RF pins. (into 50 Ohm load)	From T = -40 °C to +85 °C	-	+/-1	-	dB
VSWRstb	VSWR for stability	VSWR mismatch applied to ant port			6:1	
VSWRdm	VSWR for damage	VSWR mismatch applied to ant port			10:1	

PHN	Transmitter Phase Noise	Low Consumption PLL 50kHz Offset 400kHz Offset 1MHz Offset	 - - -	 -102 -114 -120	 - - -	 dBc/ Hz
		Low Phase Noise PLL 50kHz Offset 400kHz Offset 1MHz Offset	 - - -	 -106 -117 -122	 - - -	 dBc/ Hz
TS_TR	Transmitter wake up time, to the first rising edge of DCLK	Frequency Synthesizer enabled, *PaRamp* = 10us, BR = 4.8 kb/s	-	120	-	us

* *Maximum input power at TX port (pin 7)must not exceed +7dBm. This can be accomplished by incorporating an attenuator in the interstage network. See reference design, Figure 39.*

2.4.5. Front End Control

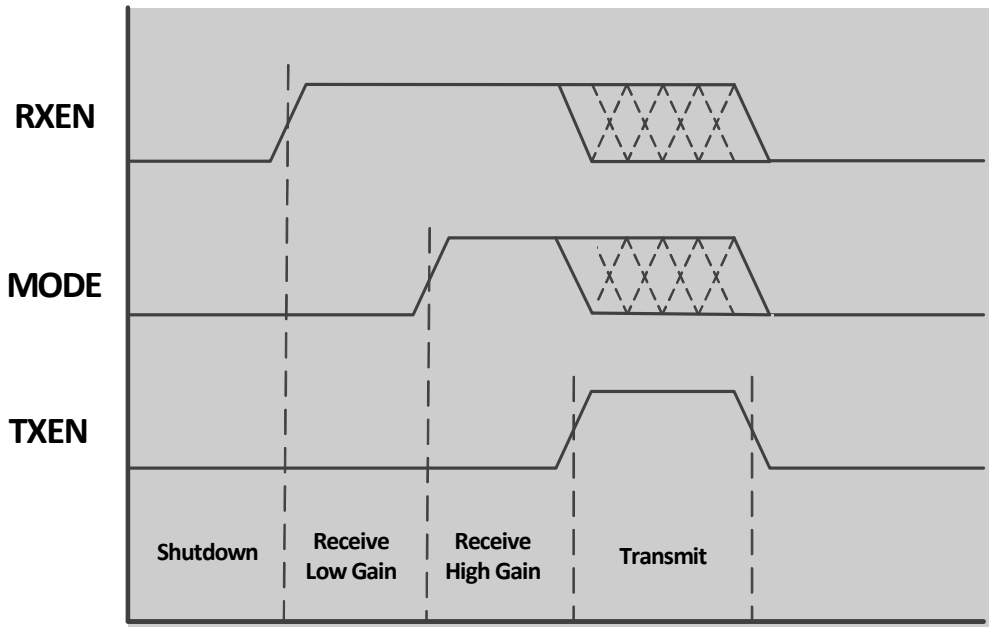


*Figure 4. Front End Control Signal Timing Diagram**

**For safe operation, please allow at least 1us between any mode change.*

Table 8 Front End Control Signal Table

TXEN	RXEN	MODE	Operating Conditions
0	0	X	Shut Down
0	1	0	RX Active, Low Gain Mode
0	1	1	RX Active, High
1	X	X	TX Active

2.4.6. Digital Specification

Conditions: Temp = 25°C, VDD = 3.3V, FXOSC = 32 MHz, unless otherwise specified.

Note: VDD must be applied before any voltage applied to Digital Input

Table 9 Digital Specification

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{IH}	Digital input level high		0.8	-	-	VDD
V_{IL}	Digital input level low		-	-	0.3	V
V_{OH}	Digital output level high	Imax = 1 mA	0.9	-	-	VDD
V_{OL}	Digital output level low	Imax = -1 mA	-	-	0.1	VDD
F_{SCK}	SCK frequency		-	-	10	MHz
t_{ch}	SCK high time		50	-	-	ns
t_{cl}	SCK low time		50	-	-	ns
t_{rise}	SCK rise time		-	5	-	ns
t_{fall}	SCK fall time		-	5	-	ns
t_{setup}	MOSI setup time	from MOSI change to SCK rising edge	30	-	-	ns
t_{hold}	MOSI hold time	from SCK rising edge to MOSI change	20	-	-	ns
t_{nsetup}	NSS setup time	from NSS falling edge to SCK rising edge	30	-	-	ns
t_{nhold}	NSS hold time	from SCK falling edge to NSS rising edge, normal mode	100	-	-	ns
t_{nhigh}	NSS high time between SPI accesses		20	-	-	ns
T_DATA	DATA hold and setup time		250	-	-	ns

3. Chip Description

This section describes in depth the architecture of the SX1238 low-power, highly integrated transceiver. The following figure shows a simplified block diagram of the SX1238.

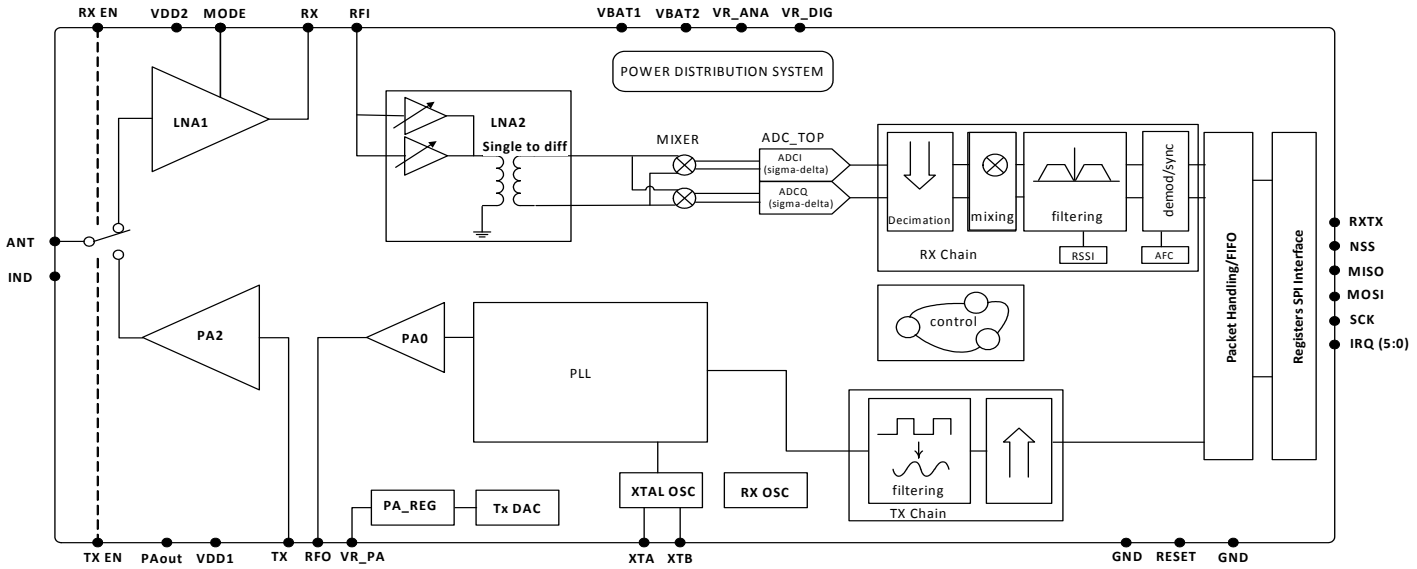


Figure 5. Simplified SX1238 Block Schematic Diagram

SX1238 is a half-duplex, low-IF transceiver. Here the received RF signal at the ANT port is amplified by LNA1 when RXEN is enabled. The MODE selects high or low LNA1 gain. LNA1 output passes through an external filter/matching network, then enters LNA2. Both LNA1 and LNA2 inputs are single ended to minimize the external BoM and for ease of design. Following LNA2 output, the conversion to differential is made internally to improve the second order linearity and harmonic rejection. The signal is then down-converted to in-phase (I) and quadrature (Q) components at the intermediate frequency (IF) by the mixer stage. A pair of sigma delta ADCs then perform data conversion, with all subsequent signal processing and demodulation performed in the digital domain. The digital state machine also controls the automatic frequency correction (AFC), received signal strength indicator (RSSI) and automatic gain control (AGC). It also features the higher-level packet and protocol level functionality of the top level sequencer.

In the receiver operating mode two states of functionality are defined. Upon initial transition to receiver operating mode the receiver is in the ‘receiver-enabled’ state. In this state the receiver awaits for either the user defined valid preamble or RSSI detection criterion to be fulfilled. Once met the receiver enters ‘receiver-active’ state. In this second state the received signal is processed by the packet engine and top level sequencer.

The frequency synthesizer generates the local oscillator (LO) frequency for both receiver and transmitter. The PLL is optimized for user-transparent low lock time and fast auto-calibrating operation. In transmission, frequency modulation is performed digitally within the PLL bandwidth. It also features optional pre-filtering of the bit stream to improve spectral purity.

The SX1238 features a pair of RF power amplifiers. The first, PA0, connected to RFO, passes through a filter/bias network then enters PA2 input connected to TX. PA2 output is connected to the T/R switch and can deliver up to +27 dBm to the ANT port directly into a 50 Ohm load when the TXEN is enabled. The PDET provides an analog DC voltage proportional to PA2 output power.

The SX1238 also includes two timing references: an internal RC oscillator and a 32 MHz crystal oscillator.

All major parameters of the RF front end and digital state machine are fully configurable via an SPI interface which gives access to internal registers. This includes a mode auto sequencer that oversees the transition and calibration of the SX1238 between intermediate modes of operation in the fastest time possible.

3.1. Power Supply Strategy

The SX1238 employs an advanced power supply scheme, which provides stable operating characteristics over the full temperature and voltage range of operation. The SX1238 can be powered from any low-noise voltage source via pins VBAT, VBAT2, VDD1, and VDD2. It is mandatory that PAout be connected to the voltage source through an inductor. Decoupling capacitors should be connected, as suggested in the reference design, including VR_PA, VR_DIG and VR_ANA pins to ensure a correct operation of the built-in voltage regulators. A 2.2uF (min) capacitor should be used to bypass the main supply.

3.2. Low Battery Detector

A low battery detector is also included allowing the generation of an interrupt signal in response to passing a programmable threshold adjustable through the register *RegLowBat*. The interrupt signal can be mapped to any of the DIO pins, by programming *RegDioMapping*.

3.3. Frequency Synthesis

3.3.1. Reference Oscillator

The crystal oscillator is the main timing reference of the SX1238. It is used as a reference for the frequency synthesizer and as a clock for the digital processing.

The XO startup time, TS_OSC, depends on the actual XTAL being connected on pins XTA and XTB. The SX1238 optimizes the startup time and automatically triggers the PLL when the XO signal is stable.

An external clock can be used to replace the crystal oscillator, for instance a tight tolerance TCXO. To do so, *TcxoInputOn* in *RegTcxo* should be set to 1, and the external clock has to be provided on XTA (pin 4). XTB (pin 5) should be left open.

The peak-peak amplitude of the input signal must never exceed 1.8 V. Please consult your TCXO supplier for an appropriate value of decoupling capacitor, C_D.

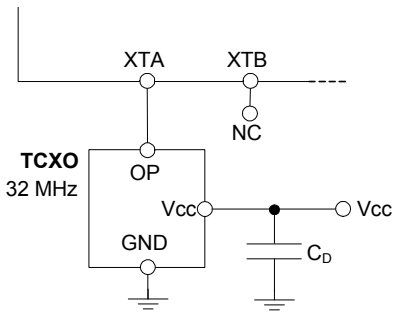


Figure 6. TCXO Connection

3.3.2. CLKOUT Output

The reference frequency, or a fraction of it, can be provided on DIO5 (pin 12) by modifying bits *ClkOut* in *RegDioMapping2*. Two typical applications of the CLKOUT output include:

- To provide a clock output for a companion processor, thus saving the cost of an additional oscillator. CLKOUT can be made available in any operation mode except Sleep mode and is automatically enabled at power on reset.
- To provide an oscillator reference output. Measurement of the CLKOUT signal enables simple software trimming of the initial crystal tolerance.

Note: To minimize the current consumption of the SX1238, please ensure that the CLKOUT signal is disabled when not required.

3.3.3. PLL Architecture

The local oscillator of the SX1238 is derived from a fractional-N PLL that is referenced to the crystal oscillator circuit. Two PLLs are available for transmit mode operation - either low phase noise or low current consumption to maximize either transmit power consumption or transmit spectral purity. Both PLLs feature a programmable bandwidth setting where one of four discrete preset bandwidths may be accessed. For reference the relative performance of both low consumption and low phase noise PLL, for each programmable bandwidth setting, is shown in the following figure.

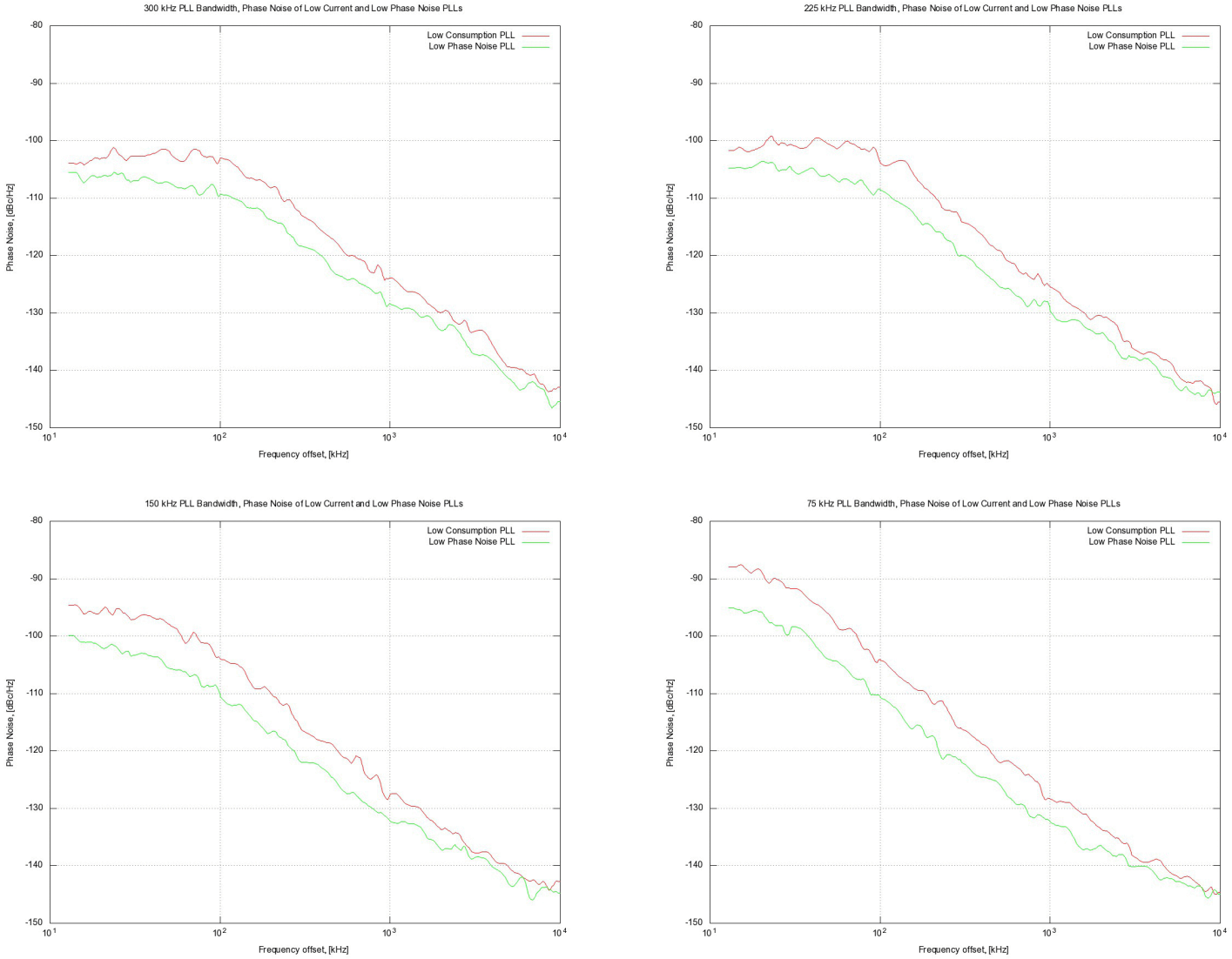


Figure 7. Typical Phase Noise Performances of the Low Consumption and Low Phase Noise PLLs.

Note: In receive mode, only the low consumption PLL is available.

The SX1238 PLL embeds a 19-bit sigma-delta modulator and its frequency resolution, constant over the whole frequency range, and is given by:

$$F_{STEP} = \frac{F_{XOSC}}{2^{19}}$$

The carrier frequency is programmed through *RegFrf*, split across addresses 0x06 to 0x08:

$$F_{RF} = F_{STEP} \times Frf(23,0)$$

Note: The Frf setting is split across 3 bytes. A change in the center frequency will only be taken into account when the least significant byte FrfLsb in RegFrfLsb is written. This allows for more complex modulation schemes such as m-ary FSK, where frequency modulation is achieved by changing the programmed RF frequency.

3.3.4. RC Oscillator

All timings in the low-power state of the Top Level Sequencer rely on the accuracy of the internal low-power RC oscillator. This oscillator is automatically calibrated at the device power-up, and it is a user-transparent process.

For applications enduring large temperature variations, and for which the power supply is never removed, RC calibration can be performed upon user request. *RcCalStart* in *RegOsc* triggers this calibration, and the flag *RcCalDone* will be set automatically when the calibration is over.

3.4. Transmitter Description

The transmitter of SX1238 comprises the frequency synthesizer, modulator and power amplifier blocks, together with the DC biasing and ramping functionality that is provided through the VR_PA block.

3.4.1. Architecture Description

The architecture of the RF front end is shown in the following diagram. Here we see that the PA0 output on the RFO pin features a single low power amplifier device. It connects to a high power amplifier that permits continuous operation up to +27 dBm.

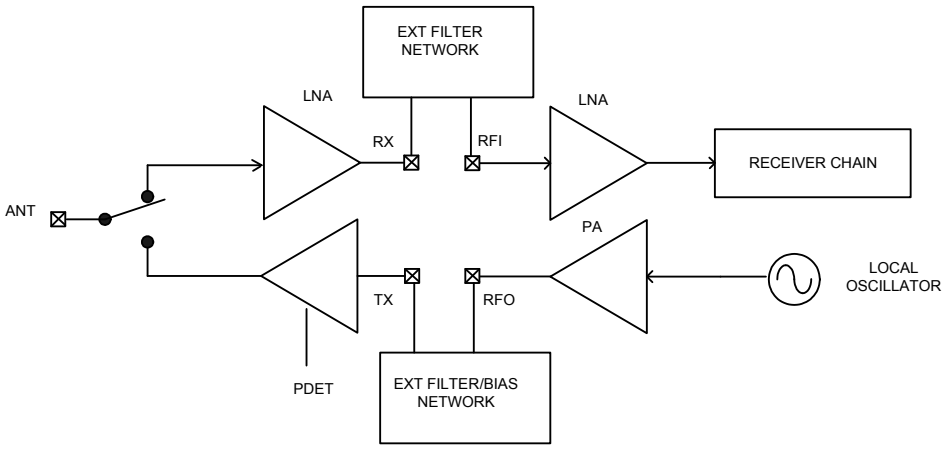


Figure 8. RF Front-end Architecture Shows the Internal PA Configuration.

3.4.2. Bit Rate Setting

The bitrate setting is referenced to the crystal oscillator and provides a precise means of setting the bit (or equivalently chip) rate of the radio. In continuous transmit mode (Section 3.2.2) the data stream to be transmitted can be input directly to the modulator via pin 9 (DIO2/DATA) in an asynchronous manner, unless Gaussian filtering is used, in which case the DCLK signal on pin 10 (DIO1/DCLK) is used to synchronize the data stream. See section [3.4.5] for details on the Gaussian filter.

In Packet mode or in Continuous mode with Gaussian filtering enabled, the Bit Rate (BR) is controlled by bits *Bitrate* in *RegBitrateMsb and RegBitrateLsb*.

$$BitRate = \frac{FXOSC}{BitRate(15,0) + \frac{BitrateFrac}{16}}$$

*Note: BitrateFrac bits have **no effect** (i.e may be considered equal to 0) **in OOK** modulation mode.*

The quantity *BitrateFrac* is hence designed to allow very high precision (max. 250 ppm calculation error) for any bitrate in the programmable range. Table 10 below shows a range of standard bitrates and the accuracy to within which they may be reached.

Table 10 Bit Rate Examples

Type	BitRate (15:8)	BitRate (7:0)	(G)FSK (G)MSK	OOK	Actual Bit Rate
Classical modem baud rates (multiples of 1.2 kbps)	0x68	0x2B	1.2 kbps	1.2 kbps	1200.015
	0x34	0x15	2.4 kbps	2.4 kbps	2400.060
	0x1A	0x0B	4.8 kbps	4.8 kbps	4799.760
	0x0D	0x05	9.6 kbps	9.6 kbps	9600.960
	0x06	0x83	19.2 kbps	19.2 kbps	19196.16
	0x03	0x41	38.4 kbps		38415.36
	0x01	0xA1	76.8 kbps		76738.60
	0x00	0xD0	153.6 kbps		153846.1
Classical modem baud rates (multiples of 0.9 kbps)	0x02	0x2C	57.6 kbps		57553.95
	0x01	0x16	115.2 kbps		115107.9
Round bit rates (multiples of 12.5, 25 and 50 kbps)	0x0A	0x00	12.5 kbps	12.5 kbps	12500.00
	0x05	0x00	25 kbps	25 kbps	25000.00
	0x80	0x00	50 kbps		50000.00
	0x01	0x40	100 kbps		100000.0
	0x00	0xD5	150 kbps		150234.7
	0x00	0xA0	200 kbps		200000.0
	0x00	0x80	250 kbps		250000.0
	0x00	0x6B	300 kbps		299065.4
Watch Xtal frequency	0x03	0xD1	32.768 kbps	32.768 kbps	32753.32

3.4.3. FSK Modulation

FSK modulation is performed inside the PLL bandwidth, by changing the fractional divider ratio in the feedback loop of the PLL. The large resolution of the sigma-delta modulator, allows for very narrow frequency deviation. The frequency deviation F_{DEV} is given by:

$$F_{DEV} = F_{STEP} \times Fdev(13,0)$$

To ensure a proper modulation, the following limit applies:

$$F_{DEV} + \frac{BR}{2} \leq (250)kHz$$

Note No constraint applies to the modulation index of the transmitter, but the frequency deviation must be set between 600 Hz and 200 kHz.

3.4.4. OOK Modulation

OOK modulation is applied by switching on and off the Power Amplifier. Digital control and smoothing are available to improve the transient power response of the OOK transmitter.

3.4.5. Modulation Shaping

Modulation shaping can be applied in both OOK and FSK modulation modes, to improve the narrowband response of the transmitter. Both shaping features are controlled with *PaRamp* bits in *RegPaRamp*.

- In FSK mode, a Gaussian filter with BT = 0.5 or 1 is used to filter the modulation stream, at the input of the sigma-delta modulator. If the Gaussian filter is enabled when the SX1238 is in Continuous mode, DCLK signal on pin 10 (DIO1/ DCLK) will trigger an interrupt on the uC each time a new bit has to be transmitted. Please refer to section [5.4.2] for details.
- When OOK modulation is used, the PA0 bias voltages are ramped up and down smoothly when the PA is turned on and off, to reduce spectral splatter.

Note *The transmitter must be restarted if the ModulationShaping setting is changed, in order to recalibrate the built-in filter.*

3.4.6. RF Power Amplifiers

Two power amplifier blocks are embedded in the SX1238. The first one, herein referred to as PA0, is output through the RFO port (pin 9). The PA0 RF power is programmable between -1dBm and +13dBm. The RFO port is connected to the high power PA2 input port, TX (pin 7), through an impedance matching network with an embedded resistive attenuator. The nominal power setting for the PA0 port to achieve maximum power out of PA0 is +10 dBm. This provides an input power of +3 dBm to the TX port. It is important to use the recommended 7dB attenuator in the matching network between the RFO and TX ports to prevent damage to the TX input from excessive power. An application circuit showing a recommended interstage network with this embedded attenuator is shown in Fig 39 Reference Design.

The high power PA2 output is connected through the T/R switch to the ANT pin and is active when TXEN is high. It can deliver up to +27 dBm in programmable steps to the antenna, directly into a 50 Ohm load. Harmonic filtering is required to ensure regulatory compliance. The RF power is programmable between a nominal +17 dBm and +27 dBm.

Table 11 Power Amplifier Mode Selection Truth Table

PaSelect	Mode	Power Range
0*	PA0 output on pin RFO to drive PA2	+17 to +27 dBm
1	Not defined	-

** TXEN must be high to enable PA2*

3.5. Receiver Description

3.5.1. Overview

The SX1238 features a digital receiver with the analog to digital conversion process being performed directly following the LNA-Mixers block. The Low-IF receiver is able to handle ASK, OOK, (G)FSK and (G)MSK modulation. All the filtering, demodulation, gain control, synchronization and packet handling is performed digitally, which allows a very wide range of bit rates and frequency deviations to be selected. The receiver is also capable of automatic gain calibration to improve precision on RSSI measurement and enhanced image rejection.

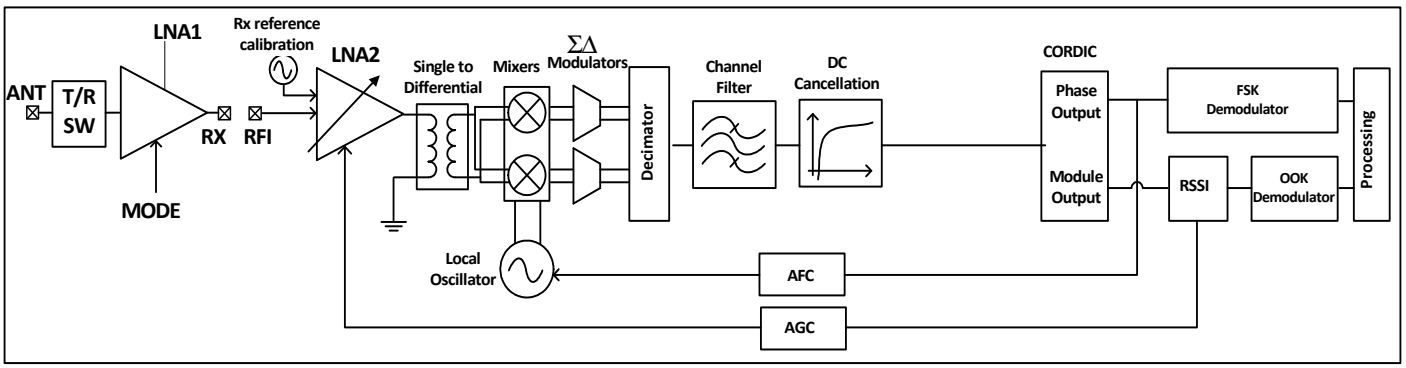


Figure 9. Receiver Block Diagram

3.5.2. LNA1, LNA2

The LNA1 precedes LNA2 and provides selection of two fixed gain settings. When MODE = 0, the low gain setting is 10 dB and when MODE = 1, the high gain setting is 13 dB. The LNA1 output is connected to the LNA2 input through an external matching network. LNA2 provides variable gain for AGC control.

3.5.3. Automatic Gain Control - AGC

The AGC feature allows receiver to handle a wide Rx input dynamic range from the sensitivity level up to maximum input level of 0dBm or more, whilst optimizing the system linearity.

The automatic LNA gain control is effective by setting the bit *AgcAutoOn* to '1'. The automatic adjustment of the LNA2 gain can be performed on the Rx input level (Pin) at receiver start up and/or during the Preamble reception. The automatic adjustment of the LNA2 during the Preamble is effective by setting the bit *AgcOnPreamble* to '1' otherwise it will be performed only at the receiver start up.

The LNA2 gain can also be manually selected using *LnaGain* bits and by disabling the automatic LNA2 gain control by setting the *AgcAutoOn* bit to '0'.

Table 12, below, shows typical NF and IIP3 performance for the different LNA1 and LNA2 gains.

Table 12 LNA1, LNA2 Gain Control and Receiver Performance

RF input level (Pin)	Gain Setting	LNA1 Gain	LnaGain	Relative LNA1,2 Gain [dB]	NF [dB]	IIP3 [dBm]
Pin <= AgcThresh1	G1	High	001	0	3.3	-25
Pin <= AgcThresh1	G1	Low	001	-3	4	-22
AgcThresh1 < Pin <= AgcThresh2	G2	High	010	-3.9	3.9	-23
AgcThresh1 < Pin <= AgcThresh2	G2	Low	010	-9	5	-20
AgcThresh2 < Pin <= AgcThresh3	G3	High	011	-12	5.5	-18
AgcThresh2 < Pin <= AgcThresh3	G3	Low	011	-15	7.2	-15
AgcThresh3 < Pin <= AgcThresh4	G4	High	100	-24	12.5	-18
AgcThresh3 < Pin <= AgcThresh4	G4	Low	100	-27	15.3	-15
AgcThresh4 < Pin <= AgcThresh5	G5	High	110	-26	20.1	-3
AgcThresh4 < Pin <= AgcThresh5	G5	Low	110	-29	23	0
AgcThresh5 < Pin	G6	High	111	-48	30	-3
AgcThresh5 < Pin	G6	Low	111	-51	33	0

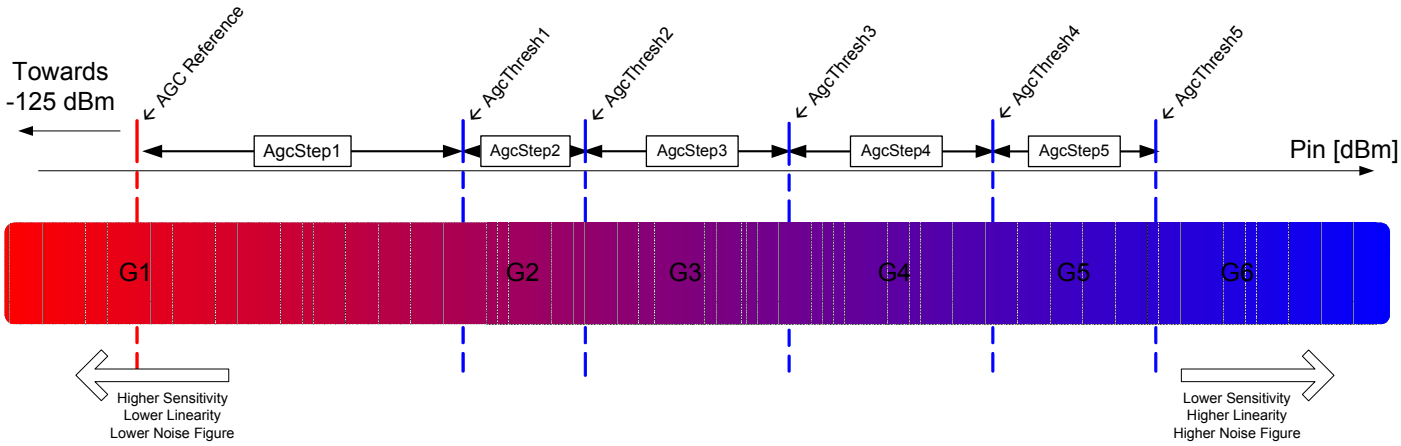


Figure 10. AGC Steps Definition

The global AGC reference, reference all AGC thresholds, is determined as follows:

AGC Reference[dBm]=-174dBm+10*log(2**RxBw*)+SNR+*AgcReferenceLevel*

with SNR = 8dB, fixed value.

A detailed description of the receiver setup to enable the AGC is provided in section [3.3].