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SX1261/2

Long Range, Low Power, sub-GHz RF Transceiver

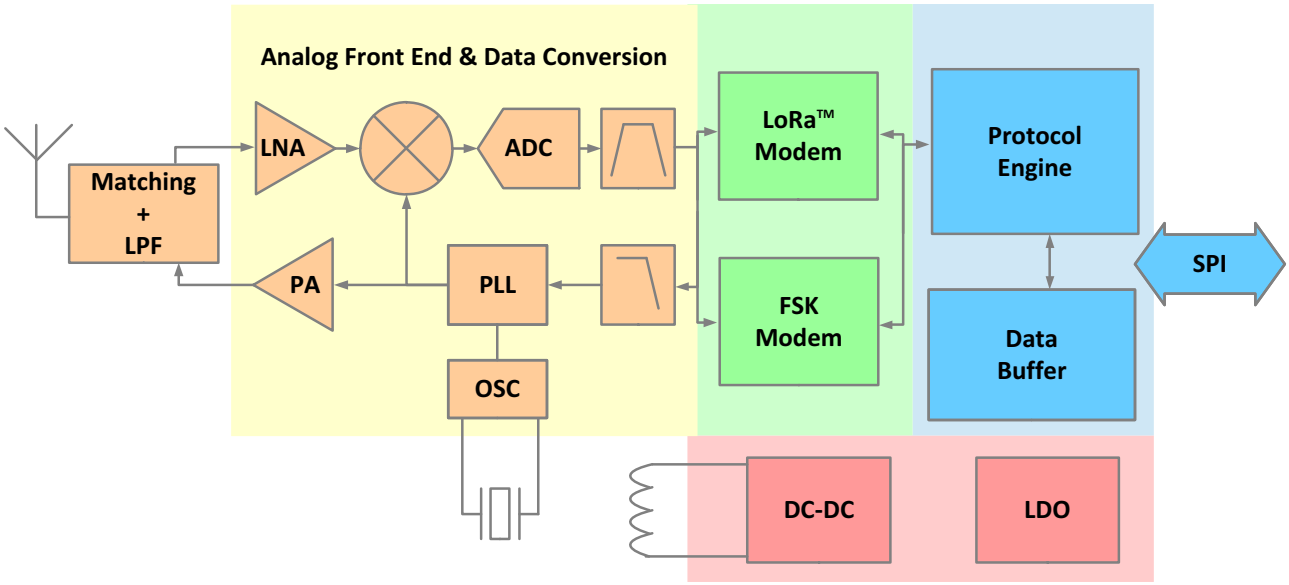

Figure A: SX1261/2 Block Diagram

General Description

SX1261 and SX1262 sub-GHz radio transceivers are ideal for long range wireless applications. Both devices are designed for long battery life with just 4.2 mA of active receive current consumption. The SX1261 can transmit up to +15 dBm and the SX1262 can transmit up to +22 dBm with highly efficient integrated power amplifiers.

These devices support LoRa® modulation for LPWAN use cases and (G)FSK modulation for legacy use cases. The devices are highly configurable to meet different application requirements utilizing the global LoRaWAN™ standard or proprietary protocols.

The devices are designed to comply with the physical layer requirements of the LoRaWAN™ specification released by the LoRa Alliance™.

The radio is suitable for systems targeting compliance with radio regulations including but not limited to ETSI EN 300 220, FCC CFR 47 Part 15, China regulatory requirements and the Japanese ARIB T-108. Continuous frequency coverage from 150 MHz to 960 MHz allows the support of all major sub-GHz ISM bands around the world.

Applications

The level of integration and the low consumption within SX1261/2 enable a new generation of Internet of Things applications.

- Smart meters
- Supply chain and logistics
- Building automation
- Agricultural sensors
- Smart cities
- Retail store sensors
- Asset tracking
- Street lights
- Parking sensors
- Environmental sensors
- Healthcare
- Safety and security sensors
- Remote control applications

Ordering Information

Part Number	Delivery	Minimum Order Quantity
SX1261IMLTRT	Tape & Reel	3'000 pieces
SX1262IMLTRT	Tape & Reel	3'000 pieces

QFN 24 Package, Pb-free, Halogen free, RoHS/WEEE compliant product.

Revision History

Version	ECO	Date	Modifications
1.0	039166	October 2017	First Release
1.1	040046	December 2017	Addition of a note "when using a TCXO" to explain the XTA cap value change with TCXO in chapter 4.1.3 XTAL Control Block New sub-chapter 5.1.5 "Considerations on the DC-DC Inductor Selection" Addition of a note recommending 12 symbols of LoRa preamble for optimal performances in chapter 6.1.1.1 Spreading Factor Addition of a note on SetLoRaSymbNumTimeout in chapter 9.6 Receive Mode Correction of RandomNumber Gen[] values in chapter 12.1 Register Map

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1. Architecture

The SX1261 and SX1262 (designated hereafter as "SX1261/2") are half-duplex transceivers capable of low power operation in the 150-960 MHz ISM frequency band. The radio comprises four main blocks:

1. **Analog Front End**: the transmit and receive chains, as well as the data converter interface to ensuing digital blocks. The last stage of the transmit chain is different between the SX1261 and SX1262 chip versions. The SX1261 transceiver is capable of outputting +14/15 dBm maximum output power under DC-DC converter or LDO supply. The SX1262 transceiver is capable of delivering up to +22 dBm under the battery supply.
2. **Digital Modem Bank**: a range of modulation options is available in the SX1261/2:
   - LoRa® Rx/Tx, BW = 7.8 - 500 kHz, SF5 to SF12, BR = 0.018 - 62.5 kb/s
   - (G)FSK Rx/Tx, with BR = 0.6 - 300 kb/s
3. **Digital Interface and Control**: this comprises all payload data and protocol processing as well as access to configuration of the radio via the SPI interface.
4. **Power Distribution**: two forms of voltage regulation, DC-DC or linear regulator LDO, are available depending upon the design priorities of the application.

2. Pin Connection

2.1 I/O Description

Table 2-1: SX1261/2 Pinout in QFN 4x4 24L

Pin Number	Pin Name	Type (I = input O = Ouptut)	Description
0	GND	-	Exposed Ground pad
1	VDD_IN	I	Input voltage for power amplifier regulator, VR_PA SX1261: connected to pin 7 SX1262: connected to pin 10
2	GND	-	Ground
3	XTA	-	Crystal oscillator connection, can be used to input external reference clock
4	XTB	-	Crystal oscillator connection
5	GND	-	Ground
6	DIO3	I/O	Multipurpose digital I/O - external TCXO supply voltage
7	VREG	O	Regulated output voltage from the internal regulator LDO / DC-DC
8	GND	-	Ground
9	DCC_SW	O	DC-DC Switcher Output
10	VBAT	I	Supply for the RFIC
11	VBAT_IO	I	Supply for the Digital I/O interface pins (except DIO3)
12	DIO2	I/O	Multipurpose digital I/O / RF Switch control
13	DIO1	I/O	Multipurpose digital IO
14	BUSY	I/O	Busy indicator
15	NRESET	I/O	Reset signal, active low
16	MISO	O	SPI slave output
17	MOSI	I	SPI slave input
18	SCK	I	SPI clock
19	NSS	I	SPI Slave Select
20	GND	-	Ground
21	RFI_P	I	RF receiver input
22	RFI_N	I	RF receiver input
23	RFO	O	RF transmitter output (SX1261 low power PA or SX1262 high power PA)
24	VR_PA	-	Regulated power amplifier supply

2.2 Package View

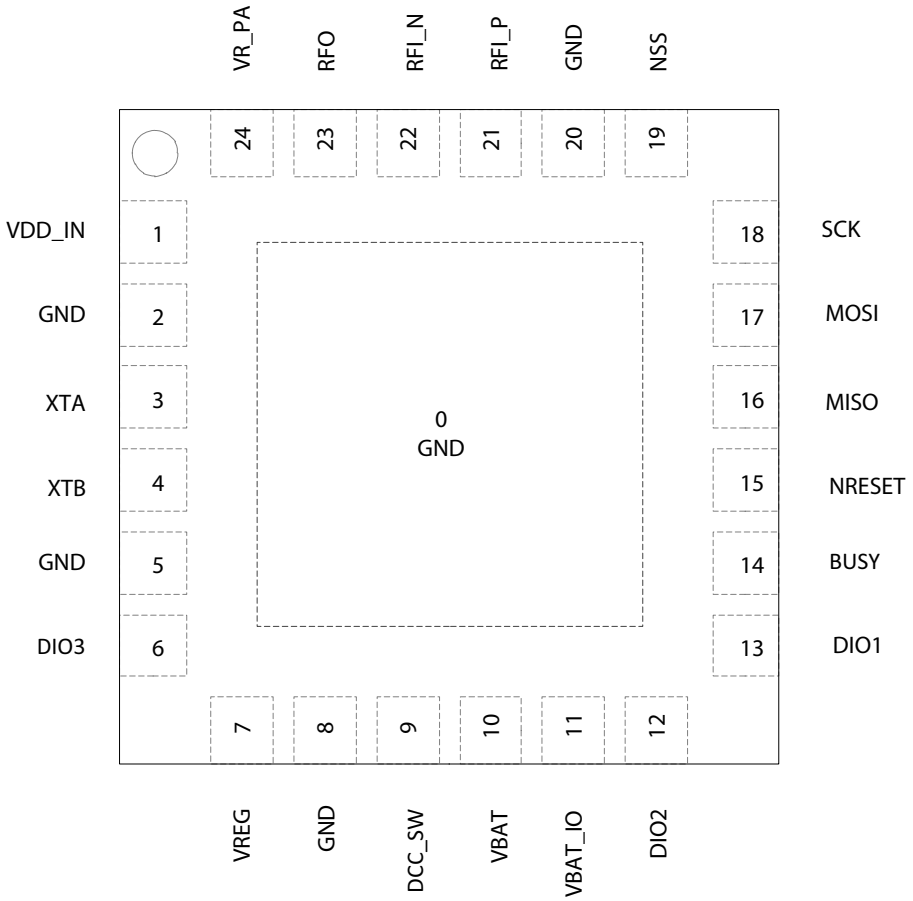

Figure 2-1: SX1261/2 Top View Pin Location QFN 4x4 24L

3. Specifications

3.1 ESD Notice

The SX1261/2 transceivers are high-performance radio frequency devices, with high ESD and latch-up resistance. The chip should be handled with all the necessary ESD precautions to avoid any permanent damage.

Table 3-1: ESD and Latch-up Notice

Symbol	Description	Min	Typ	Max	Unit
ESD_HBM	Class 2 of ANSI/ESDA/JEDEC Standard JS-001-2014 (Human Body Model)	-	-	2.0	kV
ESD_CDM	ESD Charged Device Model, JEDEC standard JESD22-C101D, class III	-	-	1000	V
LU	Latch-up, JEDEC standard JESD78 B, class I level A	-	-	100	mA

3.2 Absolute Maximum Ratings

Stresses above the values listed below may cause permanent device failure. Exposure to absolute maximum ratings for extended periods may affect device reliability, reducing product life time.

Table 3-2: Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Unit
VDDmr	Supply voltage, applies to VBAT and VBAT_IO	-0.5	-	3.9	V
Tmr	Temperature	-55	-	125	°C
Pmr	RF Input level	-	-	10	dBm

3.3 Operating Range

Operating ranges define the limits for functional operation and parametric characteristics of the device. Functionality outside these limits is not guaranteed.

Table 3-3: Operating Range

Symbol	Description	Min	Typ	Max	Unit
VDDop	Supply voltage, applies to VBAT and VBAT_IO	1.8	-	3.7	V
Top	Temperature under bias	-40	-	85	°C
Clop	Load capacitance on digital ports	-	-	20	pF
ML	RF Input power	-	-	0	dBm
VSWR	Voltage Standing Wave Ratio	-	-	10:1	-

3.4 Crystal Specifications

Table 3-4: Crystal Specifications

Symbol	Description	Min	Typ	Max	Unit
FXOSC	Crystal oscillator frequency	-	32	-	MHz
CLOAD	Crystal load capacitance	-	10	-	pF
C0XTAL	Crystal shunt capacitance	0.3	0.6	2	pF
RSXTAL	Crystal series resistance	-	30	60	Ω
CMXTAL	Crystal motional capacitance	1.3	1.89	2.5	fF
DRIVE	Drive level	-	-	100	µW

The reference frequency accuracy is defined by the complete system, and should take into account precision of the transmitter and the receiver, as well as environmental parameters such as extreme temperature limits. In a LoRaWAN™ system, the expected reference frequency accuracy on the end-device should be about +/- 30 ppm under all operating conditions. This includes initial error, temperature drift and ageing over the lifetime of the product.

3.5 Electrical Specifications

The electrical specifications are given with the following conditions unless otherwise specified:

- VBAT_IO = VBAT = 3.3 V, all current consumptions are given for VBAT connected to VBAT_IO
- Temperature = 25 °C
- FXOSC = 32 MHz, with specified crystal
- FRF = 434/490/868/915 MHz
- All RF impedances matched
- Transmit mode output power defined in 50 Ω load
- FSK BER = 0.1%, 2-level FSK modulation without pre-filtering, BR = 4.8 kb/s, FDA = ± 5 kHz, BW_F = 20 kHz double-sided
- LoRa® PER = 1%, packet 64 bytes, preamble 8 symbols, CR = 4/5, CRC on payload enabled, explicit header mode
- RX/TX specifications given using default RX gain step and direct tie connection between Rx and Tx
- Blocking immunity, ACR and co-channel rejection are given for a single tone interferer and referenced to sensitivity +3 dB, blocking tests are performed with unmodulated signal
- Optional TCXO and RF Switch power consumption always excluded

Caution!

Throughout this document, all receiver bandwidths are expressed as "double-sided bandwidth". This is valid for LoRa® and FSK modulations.

3.5.1 Power Consumption

Table 3-5: Power Consumption

Symbol	Mode	Conditions	Min	Typ	Max	Unit
IDDOFF	OFF mode (SLEEP mode with cold start[1])	All blocks off	-	160	-	nA
IDDSL	SLEEP mode (SLEEP mode with warm start [2])	Configuration retained	-	600	-	nA
		Configuration retained + RC64k	-	1.2	-	µA
IDDSBR	STDBY_RC mode	RC13M, XOSC OFF	-	0.6	-	mA
IDDSBX	STDBY_XOSC mode	XOSC ON	-	0.8	-	mA
IDDFS	Synthesizer mode	DC-DC mode used	-	2.1	-	mA
		LDO mode used	-	3.55	-	mA
IDDRX	Receive mode DC-DC mode used	FSK 4.8 kb/s	-	4.2	-	mA
		LoRa® 125 kHz	-	4.6	-	mA
		Rx Boosted[3], FSK 4.8 kb/s	-	4.8	-	mA
		Rx Boosted, LoRa® 125 kHz	-	5.3	-	mA
		LoRa® 125 kHz, VBAT = 1.8 V	-	8.2	-	mA
	Receive mode LDO mode used	FSK 4.8 kb/s	-	8	-	mA
		LoRa® 125 kHz	-	8.8	-	mA
		Rx Boosted, FSK 4.8 kb/s	-	9.3	-	mA
		Rx Boosted, LoRa® 125 kHz	-	10.1	-	mA

1. Cold start is equivalent to device at POR or when the device is waking up from Sleep mode with all blocks OFF, see Section 13.1.1 "SetSleep" on page 66
2. Warm start is only happening when device is waking up from Sleep mode with its configuration retained, see Section 13.1.1 "SetSleep" on page 66
3. For more details on how to set the device in Rx Boosted gain mode, see Section 9.6 "Receive (RX) Mode" on page 57

Table 3-6: Power Consumption in Transmit Mode

Symbol	Frequency Band	PA Match / Condition	Power Output	Typical	Unit
IDDTX SX1261 [1]	868/915 MHz	+14 dBm	+14 dBm, VBAT = 3.3 V	25.5	mA
			+10 dBm VBAT = 3.3 V	18	mA
			+14 dBm, VBAT = 1.8 V	48	mA
			+10 dBm, VBAT = 1.8 V	34	mA
		+14 dBm / optimal settings [2]	+15 dBm, VBAT = 3.3 V	32.5	mA
			+10 dBm VBAT = 3.3 V	15	mA
			+15 dBm, VBAT = 1.8 V	60	mA
			+10 dBm, VBAT = 1.8 V	29	mA
	434/490 MHz	+14 dBm	+15 dBm, VBAT = 3.3 V	25.5	mA
			+14 dBm, VBAT = 3.3 V	21	mA
			+10 dBm, VBAT = 3.3 V	14.5	mA
			+15 dBm, VBAT = 1.8 V	46.5	mA
			+14 dBm, VBAT = 1.8 V	39	mA
			+10 dBm, VBAT = 1.8 V	26	mA
IDDTX SX1262 [3]	868/915 MHz	+22 dBm	+22 dBm	118	mA
			+20 dBm	102	mA
			+17 dBm	95	mA
			+14 dBm	90	mA
		+20 dBm / optimal settings [4]	+20 dBm	84	mA
		+17 dBm / optimal settings [4]	+17 dBm	58	mA
		+14 dBm / optimal settings [4]	+14 dBm	45	mA
	434/490 MHz	+22 dBm	+22 dBm	107	mA
			+20 dBm	90	mA
			+17 dBm	75	mA
			+14 dBm	63	mA
		+20 dBm / optimal settings [4]	+20 dBm	65	mA
		+17 dBm / optimal settings [4]	+17 dBm	42	mA
		+14 dBm / optimal settings [4]	+14 dBm	32	mA

1. For SX1261, DC-DC mode is used for the whole IC. For more details, see Section 5.1 "Selecting DC-DC Converter or LDO Regulation" on page 32.
2. For more details on optimal settings, see Section 13.1.14.1 "PA Optimal Settings" on page 75.
3. For SX1262, DC-DC mode is used for the IC core but the PA is supplied from VBAT. For more details, see Section 5.1 "Selecting DC-DC Converter or LDO Regulation" on page 32.
4. Optimal settings adapted to the specified output power. For more details, see Section 13.1.14.1 "PA Optimal Settings" on page 75

3.5.2 General Specifications

Table 3-7: General Specifications

Symbol	Description	Conditions	Min	Typ	Max	Unit
FR	Synthesizer frequency range	SX1261	150	-	960	MHz
FSTEP	Synthesizer frequency step	-	-	0.95	-	Hz
PHN[1] [2]	Synthesizer phase noise (for 868 / 915 MHz)	1 kHz offset	-	-75	-	dBc/Hz
		10 kHz offset	-	-95	-	dBc/Hz
		100 kHz offset	-	-100	-	dBc/Hz
		1MHz offset	-	-120	-	dBc/Hz
		10 MHz offset	-	-135	-	dBc/Hz
TS_FS	Synthesizer wake-up time	From STDBY_XOSC mode	-	40	-	µs
TS_HOP	Synthesizer hop time	10 MHz step	-	30	-	µs
TS_OSC	Crystal oscillator wake-up time	from STDBY_RC[3]	-	150	-	µs
OSC_TRM	Crystal oscillator trimming range for crystal frequency error compensation [4]	min/max XTAL specifications	+/-15	+/-30	-	ppm
BR_F	Bit rate, FSK	Programmable Minimum modulation index is 0.5	0.6	-	300 [5]	kb/s
FDA	Frequency deviation, FSK	Programmable FDA + BR_F / 2 =< 250 kHz	0.6	-	200	kHz
BR_L	Bit rate LoRa®	Min. for SF12, BW_L = 7.8 kHz Max. for SF5, BW_L = 500 kHz	0.018	-	62.5 [6]	kb/s
BW_L	Signal BW, LoRa®	Programmable	7.8	-	500 [6]	kHz
SF	Spreading factor for LoRa®	Programmable, chips/symbol = 2^SF	5	-	12	-
VTCXO	Regulated voltage range for TCXO voltage supply	Min/Max values in typical conditions, Typ value for default setting VDDop > VTCXO + 200 mV	1.6	1.7	3.3	V
ILTCXO	Load current for TCXO regulator		-	1.5	4	mA
TSVTCXO	Start-up time for TCXO regulator	From enable to regulated voltage within 25 mV from target	-	-	100	µs
IDDTCXO	Current consumption of the TCXO regulator	Quiescent current	-	-	70	µA
		Relative to load current	-	1	2	%
ATCXO	Amplitude voltage for external TCXO applied toXTA pin	provided through a 220 Ω resistor in series with a 10 pF capacitance See Section 4.2 "Phase-Locked Loop (PLL)" on page 24	0.4	0.6	1.2	Vpk-pk

1. Phase Noise specifications are given for the recommended PLL BW to be used for the specific modulation/BR, optimized settings may be used for specific applications
2. Phase Noise is not constant over frequency, due to the topology of the PLL, for two frequencies close to each other, the phase noise could change significantly
3. Wake-up time till crystal oscillator frequency is within +/- 10 ppm
4. OSC_TRIM is the available trimming range to compensate for crystal initial frequency error and to allow crystal temperature compensation implementation; the total available trimming range is higher and allows the compensation for all IC process variations
5. Maximum bit rate is assumed to scale with the RF frequency; for example 300 kb/s in the 869/915 MHz frequency bands and only 50 kb/s at 150 MHz
6. For RF frequencies below 400 MHz, there is a scaling between the frequency and supported BW, some BW may not be available below 400 MHz

3.5.3 Receive Mode Specifications

Table 3-8: Receive Mode Specifications

Symbol	Description	Conditions	Min	Typ	Max	Unit
RXS_2FB	Sensitivity 2-FSK, RX Boosted gain, see Section 9.6 "Receive (RX) Mode" on page 57, split RF paths for Rx and Tx, RF switch insertion loss excluded	BR_F = 0.6 kb/s, FDA = 0.8 kHz, BW_F = 4 kHz	-	-125	-	dBm
		BR_F = 1.2 kb/s, FDA = 5 kHz, BW_F = 20 kHz	-	-123	-	dBm
		BR_F = 4.8 kb/s, FDA = 5 kHz, BW_F = 20 kHz	-	-118	-	dBm
		BR_F = 38.4 kb/s, FDA = 40 kHz, BW_F = 160 kHz	-	-109	-	dBm
		BR_F = 250 kb/s, FDA = 125 kHz, BW_F = 500 kHz	-	-104	-	dBm
RXS_LB	Sensitivity LoRa®, Rx Boosted gain, see Section 9.6 "Receive (RX) Mode" on page 57, split RF paths for Rx and Tx, RF switch insertion loss excluded	BW_L = 10.4 kHz, SF = 7	-	-134	-	dBm
		BW_L = 10.4 kHz, SF = 12	-	-148	-	dBm
		BW_L = 125 kHz, SF = 7	-	-124	-	dBm
		BW_L = 125 kHz, SF = 12	-	-137	-	dBm
		BW_L = 250 kHz, SF = 7	-	-121	-	dBm
		BW_L = 250 kHz, SF = 12	-	-134	-	dBm
		BW_L = 500 kHz, SF = 7	-	-117	-	dBm
		BW_L = 500 kHz, SF = 12	-	-129	-	dBm
RXS_2F	Sensitivity 2-FSK Rx Power Saving gain with direct tie connection between Rx and Tx	BR_F = 4.8 kb/s, FDA = 5 kHz, BW_F = 20 kHz	-	-115	-	dBm
RXS_L	Sensitivity LoRa® Rx Power Saving gain with direct tie connection between Rx and Tx	BW_L = 125 kHz, SF = 12	-	-133	-	dBm
CCR_F	Co-channel rejection, FSK		-	-9	-	dB
CCR_L	Co-channel rejection, LoRa®	SF = 7	-	5	-	dB
		SF = 12	-	19	-	dB
ACR_F	Adjacent channel rejection, FSK	Offset = +/- 50 kHz	-	45	-	dB
ACR_L	Adjacent channel rejection, LoRa®	Offset = +/- 1.5 x BW_L				
		BW_L = 125 kHz, SF = 7	-	60	-	dB
		BW_L = 125 kHz, SF = 12	-	72	-	dB

Table 3-8: Receive Mode Specifications

Symbol	Description	Conditions	Min	Typ	Max	Unit
BI_F	Blocking immunity, FSK	BR_F = 4.8 kb/s, FDA = 5 kHz, BW_F = 20 kHz				
		Offset = +/- 1 MHz	-	68	-	dB
		Offset = +/- 2 MHz	-	70	-	dB
		Offset = +/- 10 MHz	-	80	-	dB
BI_L	Blocking immunity, LoRa®	BW_L = 125 kHz, SF =12				
		Offset = +/- 1 MHz	-	88	-	dB
		Offset = +/- 2 MHz	-	90	-	dB
		Offset = +/- 10 MHz	-	99	-	dB
IIP3	3rd order input intercept point	Unwanted tones are 1 MHz and 1.96 MHz above LO	-	-5	-	dBm
IMA	Image attenuation	Without IQ calibration	-	35	-	dB
		With IQ calibration	-	54	-	dB
BW_F	DSB channel filter BW, FSK	Programmable, typical values	4.8	-	467	kHz
TS_RX	Receiver wake-up time	FS to RX	-	41	-	µs
FERR_L	Maximum tolerated frequency offset between transmitter and receiver, no sensitivity degradation, SF5 to SF12	All bandwidths, ±25% of BW The tighter limit applies (see below)		±25%		BW
	Maximum tolerated frequency offset between transmitter and receiver, no sensitivity degradation, SF10 to SF12	SF12	-50	-	50	ppm
		SF11	-100	-	100	ppm
		SF10	-200	-	200	ppm

3.5.4 Transmit Mode Specifications

Table 3-9: Transmit Mode Specifications

Symbol	Description	Conditions	Min	Typ	Max	Unit
TXOP	Maximum RF output power	Highest power step setting				
		SX1261	-	+14/15 [1]	-	dBm
		SX1262	-	+22	-	dBm
TXDRP	RF output power drop versus supply voltage	SX1261, under DC-DC or LDO VDDop range from 1.8 to 3.7 V	-	0.5	-	dB
		SX1262, +22 dBm, VBAT = 2.7 V	-	2	-	dB
		SX1262, +22 dBm, VBAT = 2.4 V	-	3	-	dB
		SX1262, +22 dBm, VBAT = 1.8 V	-	6	-	dB
TXPRNG	RF output power range	Programmable in 31 steps, typical value	TXOP-31	-	TXOP	dBm
TXACC	RF output power step accuracy		-	± 2	-	dB
TXRMP	Power amplifier ramping time	Programmable	10	-	3400	µs
TS_TX	Tx wake-up time	Frequency Synthesizer enabled	-	36 + PA ramping	-	µs

1. for SX1261 +15 dBm maximum RF output power can be reached with special settings, see Section 13.1.14.1 "PA Optimal Settings" on page 75.

3.5.5 Digital I/O Specifications

Table 3-10: Digital I/O Specifications

Symbol	Description	Conditions	Min	Typ	Max	Unit
VIH	Input High Voltage	-	0.7*VBAT_IO [1]	-	VBAT_IO [1]+0.3	V
VIL	Input Low Voltage	-	-0.3	-	0.3*VBAT_IO [1]	V
VIL_N	Input Low Voltage for pin NRESET	-	-0.3	-	0.2*VBAT	V
VOH	Output High Voltage	I_{max} = -2.5 mA	0.9*VBAT_IO [1]	-	VBAT_IO [1]	V
VOL	Output Low Voltage	I_{max} = 2.5 mA	0	-	0.1*VBAT_IO [1]	V
Ileak	Digital input leakage current (NSS, MOSI, SCK)	-	-1	-	1	µA

1. excluding following pins: NRESET and DIO3, which are referred to VBAT

4. Circuit Description

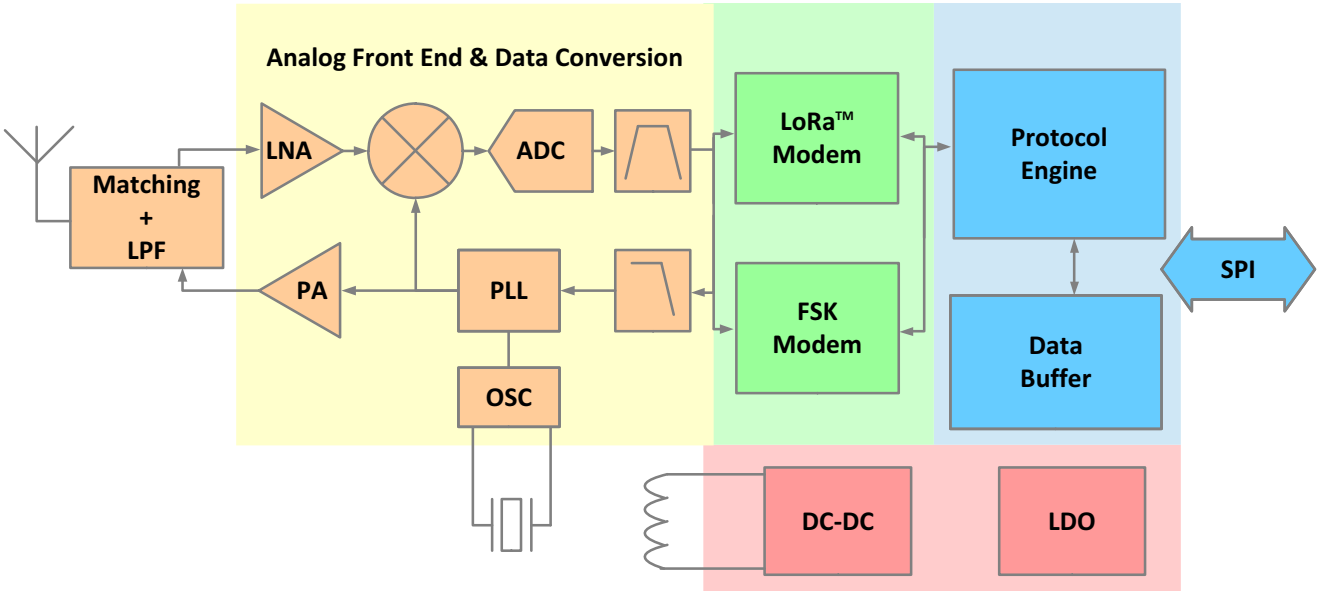

Figure 4-1: SX1261/2 Block Diagram

SX1261 and SX1262 are half-duplex RF transceivers operating in the sub-GHz frequency bands and can handle constant envelope modulations schemes such as LoRa® or FSK.

4.1 Clock References

4.1.1 RC Frequency References

Two RC oscillators are available: 64 kHz and 13 MHz RC oscillators. The 64 kHz RC oscillator (RC64k) is optionally used by the circuit in SLEEP mode to wake-up the transceiver when performing periodic or duty cycled operations. Several commands make use of this 64 kHz RC oscillator (called RTC across this document) to generate time-based events. The 13 MHz RC oscillator (RC13M) is enabled for all SPI communication to permit configuration of the device without the need to start the crystal oscillator. Both RC oscillators are supplied directly from the battery.

4.1.2 High-Precision Frequency Reference

In SX1261/2 the high-precision frequency reference can come either from an on-chip crystal oscillator (OSC) using an external crystal resonator or from an external TCXO (Temperature Compensated Crystal Oscillator), supplied by an internal regulator.

The SX1261/2 comes in a small form factor 4 x 4 mm QFN package with the SX1262 able to transmit up to +22 dBm. When in transmit mode the circuit may heat up depending on the output power and current consumption. Careful PCB design using thermal isolation techniques must be applied between the circuit and the crystal resonator to avoid transferring the heat to the external crystal resonator.

When using the LoRa® modulation with LowDataRateOptimize set to 0x00 (see Section Table 13-50: "LoRa® ModParam4 - LowDataRateOptimize" on page 87), the total frequency drift over the packet transmission time should be minimized and kept lower than *Freq_drift_max*:

$$Freq\_drift\_max = \frac{BW\_L}{3 * 2^{SF}}$$

When possible, using LowDataRateOptimize set to 0x01 will significantly relax the total frequency drift over the packet transmission requirement to 16 x *Freq_drift_max*.

Note:

Recommendations for heat dissipation techniques to be applied to the PCB designs are given in detail in the application note AN1200.37 “Recommendations for Best Performance” on *www.semtech.com*.

In miniaturized design implementations where heat dissipations techniques cannot be implemented or the use of the LowDataRateOptimize is not supported, the use of a TCXO will provide a more stable clock reference.

4.1.3 XTAL Control Block

The SX1261/2 does not require the user to set external foot capacitors on the XTAL supplying the 32 MHz clock. Indeed, the device is fitted with internal programmable capacitors connected independently to the pins XTA and XTB of the device. Each capacitor can be set independently, balanced or unbalanced to each other, by 0.47 pF typical steps.

Table 4-1: Internal Foot Capacitor Configuration

Pin	Register Address	Typical Values
XTA	0x0911	Each capacitor can be controlled independently in steps of 0.47 pF added to the minimal value: 0x00 sets the trimming cap to 11.3 pF (minimum) 0x2F sets the trimming cap to 33.4 pF (maximum)
XTB	0x0912	

Note when using an XTAL:

At POR or when waking-up from Sleep in cold start mode, the trimming cap registers will be initialized at the value 0x05 (13.6 pF). Once the device is set in STDBY_XOSC mode, the internal state machine will overwrite both registers to the value 0x12 (19.7pF). Therefore, the user must ensure the device is already in STDBY_XOSC mode before changing the trimming cap values so that they are not overwritten by the state machine.

Note when using a TCXO:

Once the command *SetDIO3AsTCXOCtrl(...)* is sent to the device, the register controlling the internal cap on XTA will be automatically changed to 0x2F (33.4 pF) to filter any spurious which could occur and be propagated to the PLL.

4.1.4 TCXO Control Block

Under certain circumstances, typically small form factor designs with reduced heat dissipation or environments with extreme temperature variation, it may be required to use a TCXO (Temperature Compensated Crystal Oscillator) to achieve better frequency accuracy. This depends on the complete system, transmitter and receiver. The specification FERR_L in Section Table 3-8: "Receive Mode Specifications" on page 19 provides information on the maximum tolerated frequency offset for optimal receiver performance.

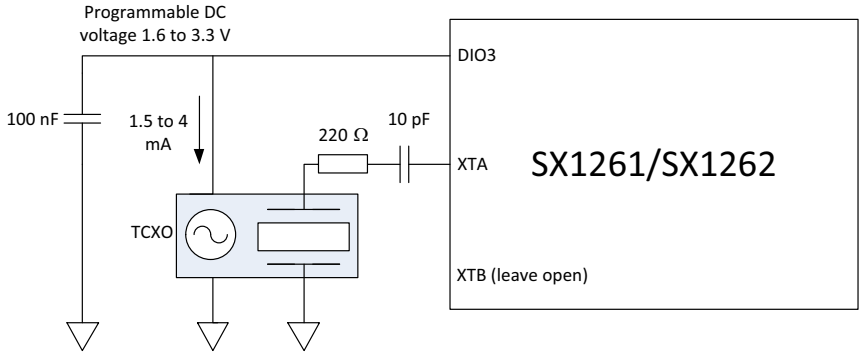

Figure 4-2: TCXO Control Block

When a TCXO is used, it should be connected to pin 3 XTA, through a 220 Ω resistor and a10 pF DC-cut capacitor. Pin 4 XTB should be left open. Pin 6 DIO3 can be used to provide a regulated DC voltage to power the TCXO, programmable from 1.6 to 3.3 V. VBAT should always be 200 mV higher than the programmed voltage to ensure proper operation.

The nominal current drain is 1.5 mA, but the regulator can support up to 4 mA of load. Clipped-sine output TCXO are required, with the output amplitude not exceeding 1.2 V peak-to-peak. The commands to enable TCXO mode are described in Section 13.3.6 "SetDIO3AsTCXOCtrl" on page 80, and that includes DC voltage and timing information.

Note:

A complete Reset of the chip as described in Section 8.1 "Reset" on page 49 is required to get back to normal XOSC operation, after the chip has been set to TCXO mode with the command *SetDIO3AsTCXOCtrl*.

4.2 Phase-Locked Loop (PLL)

A fractional-N third order sigma-delta PLL acts as the frequency synthesizer for the LO of both receiver and transmitter chains. SX1261/2 is able to cover continuously all the sub-GHz frequency range 150-960 MHz. The PLL is capable of auto-calibration and has low switching-on or hopping times. Frequency modulation is performed inside the PLL bandwidth. The PLL frequency is derived from the crystal oscillator circuit which uses an external 32 MHz crystal reference.

4.3 Receiver

The received RF signal is first amplified by a differential Low Noise Amplifier (LNA), then down-converted to low- IF intermediate frequency by mixers operating in quadrature configuration. The I and Q signals are low-pass filtered and then digitized by a continuous time feedback architecture ΣΔ converter (ADC) allowing more than 80 dB dynamic range. Once in the digital domain the signal is then decimated, down-converted again, decimated again, channel filtered and finally demodulated by the selected modem depending on modulation scheme: FSK modem or LoRa® modem.

4.3.1 Intermediate Frequencies

The SX1261/2 receiver mostly operates in low-IF configuration, expect for specific high-bandwidth settings.

Table 4-2: Intermediate Frequencies in FSK Mode

Setting Name	Bandwidth [kHz DSB]	Intermediate Frequency [kHz]
RX_BW_467	467.0	250
RX_BW_234	234.3	250
RX_BW_117	117.3	250
RX_BW_58	58.6	250
RX_BW_29	29.3	250
RX_BW_14	14.6	250
RX_BW_7	7.3	250
RX_BW_373	373.6	200
RX_BW_187	187.2	200
RX_BW_93	93.8	200
RX_BW_46	46.9	200
RX_BW_23	23.4	200
RX_BW_11	11.7	200
RX_BW_5	5.8	200
RX_BW_312	312.0	167
RX_BW_156	156.2	167
RX_BW_78	78.2	167
RX_BW_39	39.0	167
RX_BW_19	19.5	167
RX_BW_9	9.7	167
RX_BW_4	4.8	167