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SX1280/SX1281

Long Range, Low Power, 2.4 GHz Transceiver with Ranging Capability

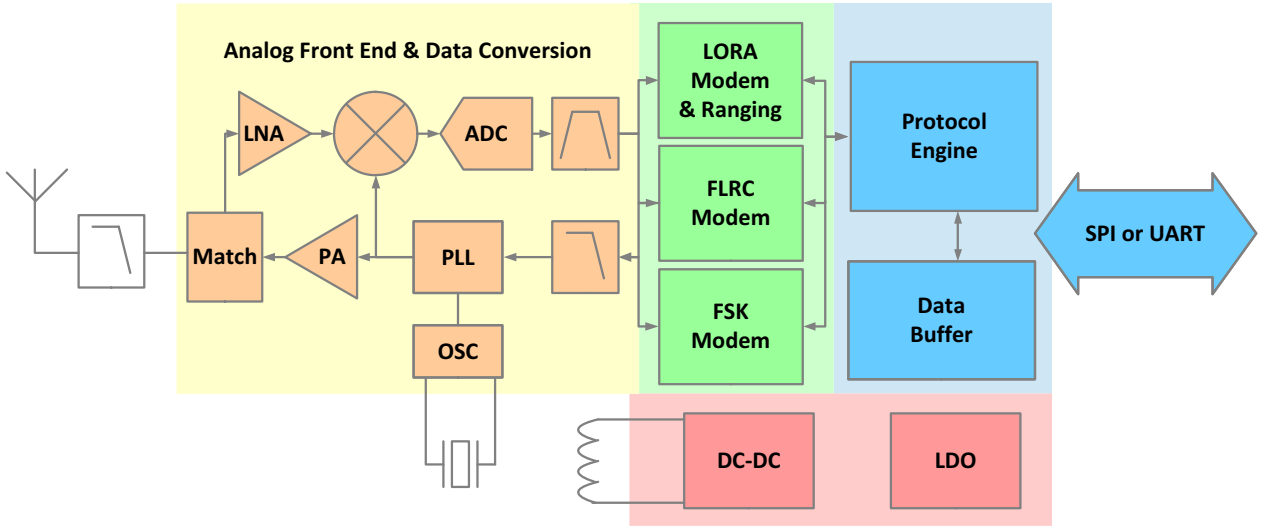

Figure A: Transceiver Block Diagram

General Description

The SX1280 and SX1281 transceivers provide ultra long range communication in the 2.4 GHz band with the linearity to withstand heavy interference. This makes them the ideal solution for robust and reliable wireless solutions. They are the first ISM band transceiver IC of their kind to integrate a time-of-flight functionality, opening up application solutions to track and localize people, pets, drones, or objects in a factory. These long range 2.4 GHz products include multiple physical layers and modulations to optimize long range communication at high data rate for video and security applications. Very small products for wearables can easily be designed thanks to the high level of integration and the ultra-low current consumption which allows the use of miniaturized batteries.

The radio is fully compliant with all worldwide 2.4 GHz radio regulations including EN 300 440, FCC CFR 47 Part 15 and the Japanese ARIB STD-T66.

The level of integration, low consumption and ranging function within the long range 2.4 GHz product line enable enhanced connectivity and provide additional functionality to a new generation of previously unconnected devices and applications.

Key Features

- Long Range 2.4 GHz transceiver
- High sensitivity, down to -132 dBm
- +12.5 dBm, high efficiency PA
- Low energy consumption, on-chip DC-DC
- LoRa®, FLRC, (G)FSK supported modulations
- Programmable bit rate
- Excellent blocking immunity
- Ranging Engine, Time-of-flight function
- BLE PHY layer compatibility
- Low system cost

Applications

- Home automation & appliances
- Security systems
- Tracking applications
- Wearables & sports/fitness sensors
- Radio-controlled toys & drones
- Smart watches & beacons
- Healthcare

Ordering Information

Part Number	Delivery	Order Quantity
SX1280IMLTRT	Tape & Reel	3'000 pieces
SX1281IMLTRT	Tape & Reel	3'000 pieces

QFN 24 Package, with the temperature operating range from -40 to 85°C

Pb-free, Halogen free, RoHS/WEEE compliant product

Revision History

Version	ECO	Date	Changes and/or Modifications
Rev 1.0	035543	February 2017	First Release
Rev 1.1	037029	May 2017	Added table of effective data rates for the LoRa® Modem Correction of the formulas for time-on-air in LoRa® Correction of typos in the chapter Host Controller Interface Update of the application schematic with optional TCXO Update of the reference design BOM Deletion of redundant information in the chapter Thermal Impedance
Rev 2.0	040575	February 2018	The maximum SPI clock speed is reduced to 18 MHz Addition of a note in chapter 6.2.3 "Bandwidth" on SF and BW to be known in advance Addition of chapter 6.2.6 "Frequency Error" Addition of calculations of time-on-air in chapter 7.5 "LoRa Ranging Engine Packet" Addition of examples of SPI communication in chapter 11 "Host Controller Interface" Update of explanation on SetAutoTx in chapter 13.2.4 "BLE Specific Functions" Update of ranging results description in chapter 13.5 "Ranging Operation" Addition of an explanation of the Reference Design in chapter 14.1 "Reference Design" Addition of the tape and reel specifications in chapter 15 "Packaging Information" Addition of LoRa® and Bluetooth® trademark information

Version	ECO	Date	Changes and/or Modifications (Continued)
Rev 2.1	041639	April 2018	Maximum RF input power (ML) is now 0 dBm Phase noise at 2.45 GHz with 1 MHz offset (PHN) is now -115 dBc/Hz Correction of minor typographical errors in tables 6-5, 6-7, 13-20 and in chapter 7.2 Addition of formulas for ranging duration in chapter 7.5.4 Addition of description of RSSI packet for LoRa® when SNR ≤ 0 in table 11-64 Correction of package thickness to 0.9 mm in chapter 15.1 Addition of package marking in chapter 15.2
Rev 2.2	041738	May 2018	The following specifications have been changed: • The 3rd order input intercept for maximum low power gain setting (IIP3) - at 6 MHz offset, has been changed from -6 dBm to -12 dBm - at 10 and 20 MHz offset, has been improved from -6 dBm to 0 dBm • IDDSTDBYRC has been improved from 760 µA to 700 µA • IDDSTDBYXOSC has been improved from 1.2 mA to 1 mA • PHN 10 MHz has been improved from -133 dBc/Hz to -135 dBc/Hz • TS_OS has been improved from 100 µs to 40 µs • RFSHS_L , SF7, BW = 1625 kHz, has been changed from -109 dBm to -108 dBm The switching times have been modified for the following transitions: • SLEEP to STDBY_RC from 1700 µs to 1200 µs • SLEEP to STDBY_RC from 250 µs to 130 µs • STDBY_RC to STDBY_XOSC from 53 µs to 40 µs • STDBY_RC to FS from 83 µs to 55 µs • STDBY_RC to Rx from 115 µs to 85 µs • STDBY_RC to Tx from 102 µs to 80 µs • STDBY_XOSC to FS from 40 µs to 54 µs Table 6-2 now gives the raw data rates when using LoRa® Formulas of time-on-air for long interleaving in LoRa® mode have been updated in chapter 7.4.4

Table of Contents

List of Figures

List of Tables

1. Introduction

The SX1280 and SX1281 are half-duplex transceivers capable of low power operation in the worldwide 2.4 GHz ISM band. The radio comprises 5 main parts, which are described in the following chapters.

1.1 Analog Front End

The radio features a high efficiency +12.5 dBm transmitter and a high linearity receive chain that are both accessed via a common antenna port pin. Frequency conversion between RF and baseband (low-IF) is governed by a digital PLL that is referenced to a 52 MHz crystal. Both transmit and receive chains are interfaced by data converters to the ensuing digital blocks. For more information see the Section 4. "Analog Front End" on page 25 .

1.2 Power Distribution

Two forms of voltage regulation are available, either a integrated Low-DropOut (LDO) or a high efficiency buck (step down) DC to DC converter. This allows the designer to choose between high energy efficiency or miniaturisation of the radio depending upon the design priorities of the application. For more information, please see the Section 5. "Power Distribution" on page 28 .

1.3 Modem

There are a range of modulation options available in the LoRa® family's three modems, each of which has packet options that include many MAC layer functionalities. For a description of each modulation format and the performance benefits associated with that modulation, please see the corresponding section below:

- LoRa® Modem and Packet: Section 6.2 "LoRa® Modem" on page 31
- FLRC Modem and Packet: Section 6.3 "FLRC Modem" on page 34
- FSK Modem and Packet: Section 6.4 "FSK Modem" on page 37

The long range 2.4 GHz product line also features the Ranging Engine, a long distance ranging functionality that permits round-trip time-of-flight measurement between a pair of LoRa® radios. The availability of each modem and the Ranging Engine, for each part number in the long range 2.4 GHz product line is shown below.

Table 1-1: Product Portfolio and Modem Functionality

Product Reference	SX1280	SX1281
LoRa®	✓	✓
FLRC	✓	✓
GFSK	✓	✓
Ranging Engine	✓	

1.4 Packet Processing

The radio can operate in a fully automatic mode where the processing of packets for transmission or reception can be performed without the intervention of an external host micro-controller. For more details see Section 7. "Packet Engine" on page 40 .

In both transmit and receive modes the payload interface to the transceiver is the packet data buffer described in Section 8. "Data Buffer" on page 53 of this datasheet.

1.5 Digital Interface and Control

The specification and processing for all digital communication with the transceiver is described in Section 9. "Digital Interface and Control" on page 55 . This includes descriptions of the SPI and UART interfaces, that can be used to configure the transceiver together with the Digital Input / Output (DIO) that are used to send interrupts to an external host micro-controller.

- For the SPI interface see Section 9.3 "SPI Interface" on page 56
- For the UART interface see Section 9.4 "UART Interface" on page 59
- For the DIO see Section 9.6 "Multi-Purpose Digital Input/Output (DIO)" on page 59

2. Pin Connections

2.1 Transceiver Pinout

Table 2-1: Transceiver Pinout

Pin Number	Pin Name	Type (I = input O = Output)	SPI description	UART description
0	GND	-	Exposed Ground pad	
1	VR_PA	-	Regulated supply for the PA	
2	VDD_IN	I	Regulated supply input. Connect to Pin 12.	
3	NRESET	I	Reset signal, active low with internal pull-up at 50 kΩ	
4	XTA	-	Reference oscillator connection or TCXO input	
5	GND	-	Ground	
6	XTB	-	Reference oscillator connection	
7	BUSY	O	Transceiver busy indicator	
8	DIO1	I/O	Optional multi-purpose digital I/O	
9	DIO2	I/O	Optional multi-purpose digital I/O	
10	DIO3	I/O	Optional multi-purpose digital I/O	
11	VBAT_IO	I	Supply for the Digital IO interface (1.8 V to 3.7 V). Must be ≤ VBAT.	
12	DCC_FB	O	Regulated output voltage from the internal regulator	
13	GND	-	Ground	
14	DCC_SW	O	DC-DC Switcher Output	
15	VBAT	I	Supply for the RFIC (1.8 V to 3.7 V). Must be ≥ VBAT_IO.	
16	MISO_TX	O	SPI slave output	UART Transmit pin
17	MOSI_RX	I	SPI slave input	UART Receive pin
18	SCK_RTSN	I	SPI clock	UART Request To Send
19	NSS_CTS	I	SPI Slave Select	UART Clear To Send
20	GND	-	Ground	
21	GND	-	Ground	
22	RFIO	I/O	RF transmit output and receive input	
23	GND	-	Ground	
24	GND	-	Ground	

2.2 Package view

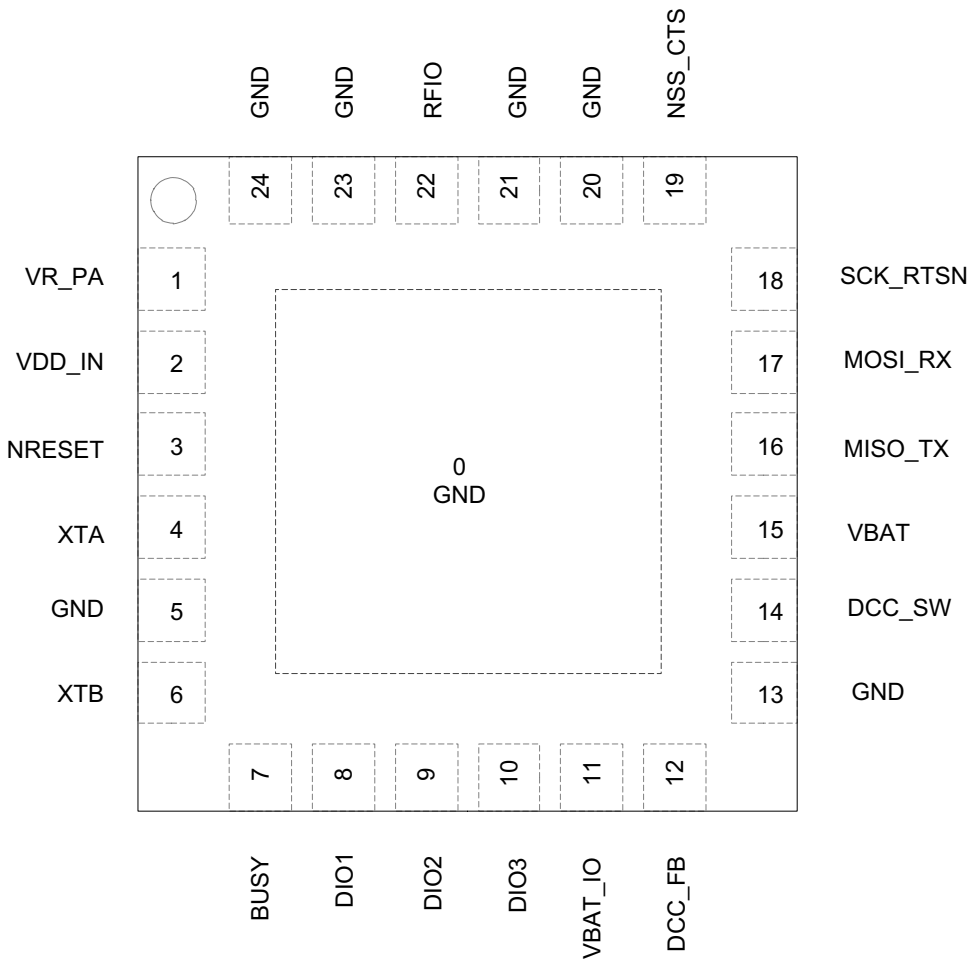

Figure 2-1: Transceiver Pin Locations

3. Specifications

The following specifications are given for the typical operating conditions of VBAT_IO = VBAT = 3.3 V, temperature = 25 °C, crystal oscillator frequency = 52 MHz, RF centre frequency = 2.4 GHz. All RF impedances are matched using the reference design, see Section 14.1 "Reference Design" on page 127. Blocking, ACR and co-channel rejection are given for a single tone interferer and referenced to sensitivity level +6 dB. The current supply is given as the sum of current on VBAT and VBAT_IO. The buck converter (DC-DC) is considered switched ON unless otherwise stated.

3.1 ESD Notice

The SX1280/SX1281 transceivers are high-performance radio frequency devices.

They all satisfy:

- Class 2 of the JEDEC standard JESD22-A114 (Human Body Model) on all pins
- Class III of the JEDEC standard JESD22-C101 (Charged Device Model) on all pins

3.2 Absolute Minimum and Maximum Ratings

Table 3-1: Minimum and Maximum Ratings

Symbol	Description	Minimum	Typical	Maximum	Unit
VBATmr	Supply voltage on VBAT and VBAT_IO	-0.5	-	3.9	V
Tmr	Temperature	-55	-	115	°C
Pmr	RF Input level	-	-	10	dBm

3.3 Operating Range

Table 3-2: Operating Range

Symbol	Description	Minimum	Typical	Maximum	Unit
VBATop	Supply voltage VBAT and VBAT_IO	1.8	-	3.7	V
Top	Temperature under bias	-40	-	85	°C
Clop	Load capacitance on digital ports	-	-	10	pF
ML	RF Input power	-	-	0	dBm

3.4 General Electrical Specifications

Table 3-3: General Electrical Specifications

Symbol	Description	Minimum	Typical	Maximum	Unit
IDDSL	Supply current in Sleep mode with - data RAM not retained - data buffer retained - instruction RAM flushed	-	0.215	1.0	µA
	Supply current in Sleep mode with - data RAM retained (context saved) - data buffer flushed - instruction RAM flushed	-	0.25	1.0	µA
	Supply current in Sleep mode with - data RAM retained - data buffer flushed - instruction RAM retained	-	0.4	1.0	µA
	Supply current in Sleep mode with - data RAM retained - data buffer retained - instruction RAM retained RC64k is running	-	1.2	1.8	µA
IDDSTDBYRC	Supply current in STDBY_RC mode	-	700	-	µA
IDDSTDBYXOSC	Supply current in STDBY_XOSC mode	-	1	-	mA
IDDFS	Supply current in FS mode	-	2.8	-	mA
FR	Synthesizer frequency range	2400	-	2500	MHz
FSTEP	Synthesizer frequency step (52 MHz reference)	-	198	-	Hz
PHN	Phase noise at 2.45 GHz				
	1 MHz offset	-	-115	-	dBc/Hz
	10 MHz offset	-	-135	-	dBc/Hz
FXOSC	Crystal oscillator frequency	-	52	-	MHz
TS_FS	Frequency synthesizer wake-up time with XOSC enabled	-	54	-	µs
TS_HOP	Frequency synthesizer hop time to within 10 kHz of target frequency				
	1 MHz	-	20	-	µs
	10 MHz	-	30	-	µs
	100 MHz	-	50	-	µs
TS_OS	Crystal oscillator wake-up time from STDBY_RC mode	-	40	-	µs

For the digital specifications, see Table 10-2: "Switching Time (TswMode) for all Possible Transitions" on page 63.

3.5 Receiver Electrical Specifications

All receiver sensitivity numbers are given for a Packer Error Rate (PER) of 1%, for packet with 10 bytes of payload.

Values are given for maximum AGC gain which is the highest low power gain.

A continuous wave (CW) interferer is used for all blocking and rejection measurements unless otherwise stated.

3.5.1 Receiver Specifications

Table 3-4: Receiver Specifications

Symbol	Description	Minimum	Typical	Maximum	Unit
IIP3	3rd Order input intercept for maximum low power gain setting				
	In-band interferer <6 MHz	-	-25	-	dBm
	In-band interferer at 6 MHz offset	-	-12	-	dBm
	In-band interferer at10 MHz offset	-	0	-	dBm
	In-band interferer at 20 MHz offset	-	0	-	dBm
IMR	Image rejection (CW tone 1% PER)	-	30	-	dB

3.5.2 LoRa® Modem

Table 3-5: LoRa® Modem Specifications

Symbol	Description	Minimum	Typical	Maximum	Unit
IDDRXLP_L	Supply current for low power mode				
	for BW = 203 kHz	-	5.5	-	mA
	for BW = 406 kHz	-	6.0	-	mA
	for BW = 812 kHz	-	7.0	-	mA
	for BW = 1625 kHz	-	7.5	-	mA
IDDRXHS_L	Supply current for high sensitivity mode				
	for BW = 203 kHz	-	6.2	-	mA
	for BW = 406 kHz	-	6.7	-	mA
	for BW = 812 kHz	-	7.7	-	mA
	for BW = 1625 kHz	-	8.2	-	mA
RB_L	LoRa® bitrate programmable range with CR = 4/5				
	SF5, BW = 1625 kHz	-	202	-	kb/s
	SF6, BW = 1625 kHz	-	122	-	kb/s
	SF7, BW = 1625 kHz	-	71	-	kb/s
	SF12, BW = 203 kHz	-	0.476	-	kb/s
BW_L	LoRa® bandwidth programmable range	203	-	1625	kHz
RFSLP_L	LoRa® receiver sensitivity with CR = 4/5 and low power mode enabled [1]				
	SF7, BW = 1625 kHz,	-	-106	-	dBm
	SF12, BW = 203 kHz	-	-130	-	dBm
RFSHS_L	LoRa® receiver sensitivity with CR = 4/5 and high sensitivity mode enabled 1				
	SF7, BW = 1625 kHz,	-	-108	-	dBm
	SF12, BW = 203 kHz	-	-132	-	dBm
CCR_L	Co-channel rejection LoRa®				
	SF7	-	7.5	-	dB
	SF12	-	19.5	-	dB
BI_L	Blocking immunity SF12				
	+/- 1 MHz	-	60	-	dB
	+/- 2 MHz	-	63	-	dB
	+/- 10 MHz	-	81	-	dB

Table 3-5: LoRa® Modem Specifications

Symbol	Description	Minimum	Typical	Maximum	Unit
ACR_L	Adjacent channel rejection at 1.5 BW of CW				
	SF = 12, BW = 203 kHz	-	37	-	dB
	SF = 7, BW = 1.6 MHz	-	37	-	dB

1. See Section 4.2.1 "Low Power Mode and High Sensitivity Mode" on page 27.

3.5.3 FLRC Modem

Table 3-6: FLRC Modem Specifications

Symbol	Description	Minimum	Typical	Maximum	Unit
IDDRX_FL	Supply currents				
	BW = 300 kHz, BR = 260 kb/s	-	6.5	-	mA
	BW = 1200 kHz, BR = 1300 kb/s	-	8.6	-	mA
RB_FL	FLRC Modem programmable bitrate	260	-	1300	kb/s
BW_FL	Programmable channel bandwidth range	300	-	2400	kHz
RFS_FL	FLRC Receiver Sensitivity				
	260 kSymb/s, 130 kb/s BW = 300 kHz CR=1/2	-	-106	-	dBm
	2.6 MSymb/s, 1.3 Mb/s, BW = 2.4 MHz, CR=1/2	-	-97	-	dBm
CCR_FL	Co-channel rejection FLRC	-	-10	-	dB
BI_FL	Blocker level for Max low power gain setting				
	+/- 1 MHz	-	41	-	dB
	+/- 2 MHz	-	44	-	dB
	+/- 10 MHz	-	62	-	dB
	+/- 20 MHz	-	69	-	dB
ACR_FL	Adjacent channel rejection at 1.5 BW for CW				
	260 kb/s, BW = 300 kHz	-	44	-	dB
	1.3 Mb/s, BW = 2.4 MHz	-	49	-	dB

Notice: all data rates listed in the table above are in raw bits. All values are given with BT = 0.5.

3.5.4 FSK Modem

Table 3-7: FSK Modem Specifications

Symbol	Description	Minimum	Typical	Maximum	Unit
IDDRX_FSK_250_LP	Supply currents for low power mode, demodulation running[1]				
	BW = 300 kHz, BR = 250 kb/s	-	4.8	-	mA
IDDRX_FSK_1000_LP	BW = 1200 kHz, BR = 1000 kb/s	-	5.3	-	mA
IDDRX_FSK_2000_LP	BW = 2400 kHz, BR = 2000 kb/s	-	5.7	-	mA
IDDRX_FSK_250_HS	Supply currents for high sensitivity mode, demodulation running[1]				
	BW = 300 kHz, BR = 250 kb/s	-	5.5	-	mA
IDDRX_FSK_1000_HS	BW = 1200 kHz, BR = 1000 kb/s	-	6.0	-	mA
IDDRX_FSK_2000_HS	BW = 2400 kHz, BR = 2000 kb/s	-	6.4	-	mA
BR_FSK	FSK Modem programmable bitrate	125	-	2000	kb/s
BW_FSK	Programmable channel bandwidth range DSB	300	-	2400	kHz
RFS_FSK1 low power mode	FSK Receiver Sensitivity BER 0.1%				
	250 kb/s, β = 0.5, BW = 300 kHz	-	-100	-	dBm
	1 Mb/s, β = 0.5, BW = 1200 kHz	-	-94	-	dBm
RFS_FSK1_HS high sensitivity mode	FSK Receiver Sensitivity BER 0.1%				
	250 kb/s, β = 0.5, BW = 300 kHz	-	-102	-	dBm
	1 Mb/s, β = 0.5, BW = 1200 kHz	-	-96	-	dBm
RFS_FSK2 low power mode	FSK Receiver Sensitivity PER 1%				
	250 kb/s, β = 0.5, BW = 300 kHz	-	-93	-	dBm
	1 Mb/s, β = 0.5, BW = 1200 kHz	-	-88	-	dBm
RFS_FSK2_HS high sensitivity mode	FSK Receiver Sensitivity PER 1%				
	250 kb/s, β = 0.5, BW = 300 kHz	-	-94	-	dBm
	1 Mb/s, β = 0.5, BW = 1200 kHz	-	-90	-	dBm
CCR_FSK	Co-Channel Rejection	-	-10	-	dB
BI_FSK	Blocker level for max low power gain setting, BR = 250 kb/s, BW = 300 kHz				
	+/- 1 MHz	-	41	-	dB
	+/- 2 MHz	-	44	-	dB
	+/- 10 MHz	-	62	-	dB
	+/- 20 MHz	-	69	-	dB

Table 3-7: FSK Modem Specifications

Symbol	Description	Minimum	Typical	Maximum	Unit
ACR_FSK	Adjacent channel rejection at 1.5 BW for CW				
	BW = 300 kHz	-	34	-	dB
	BW = 1200 kHz	-	34	-	dB

1. See Section 4.2.1 "Low Power Mode and High Sensitivity Mode" on page 27.

Notice: all values listed in the table above are given with the modulation index β = 0.5.

3.6 Transmitter Electrical Specifications

Table 3-8: Transmitter Electrical Specifications

Symbol	Description	Minimum	Typical	Maximum	Unit
IDD_T13	12.5 dBm	-	24	-	mA
IDD_T10	10 dBm	-	18	-	mA
IDD_T0	0 dBm	-	10	-	mA
RFOPMIN	Minimum RF output power	-	-18	-	dBm
RFOPMAX	Maximum RF output power	-	12.5	-	dBm
FDA	Programmable FSK frequency deviation	62.5	-	1000	kHz

3.7 Crystal Oscillator Specifications

Table 3-9: Crystal Oscillator Specifications

Symbol	Description	Minimum	Typical	Maximum	Unit
FXOSC	Crystal oscillator frequency	-	52	-	MHz
CLOAD	Crystal loading capacitance	-	10	-	pF
C0XTAL	Crystal shunt capacitance	-	2	5	pF
RSXTAL	Crystal series resistance	-	10	50[1]	Ω
CMXTAL	Crystal motional capacitance	3	3.5[2]	4	fF

1. An RSXTAL of up to 90 Ω may be used if C0XTAL is restricted to < 3 pF.
2. Other CMXTAL values may be used, noting that smaller values reduce start up time whilst larger values will degrade frequency accuracy and phase noise.

3.8 Digital Pin Levels

Table 3-10: Digital Levels and Timings

Symbol	Description	Minimum	Typical	Maximum	Unit	Conditions
V_{IH}	Digital input level high	0.8	-	-	VBAT_IO	-
V_{IL}	Digital input level low	-	-	0.2	VBAT_IO	-
V_{OH}	Digital output level high	0.9	-	-	VBAT_IO	I_{max} = 2.5 mA
V_{OL}	Digital output level low	-	-	0.1	VBAT_IO	I_{max} = -2.5 mA
I_{Leak}	Digital input leakage current (NSS, MOSI, SCK)	-1	-	1	µA	-

4. Analog Front End

The analog front end features a single antenna port connection to an integrated matching circuit that permits half- duplex operation of the radio without external RF switching.

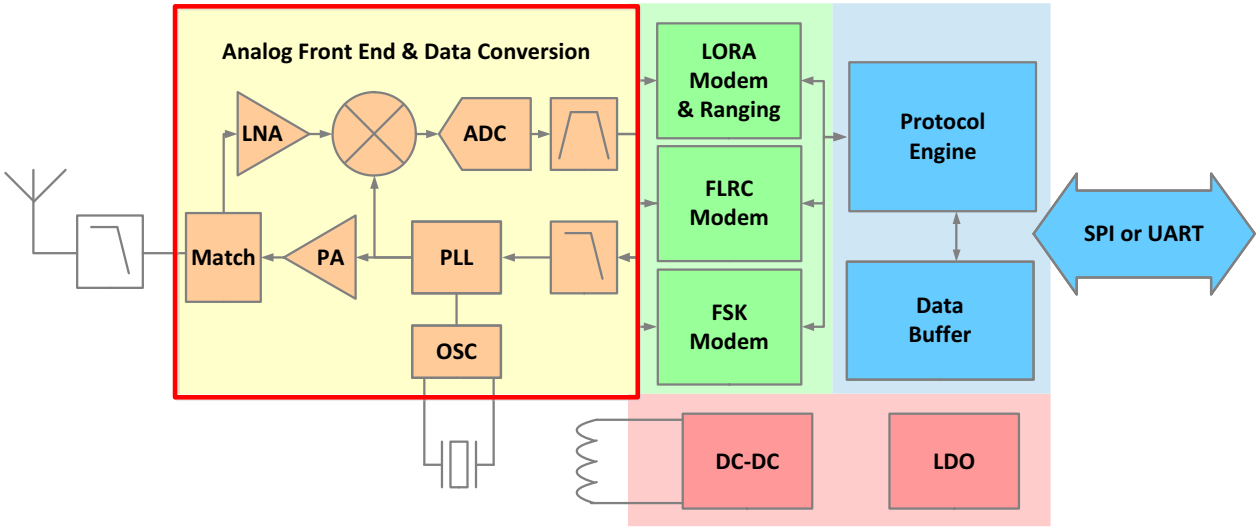

Figure 4-1: Transceiver Block Diagram, Analog Front End Highlighted

4.1 Transmitter

The transmit chain comprises the modulated output from the modem bank which directly modulates the fractional-N PLL. An optional pre-filtering of the bit stream can be enabled to reduce the power in the adjacent channels, also dependent upon the selected modulation type.

The transmitter is enabled by using the *SetTx(periodBase, periodBaseCount)* command. Upon issuing this command, the transmitter sends the packet stored in the data buffer. The transmitter then returns to STDBY_RC mode, either upon completion of the packet transmission, or after a time-out period predefined by the time base of the interrupt timer, *periodBase*, and the preset number of clock ticks *periodBaseCount* as in Section 12. "List of Commands" on page 89.

The RF output power of the transmitter is controllable in 1 dB increments in the range -18 dBm to +12 dBm, the final power step is then a 0.5 dB increment to the maximum transmitter output power of 12.5 dBm. The RF output power (PRF) and the ramp time are determined by the command *SetTxParam(power, rampTime)*. The output power is set using the formula:

$$P_{RF} = -18 + power$$

Where the maximum output power P_{RF} is 12.5 dBm.

This corresponds to the RF output power at the antenna feed-point of the reference design (see Section 14.1.1 "Application Design Schematic" on page 127). Switching of an RF power amplifier can cause undesirable spurious spectral emissions. A precision DAC is therefore used as a reference for the transceiver PA supply voltage allowing smooth transition to transmit mode. The time over which the PA is ramped, prior to packet transmission, *rampTime* can be varied from 2 to 20 µs accordingly. In some applications, and for regulatory testing purposes it can be useful to generate a continuous wave (CW) tone in transmit mode or enable a continuously modulated output. These two functionalities are accessible through the *SetTxContinuousWave()* and *SetTxContinuousPreamble()* functions. The latter provides a stream of alternating logical '1' and '0' modulated data using the configured modulation settings.