Chipsmall

Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of "Quality Parts,Customers Priority,Honest Operation,and Considerate Service",our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!
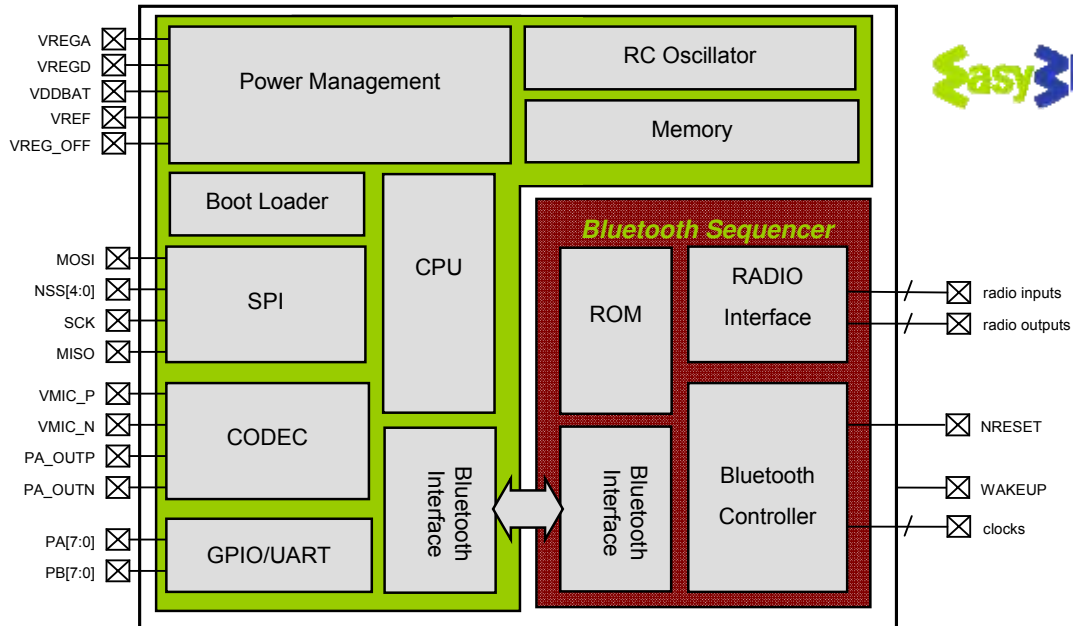
Contact us

SEMTECH

Personal Area Network

SX1441

Ultra Low Power Bluetooth® V1.2 Soc for Wireless Headset and Data Applications with DSP Capabilities

GENERAL DESCRIPTION

The SX1441 is a Bluetooth® System-on-Chip based on the Semtech Bluetooth Sequencer, which includes a fully programmable 8-bit application microcontroller, a high speed UART, SPI interface, RC oscillator, power management unit, and an on-chip voice CODEC with DMA interface. The purpose of the SX1441 is to offer a very high level of integration requiring a minimum of external components to build complete voice and data applications whilst maintaining design flexibility.

This product has been designed for ultra low power consumption and low cost solutions. By combining the SX1441 with a low power 2.4 GHz radio device such as the XE1413, from Semtech, an ultra low power Bluetooth wireless headset consuming less than 23mW @1.8V (HV3) can be built.

APPLICATIONS

- Bluetooth wireless headset
- Handsfree kit
- VoIP, VoRF
- Cable replacement
- Computer accessories

KEY PRODUCT FEATURES

- Ultra low power single-chip Bluetooth SoC, fully Bluetooth rev 1.2 compliant. Supports AFH, Fast Connect and eSCO
- Fully integrated Bluetooth protocol stack up to the HCI, compliant to revision 1.2
- On-chip 16-bit audio linear Codec with DMA interface, preamplifier and audio power amplifier
- Minimum of external components required
- Small form factor
- On-chip battery level detector
- High speed general purpose UART
- Supports simultaneously one SCO and up to three ACL channels
- On-chip MCU and ROM/SRAM memory
- Ni-MH or Li-ion polymer rechargeable battery operation. Supply voltage range 1.8V to 3.6V
- Ultra low power consumption
- Supports CX72303 and XE1413 BT 1.2 radios

ORDERING INFORMATION

Part Number	Description
SX1441IO77TR LF	Bluetooth SoC for voice and data applications

Table of Contents

1   APPLICATION INFORMATION – SX1441-BASED SYSTEM LEVEL BLOCK DIAGRAM

The Semtech SX1441, a member of the EasyBlue™ family, is based on a unique Embedded-Host architecture which enables any data or voice application to be enhanced with ultra low power Bluetooth technology, with low risk and a short development time.

The core of the SX1441 is the Semtech ROM-based Bluetooth sequencer combined with an embedded 8-bit RISC microcontroller and several standard peripherals such as GPIO, high speed UART, audio CODEC, and a power management unit. The Bluetooth sequencer executes the lower layers of the Bluetooth stack, while the microcontroller runs the application and the higher levels of the protocol. Since the sequencer and the microcontroller are independent, the effort required for validation and qualification of the Bluetooth protocol is greatly decreased.

A typical wireless headset block diagram using the SX1441 is shown in Figure 1. The on-chip CODEC is connected with a microphone and a speaker. The Serial Peripheral Interface (SPI) directly interfaces to an external Flash memory. This memory stores the application and the upper layers of the Bluetooth protocol stack which are loaded at boot-up time, and then executed by the on-chip application processor.

Fully programmable General Purpose Input/Output ports (GPIO) are available to interface push-buttons, LED's or other peripherals. The high speed UART supports hardware flow control and data rates up to 921kbit/s.
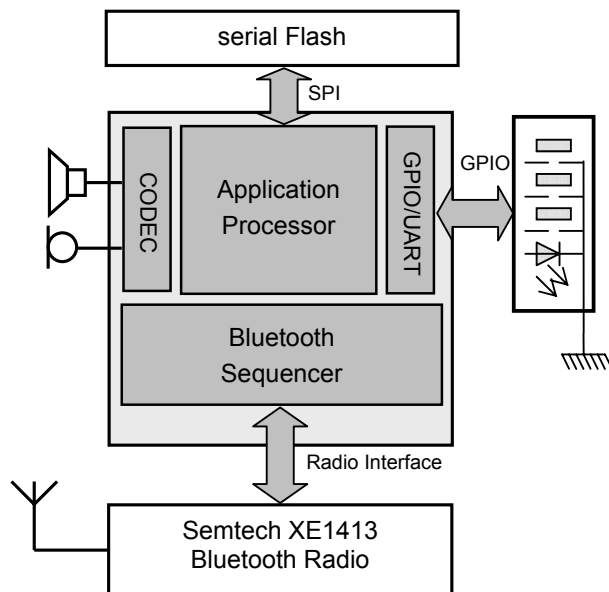
Figure 1 - Bluetooth Headset Application

The on-chip host processor runs the application software and the upper layer Bluetooth protocol stack software while the Bluetooth sequencer handles the low level of the protocol with no intervention by the application processor. This architecture guarantees that the real time operations of the lower levels cannot be influenced by the application. Qualified upper layer Bluetooth protocol software from various 3rd party suppliers can be supplied to run on the SX1441. This system architecture definitely eases the software development and Bluetooth qualification processes and guarantees the highest flexibility. The Bluetooth qualification process for the final application is simplified by the fact that the SX1441 uses a qualified Bluetooth ROM implementation

www.semtech.com

2   SX1441 PINOUT
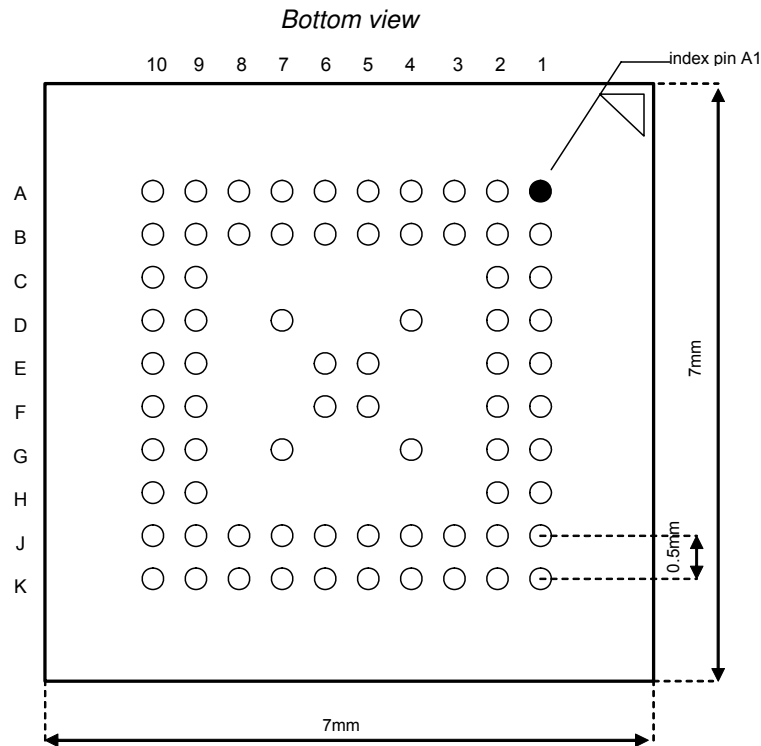
Bottom view

Figure 2 - LFBGA72, bottom view

2.1   PIN DESCRIPTION

Pin	Symbol	Type/ capabilities	Reset	Description	Voltage level
A1	TP0	Do not connect	Do not connect	Test pin	-
A2	TP1	Do not connect	Do not connect	Test pin	-
A3	TP2	Connect to ground	Connect to ground	Test pin	-
A4	PB[1]	D I O ud	D I u	General purpose port B I/O	VDDIO_DIG
A5	PB[3]	D I O ud	D I u	General purpose port B I/O	VDDIO_DIG
A6	PB[5] / UA_RTS	D I O ud	D I u	General purpose port B I/O UART RTS handshaking	VDDIO_DIG
A7	PB[7] / UA_RX	D I O ud	D I u	General purpose port B I/O UART receive signal	VDDIO_DIG
A8	MOSI	D I O u	D O	SPI master Out slave In	VDDIO_DIG
A9	MISO	D I O u	D I u	SPI master In slave Out	VDDIO_DIG
A10	SCK	D I O u	D O	SPI clock	VDDIO_DIG
B1	NRESET	D I u	D I u	Master Reset	VDD_M
B2	VSS_DIG	P	P	Digital core ground	-

Personal Area Network

Pin	Symbol	Type/ capabilities	Reset	Description	Voltage level
B3	PB[0]	D I O ud	D I u	General purpose port B I/O	VDDIO_DIG
B4	PB[2]	D I O ud	D I u	General purpose port B I/O	VDDIO_DIG
B5	PB[4] / UA_CTS	D I O ud	D I u	General purpose port B I/O UART CTS handshaking	VDDIO_DIG
B6	PB[6] / UA_TX	D I O ud	D I u	General purpose port B I/O UART transmit signal	VDDIO_DIG
B7	VSSIO_DIG	P	P	digital pads ground	-
B8	VDDIO_DIG	P	P	digital pads supply voltage	-
B9	NSS[0]	D I O u	D I u	First SPI slave select	VDDIO_DIG
B10	NSS[1]	D I O u	D I u	Second SPI slave select	VDDIO_DIG
C1	VREG_OFF	D O	D O	Internal regulators status	VDDM
C2	VDDBAT	A I	A I	Sensor input for battery end-of-life detection	-
C9	NSS[2]	D I O u	D I u	Third SPI slave select	VDDIO_DIG
C10	NSS[3]	D I O u	D I u	Fourth SPI slave select	VDDIO_DIG
D1	VMIC_P	A I	A I	Microphone positive input	-
D2	VDD_ANA	P	P	Analog core supply voltage	-
D4	DBG[4]	D I O k	D I k	Debug Interface HCI CTS	VDDIO_DIG
D7	DBG[7]	D I O k	D I k	Debug Interface HCI TX	VDDIO_DIG
D9	PA[0]	D I u d	D I u	General purpose port A input	VDDIO_DIG
D10	NSS[4]	D I O u	D I u	Fifth SPI slave select	VDDIO_DIG
E1	VMIC_N	A I	A I	Microphone negative input	-
E2	VREGA	A O	A O	Analog regulated voltage	-
E5	DBG[5]	D I O k	D I k	Debug Interface HCI RTS	VDDIO_DIG
E6	DBG[6]	D I O k	D I k	Debug Interface HCI RX	VDDIO_DIG
E9	PA[2]	D I u d	D I u	General purpose port A input	VDDIO_DIG
E10	PA[1]	D I u d	D I u	General purpose port A input	VDDIO_DIG
F1	VREF	A O	A O	Reference voltage output	-
F2	VDD_M	P	P	Main supply voltage	-
F5	DBG[1]	D I O k	D I k	Debug Interface PCM clock	VDDIO_DIG
F6	DBG[3]	D I O k	D I k	Debug Interface PCM data in	VDDIO_DIG
F9	PA[4]	D I u d	D I u	General purpose port A input	VDDIO_DIG
F10	PA[3]	D I u d	D I u	General purpose port A input	VDDIO_DIG
G1	VSS_M	P	P	Analog ground	-
G2	VREGD	A O	A O	Digital regulated voltage	-

Personal Area Network

Pin	Symbol	Type/ capabilities	Reset	Description	Voltage level
G4	DBG[0]	D I O k	D I k	Debug Interface PCM fsync	VDDIO_DIG
G7	DBG[2]	D I O k	D I k	Debug Interface PCM data out	VDDIO_DIG
G9	PA[6]	D I u d	D I u	General purpose port A input	VDDIO_DIG
G10	PA[5]	D I u d	D I u	General purpose port A input	VDDIO_DIG
H1	PA_OUTP	A O	A O	Power amplifier positive output	VDD_PA
H2	VDD_PA	P	P	Power amplifier supply voltage	-
H9	VDD_DIG	P	P	Digital core supply voltage	-
H10	PA[7]	D I u d	D I u	General purpose port A input	VDDIO_DIG
J1	PA_OUTN	A O	A O	Power amplifier negative output	VDD_PA
J2	TP3	Do not connect	Do not connect	Test pin	-
J3	WAKEUP	D I d	D I d	Chip wake up	VDD_M
J4	SPI_DATA_IN	D I k	D I k	Radio SPI input	VDDIO
J5	VDDIO	P	P	Radio pads supply voltage	-
J6	VSSIO	P	P	Radio pads ground	-
J7	SPI_CLK_OUT	D O	D O	Radio SPI serial clock	VDDIO
J8	SPI_DATA_OUT	D O	D O	Radio SPI data out	VDDIO
J9	SYS_CLOCK_IN	D I	DI	Master clock input	VDDIO
J10	DOC_SDIO	D I O u	D I u	Monitor data I/O	VDDIO_DIG
K1	VSS_PA	P	P	Power amplifier ground	-
K2	TP4	Do not connect	Do not connect	Test pin	-
K3	SLW_CLK_IN	D I k	D I k	32 kHz clock input	VDDIO
K4	RX_DATA	D I k	D I k	Radio RX data	VDDIO
K5	SPI_EN_BAR	D O	D O	Radio SPI select	VDDIO
K6	TX_EN	D O	D O	Radio TX enable	VDDIO
K7	SYNC_DETECT	D O	D O	Radio sync detect	VDDIO
K8	RX_EN	D O	D O	Radio RX enable	VDDIO
K9	TX_DATA	D O	D O	Radio TX data	VDDIO
K10	DOC_SCK	D I u	D I u	Monitor clock	VDDIO_DIG

A : Analog   D : Digital   I : Input   O : Output
u : Internal pull-up   d : Internal pull-down   k : Internal keeper   P : Power

Table 1 – Pin description

SEMTECH

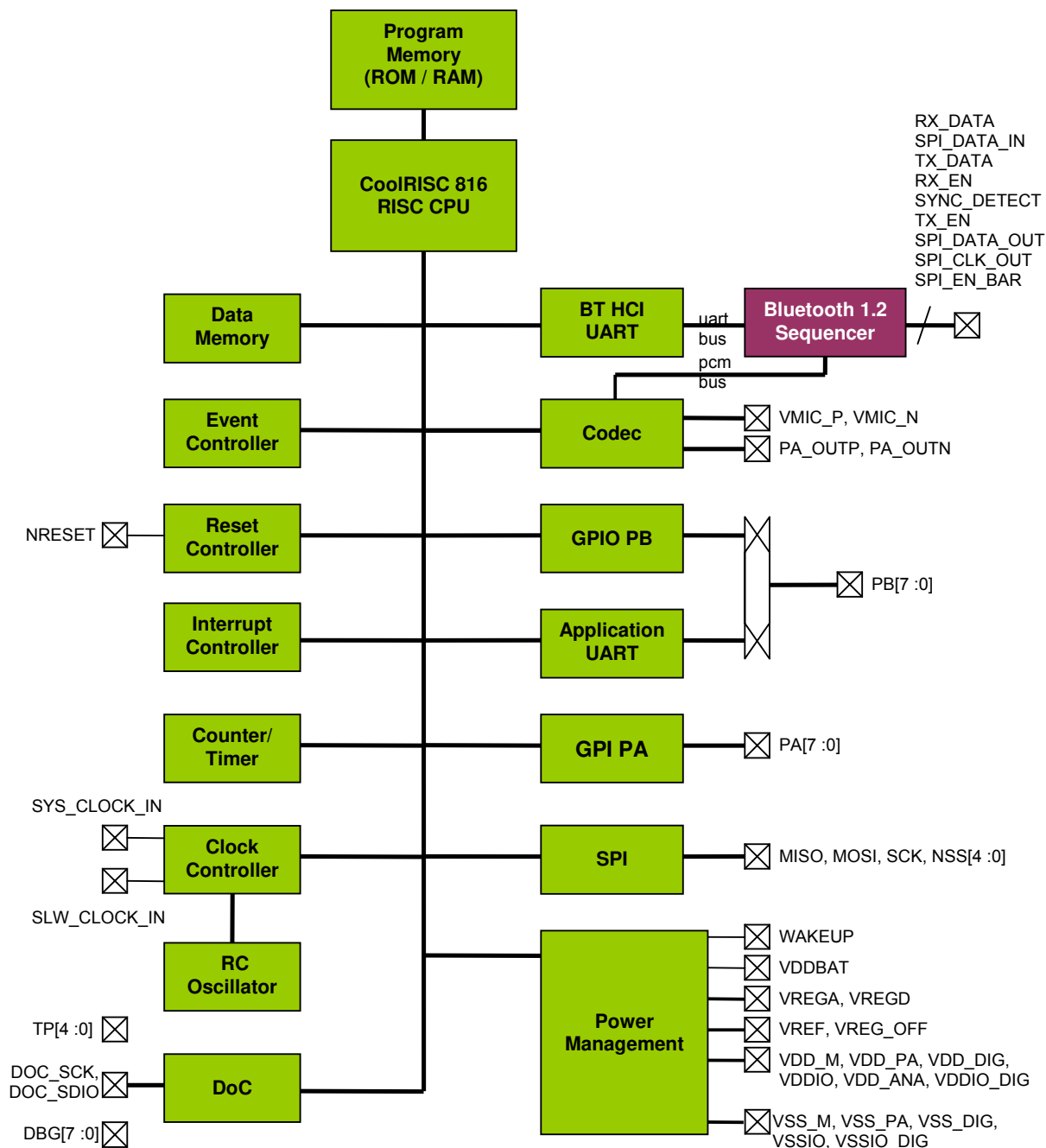# 3   DETAILED FUNCTIONAL DESCRIPTION

3.1   BLOCK DIAGRAM

Figure 3 - SX1441 block diagram

A high-level block diagram of the SX1441 is shown in Figure 3. The CoolRISC$^®$ 816 8-bit RISC processor is optimized for both computation power and energy consumption efficiency. Every instruction executes in one clock cycle. The system frequency can be selected from different possible clock signals. SLW_CLOCK_IN, which is typically 32 kHz, SYS_CLOCK_IN, which is typically 13 MHz, or the internal programmable RC oscillator f_{RC} up to 15 MHz. The program memory consists of; firstly 4k instructions in ROM for the boot code and the debug drivers, and then 40k instructions in RAM dedicated to the application and the upper layers of the Bluetooth protocol stack. The data memory is 8 kbyte RAM. The interrupt and event controllers manage interrupts and events from peripherals and internal timers. The reset controller takes care of the power-on phase. The clock controller selects the processor and peripherals clocks between the internal RC oscillator or the two external clocks.

GPIO's are split into two peripherals: a) port A (PA) is an 8-bit wide input digital port with selectable pull-up and debouncer, which can also be programmed to generate interrupts and resets; and b) port B (PB), an 8-bit wide input/output digital port with selectable pull-up and open-drain capabilities.

The SPI and UART interfaces implement serial communication protocols. The SPI can communicate with up to 5 peripherals, one of them being the serial non-volatile memory storing the application code. The UART has an 8-byte FIFO and supports hardware flow control.

The integrated power management unit generates the regulated supply voltages for the SX1441, thus reducing the number of external components. It also monitors the battery voltage to detect the end-of-life of the battery.

The CODEC is compliant with the Bluetooth audio specifications and integrates a built-in CVSD coder/decoder. The audio samples are transferred directly from the Bluetooth sequencer to the CODEC to reduce the processor load and power consumption. A DMA interface allows transferring of samples directly between the memory and the CODEC.

The Bluetooth sequencer is a complete dedicated Bluetooth co-processor. It implements the lower layers of the Bluetooth protocol stack from the radio interface up to the HCI. It runs independently from the processor and communicates with it through a dedicated internal UART link. This massively simplifies the debugging of the final product and the Bluetooth qualification process since the application cannot disturb the time-critical part of the Bluetooth stack. The Bluetooth sequencer supports all modes of operation (Active, Hold, Sniff, Park, Standby), all packet types, simultaneous operation with up to 7 ACL (data) links and one SCO (audio) link in a point-to-point, piconet, or scatternet network configuration.

The debug-on-chip (DoC) peripheral interfaces the chip with the software debugger.

SEMTECH

3.2 HOST PROCESSOR SYSTEM

3.2.1 CoolRISC 816 CPU

The CPU of the SX1441 is a CoolRISC816, an 8-bit low power RISC core. The instruction set is made up of 35 generic instructions coded on 22 bits and always executed in one clock cycle, including conditional jumps and 8x8 multiplications, thus providing 1 MIPS/MHz. Instructions and data memory are separated (Harvard architecture). The 16 8-bit registers enable the use of a C compiler.

The complete CPU hardware and software description is given in the document "CoolRISC 816, 8-bit Microprocesor Core, Hardware and Software Reference Manual", version 4.5 which can be found on the Semtech website (http://www.semtech.com).
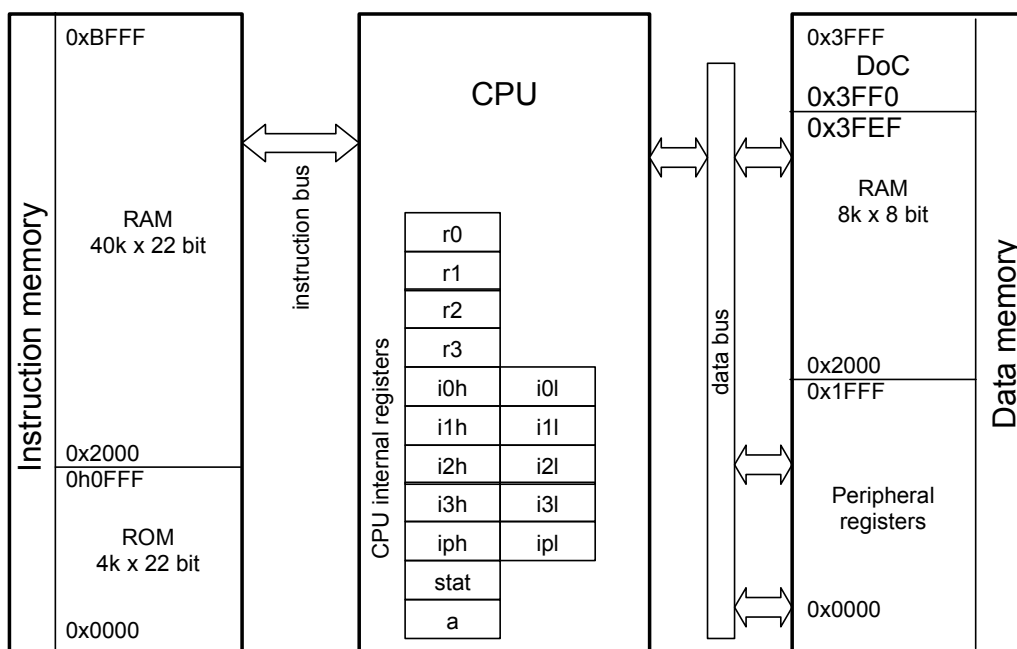
Figure 4 - Memory organization

3.2.2 Program Memory

The instruction memory is composed of both ROM and RAM. The ROM size is 4096 x 22-bit and stores the boot code and the Debug-On-Chip (DoC) driver. The RAM size is 40k instructions which is completely available for the application, except for the last 64 instructions between 0xBFB0 and 0xBFFF which are used by the Debug-on-Chip.

The ROM is located from the address 0x0000 to the address 0x0FFF. The RAM is located in the 0x2000 to 0xBFFF range. Addresses 0x2000 to 0x2004 are jump and interrupt vectors.

Address	Usage	Comment
0x2000	start vector	Usually set to 0x2005. The code actually begins at 0x2005
0x2001	Mid priority interrupt handler	
0x2002	Low priority interrupt handler	
0x2003	High priority interrupt handler	
0x2004	RESERVED	

Table 2 – Jump and interrupt vectors address table

3.2.3 Data Memory

The data memory space is made of 8 kbytes of RAM. The last 16 bytes between 0x3FF0 and 0x3FFF are reserved for the Debug-On-Chip (DoC) interface. The rest of the space from 0x2000 to 0x3FEF is available for the application. The peripheral registers are located in the page 0 of the data memory space.

Block	Address range
System registers (reset controller & clock controller)	0x0010 to 0x001F
Port A registers	0x0020 to 0x0027
Port B registers	0x0028 to 0x002D
Application UART registers	0x0030 to 0x0037
reserved	0x0038 to 0x003B
Event controller registers	0x003C to 0x003F
Interrupt controller registers	0x0040 to 0x0047
Power management unit registers	0x0048 to 0x004C
HCI UART (to/from Bluetooth Sequencer) registers	0x0050 to 0x0057
Counter registers	0x0058 to 0x005F
SPI registers	0x0068 to 0x006F
Bluetooth Sequencer registers	0x007C to 0x007D
Debug Interface (reserved)	0x0080 to 0x009F
Codec registers	0x00E0 to 0x00FF
Data Memory	0x2000 to 0x3FEF
Debug-on-Chip memory (reserved)	0x3FF0 to 0x3FFF

Table 3 - Data memory and registers map

3.3 POWER MANAGEMENT UNIT

3.3.1 Features
- Wide power supply range, VDD_M from 2.2 to 3.6V.
- High current (50 mA) integrated 1.8V regulator to supply the digital core of the SX1441 and external chips, VREGD output.
- Integrated 1.8V analog regulator to supply analog blocks, VREGA output.
- Integrated temperature-compensated voltage reference.
- Battery end-of-life detection, VDDBAT input.
- Mode of operation controller to suppress the need for external power supply switch.
- Ultra low power consumption in OFF mode.

3.3.2 Register Map

Name	Address (Hex)
RegPmgtVrega	0x0048
RegPmgtVregd	0x0049
RegPmgtEol	0x004A

Table 4 - Power management unit register mapping

Pos	RegPmgtVrega	r/w	Reset	Function
7:6	-	r	00	reserved
5	DefaultVrega	rw	1	force analog tuning to default values
4	EnableVrega	rw	0	1 = VREGA voltage regulator switched on 0 = VREGA voltage regulator switched off
3:0	TuneVrega	rw	0011	adjust VREGA value

Table 5 - RegPmgtVrega register

Pos	RegPmgtVregd	r/w	Reset	Function
7	WakeUp	r	0	value of the wakeup pin
6:5	-	r	00	reserved
4	VregdStatus	r	1	1 = VREGD voltage regulator switched on 0 = VREGD voltage regulator switched off
3:2	TuneVregd	rw	00	adjust VREGD value
1	VregdLock	w	1	1 = lock VREGD voltage regulator 0 = shut down VREGD voltage regulator
0	-	r	0	reserved

Table 6 - RegPmgtVregd register

Pos	RegPmgtEol	r/w	Reset	Function
7	EolOk	r	x	0 = VDDBAT pin voltage < EolThreshold 1 = VDDBAT pin voltage ≥ EolThreshold
6	-	r	0	reserved
5	EnableEol	rw	0	1 = battery end-of-life switched on 0 = battery end-of-life switched off
4:0	EolThreshold	rw	00000	adjust battery end-of-life comparator threshold

Table 7 - RegPmgtEol register

3.3.3 Modes of Operation

The power management unit's role is to generate regulated voltages for both internal and the external components such as the non-volatile serial memory and the radio chip. It includes a controller to switch on/off all voltage regulators when needed in order to reduce power consumption. Three modes of operation are defined (see Figure 6):

- **OFF mode**: all internal power supplies are shut down. Power consumption is very low, typically a few micro-amps.
- **ON mode**: all blocks except the CODEC are powered. The application is running and a Bluetooth connection may be active. The chip enters this state when the WAKEUP input is set high (see Figure 5), and leaves this mode under software control, when requested by the application. In the ON mode, the pin VREGD outputs 1.8V and the pin VREGA is floating.
- **AUDIO mode**: all blocks are powered. It is entered upon request from the application. In the AUDIO mode, the pins VREGA and VREGD output 1.8V.
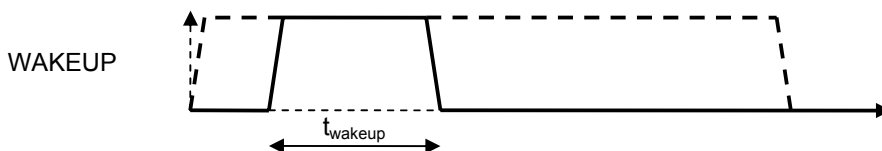
Figure 5 - WAKEUP timing diagram
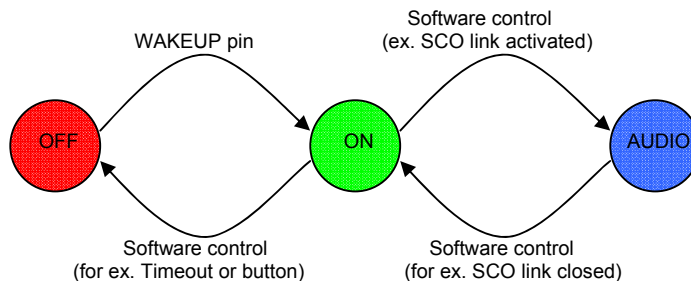
Figure 6 - SX1441 power management modes
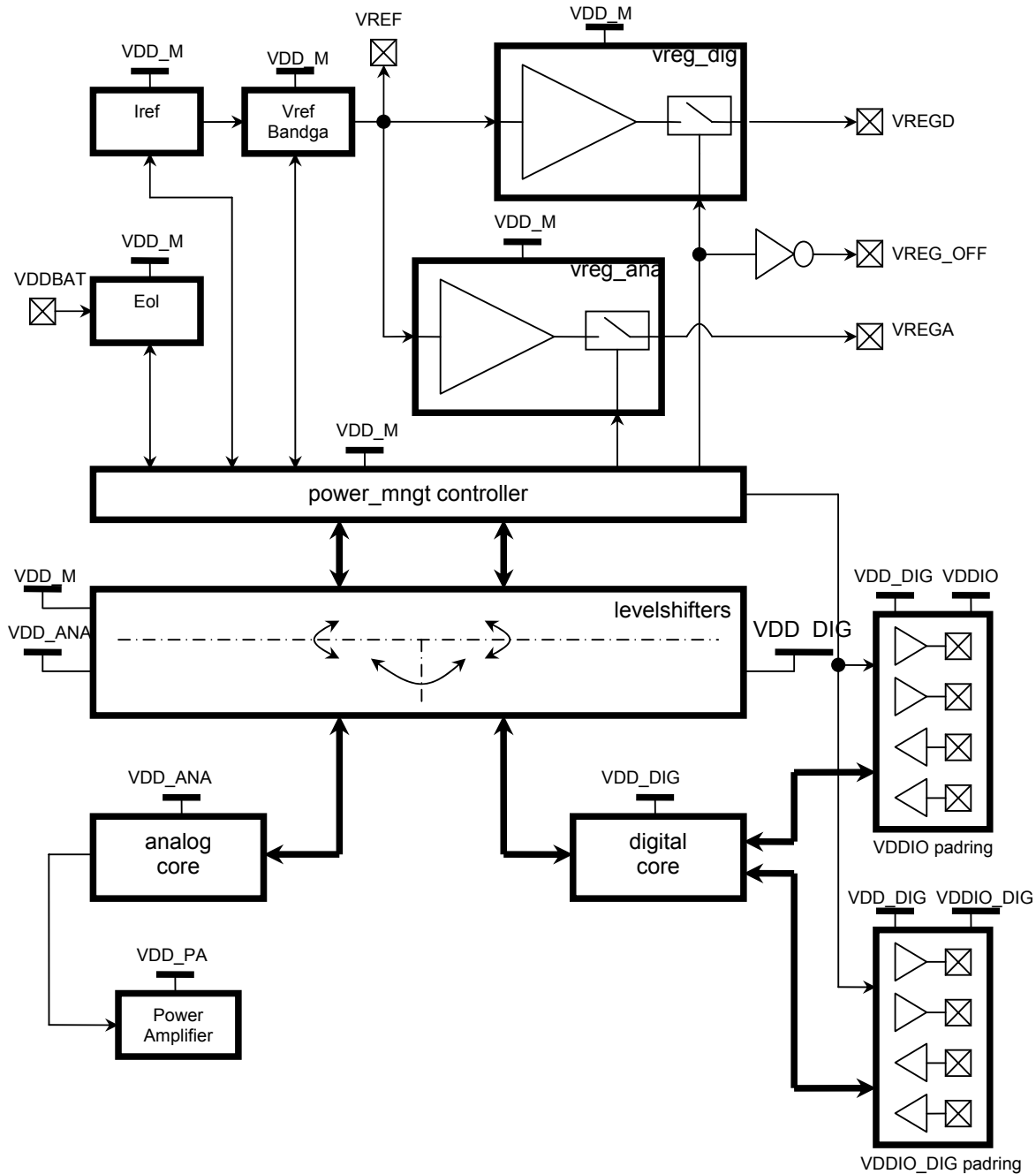
3.3.4 Block Diagram

Figure 7 - Power management unit block diagram

The main power supply is VDD_M. It powers the power management unit and some I/O pads. The power management unit generates the VREGD and VREGA regulated voltages. VREGD is usually used to supply the digital core, through the VDD_DIG pin, and external components such as a serial non-volatile memory and the radio chip. VREGA is usually used to supply the internal analog blocks, through the pin VDD_ANA. It may also be used to power an external microphone.

VDDIO is the power supply for the radio interface. If the radio chip is powered by VREGD, then VDDIO should be connected to VREGD as well. VDDIO_DIG is the power supply for most of the digital pads. Depending on the application, it may be connected to VREGD, VDD_M, or any other power supply which fulfills the specifications.

VDD_M should be decoupled with a capacitor C_{VDD_M} for best performances. VREGD has to be connected to an external capacitor C_{VREGD} to insure the stability and the performance of the voltage regulator. VREGA has to be connected to an external capacitor C_{VREGA} to insure the stability and the performance of the voltage regulator. VREF is connected to an external capacitor C_{VREF}. VDD_PA can be connected to VREGD.

3.3.5 Regulators Specifications, External Components

Symbol	Description	Min	Typ	Max	Unit	Comments
V_{REGA}	Analog regulated output voltage	1.62	1.8	1.98	V	I_load=1mA
V_{REGD}	Digital regulated output voltage	1.62	1.8	1.98	V	I_load=50mA
I_{REGA}	Output current on VREGA			10	mA	Recommended max. load
I_{REGD}	Output current on VREGD			50	mA	Recommended max. load

Note : Values above are specified across temperature range and for VDD_M > 2.2V unless otherwise specified

Table 8 - On-chip voltage regulators specifications

Symbol	Value
C_{VREGD}	4.7 uF
C_{VREGA}	1 uF
C_{VREF}	1 uF
C_{VDD_M}	1 uF

Table 9 - Typical external components

Capacitors should be added to decouple VDD_PA, VDD_DIG, VDD_ANA, VDDIO, and VDDIO_DIG, as a common practice.

3.3.6 Battery End-Of-Life (EOL)
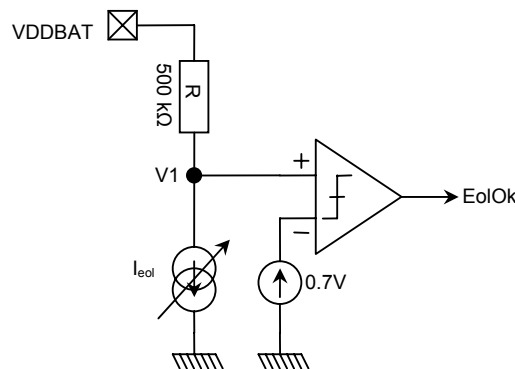
Figure 8 - Battery end-of-life structure

The battery end-of-life circuit structure is described in Figure 8. A voltage is created by drawing a constant current I_{eol} from the pin VDDBAT through the internal resistor R, and is compared with a voltage reference. The bit **EolOk** of the register **RegPmgtEol** is directly the output of the comparator. The EolOk is set to "1" whenever the voltage at VDDBAT is higher or equal to the threshold voltage $V_{EOLThreshold}$. This threshold voltage of the comparator is given by the Equation 1. For cThe start up time of the end-of-life circuit is $T_{EOLstart}$. The response time to a change on VDDBAT is T_{EOLres}.

$$V_{EOLThreshold} = V_{EOLref} + V_{EOLstep} \cdot \sum_{i=0}^{4} 2^i \cdot EolThreshold[i]$$

Equation 1 - Threshold voltage of the EOL comparator

Symbol	Parameter	Min	Typ	Max	Unit	Comment
V_{EOLref}	EOL reference voltage	0.710	0.725	0.740	V	@ VDD_M=3V, 25°C, (bandgap test)
$V_{EOLstep}$ (*)	Threshold tuning step	40	45	50	mV	@ VDD_M=3V, 25°C
EOLThreshold	EOLthreshold offset setting	0.710		2.34	V	Tested at VBAT=1.8V. and 0x31 and 0x3F register settings
$T_{EOLstart}$ (*)	start-up time			100	µs	
T_{EOLres} (*)	time response			20	µs	

Note1 : Values above are specified across temperature range and for VDD_M > 2.2V unless otherwise specified
Note2 : Values marked with asterisks are not production tested and guaranteed by design.

Table 10 - End-of-life analog specifications

3.4   RESET CONTROLLER

3.4.1 Features
- Handles different reset sources: power-on-reset, NRESET pin, BusError, Watchdog, and port PA
- Power-on-reset/Brownout detector without external components
- Programmable watchdog timer
- Reset can be triggered by NRESET pin

3.4.2 Register Map

Name	Address (Hex)
RegSysCtrl	0x0010
RegSysWd	0x0014

Table 11 - Reset controller registers

Pos	RegSysCtrl	r/w	Reset	Function
7	reserved	rw	0	Bit reserved for test purpose
6	-	r	0	reserved
5	EnableBusError	rw	0	1 = BusError reset is enabled 0 = BusError reset is disabled
4	EnableResetWD	rw	0	1 = Watchdog reset is enabled 0 = Watchdog reset is disabled
3:0	-	r	0000	reserved

Table 12 - RegSysCtrl register

Pos	RegSysWd	r/w	Reset	Function
7:4	-	r	0000	reserved
3:0	WDKey	rw	0000	Watchdog key

Table 13 - RegSysWd register

3.4.3 Power-On-Reset / Brownout Detector

The power-on-reset monitors both VDD_M and VDD_DIG. Upon start-up, when both voltages reach a level sufficient to ensure correct circuit behavior, the internal reset signal is released. Then, if during operations the supply voltage drops below the specified threshold (see

Note1 : Values above are specified across temperature range unless otherwise specified
Note2 : Values marked with asterisks are not production tested and guaranteed by design.

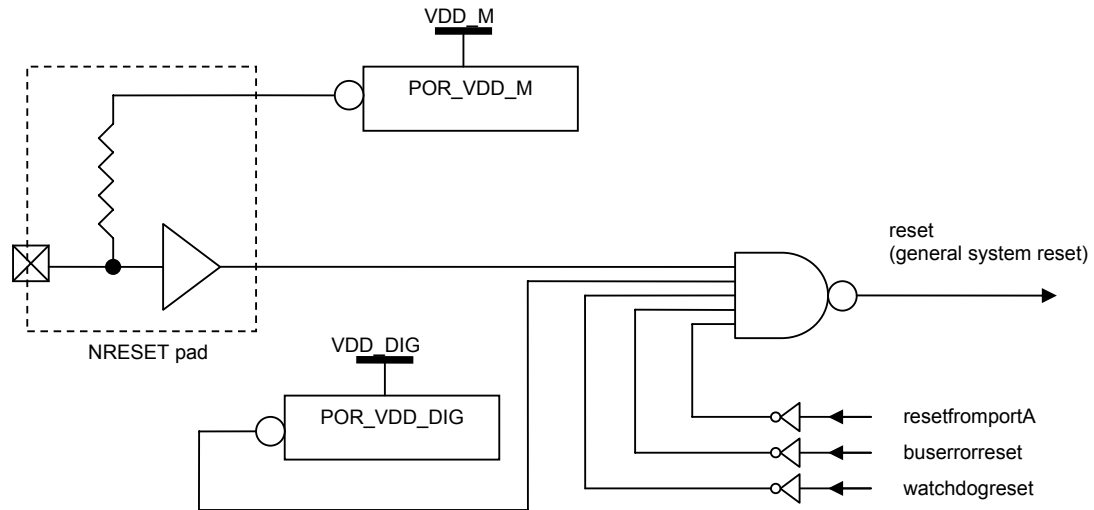Table 14), the circuit goes into a reset mode.

Figure 9 – POR, NRESET, and reset circuitry

The output of POR_VDD_M controls the pull resistor of the NRESET pad. If the NRESET pad is left unconnected (recommended) the POR_VDD_M is propagated into the system. Otherwise, the internal nreset_system signal may be activated by connecting the NRESET pad to the ground. The NRESET pad is active low.
The POR_VDD_M insures that VDD_M is stable so that the power management unit can operate safely. The POR_VDD_DIG insures that VDD_DIG is correct so that the digital core can start.

3.4.4 Bus Error

The address space is assigned as shown in the memory map in Table 3. If the bit EnableBusError is set in the register **RegSysCtrl** and an unused address is accessed by the processor, then a reset is generated.

3.4.5 Watchdog

Once enabled by setting the bit **EnableResetWD** of the **RegSysCtrl** register, a counter will be started and a reset condition (watchdogreset, Figure 9) will be generated when the counter reaches its maximum value, unless the counter is cleared by software. The counter is 3-bit wide and is clocked by the ck2Hz output of the low prescaler. Its period is typically around 4 seconds but will depend on the clock controller configuration. The watchdog is cleared by writing consecutively the values 0x0a and 0x03 in the **RegSysWd** register.
In assembler, the sequence will look like:
move RegSysWd, #0x0a
move RegSysWd, #0x03

Only writing 0x0a followed by 0x03 will clear the watchdog. If some other writing is done in and between, in **RegSysWd**, then the watchdog will not be cleared.
The status of the watchdog may be checked by reading the register **RegSysWd**. The watchdog is a four bit counter with a range of 0 to 7. The reset is generated when the counter reaches the value 8.

3.4.6 Analog Reset Specifications
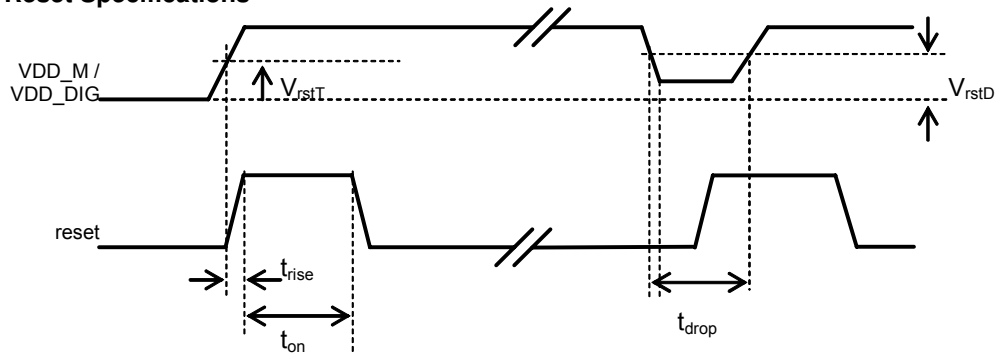
Figure 10 – Power-On / Brownout reset conditions

POR	Symbol	Description	Min	Max	Unit
VDD_M supervision	V_{rstT}	Start Voltage	0.8	1.5	V
	V_{rstD} (*)	Drop Voltage	0.8	1.5	V
	t_{on} (*)	Reset Time	-	300	µs
	t_{rise} (*)	Rise Time	-	15	µs
	t_{drop} (*)	Drop Time	6.0	-	µs
VDD_DIG supervision	V_{rstT}	Start Voltage	0.8	1.5	V
	V_{rstD} (*)	Drop Voltage	0.8	1.5	V
	t_{on} (*)	Reset Time	-	300	µs
	t_{rise} (*)	Rise Time	-	15	µs
	t_{drop} (*)	Drop Time	6.0	-	µs

Note1 : Values above are specified across temperature range unless otherwise specified
Note2 : Values marked with asterisks are not production tested and guaranteed by design.

Table 14 - POR specifications

3.5   CLOCK DISTRIBUTION UNIT

3.5.1 Features
- On-chip RC oscillator
- Three available clock sources: RC oscillator, SYS_CLOCK_IN pin, SLW_CLOCK_IN pin
- Two divider chains: high-prescaler (8 bits) and low-prescaler (15 bits).
- CPU clock disabled in halt mode.

3.5.2 Register Map

Name	Address (Hex)
RegSysClock	0x0012
RegSysMisc	0x0013
RegSysPre0	0x0015
RegSysRcTrim1	0x001B
RegSysRcTrim2	0x001C

Table 15 – Clock distribution registers addresses

Pos	RegSysClock	r/w	Reset	Function

Pos	RegSysClock	r/w	Reset	Function
7	CpuSel	rw	0	1 = Low Speed Clock Selected (generally: an external 32kHz clock crystal) 0 = High Speed Clock Selected (the nature of the clock selected will depend on the EnableSysClk bit value).
6	SelLowPresIn	rw	0	1 = Force the SLW_CLOCK_IN clock as the low prescaler input when a low speed clock is available (i.e. EnableSlwClock bit). Otherwise the high prescaler is selected. 0 = Select the SLW_CLOCK_IN clock as the low prescaler input when a low speed clock is available (i.e. EnableSlwClock bit) and the ckRC clock has been selected as the High Speed Clock (i.e. EnableSysClk bit).
5	EnableSysClk	rw	0	1 = SYS_CLOCK_IN clock is selected 0 = ckRC clock is selected
4	-	r	0	reserved
3	ColdSlwClock	r	1	Flag determining when the low speed clock starting phase is finished: 1 = SLW_CLOCK_IN still on the starting phase (32768 cycles) 0 = SLW_CLOCK_IN starting phase finished
2	-	r	0	reserved
1	EnableSlwClock	rw	0	Should be set to '1' when SLW_CLOCK_IN is available, '0' otherwise.
0	EnableRC	rw	1	1 = enable ckRC 0 = disable ckRC

Table 16 - RegSysClock register

Pos	RegSysMisc	r/w	Reset	Function
7:4	-	r	0000	reserved
3	reserved	rw	0	reserved
2	reserved	rw	0	reserved
1	OutputCk32kHz	rw	0	output ck32kHz on pad PB[3]
0	OutputCkCpu	rw	0	output CkCpu on pad PB[2]

Table 17 - RegSysMisc register

Pos	RegSysPre0	r/w	Reset	Function
7:2	-	r	000000	reserved
1	reserved	r	0	reserved
0	ResPre	w	0	1 = reset the low prescaler

Table 18 - RegSysPre0 register

Pos	RegSysRcTrim1	r/w	Reset	Function
7:5	-	r	000	reserved
4:2	RCDivFactor	rw	000	Divide RC frequency by $2^{RcDivFactor}$
1:0	RCCoarseMSB	rw	01	RC coarse adjustment (MSB)

Table 19 - RegSysTrim1 register

Pos	RegSysRcTrim2	r/w	Reset	Function
7:6	-	r	00	reserved
5:4	RCCoarseLSB	rw	00	RC coarse adjustment (LSB)

1:0	RCFine	rw	0000	RC fine adjustment

Table 20 - RegSysTrim2 register

3.5.3 RC Oscillator

The RC oscillator is always turned on and selected for CPU and system operation after a power-on reset or a negative pulse on pad NRESET. It can be deselected after the SYS_CLOCK_IN or the SLW_CLOCK_IN has been started and selected as system clock.

The **EnableRC** bit in the register **RegSysClock** controls the signal from the RC oscillator. The user can disable the RC oscillator clock signal by resetting the bit **EnableRC**.

The RC oscillator frequency is trimmed with the registers **RegSysRcTrim1** and **RegSysRcTrim2**. The absolute value of the frequency for a given register content may change from chip to chip due to process tolerances. However, the modification of the frequency as a function of a modification of the register content is fairly precise. The RC oscillator output frequency, f_{RC}, is obtained by the following trimming rule:

$$f_{RC} = fo \cdot \frac{1}{2^{RCDivFactor}} \cdot \left(1 + (RCCoarse - 8) \cdot CoarseStep + RCFine \cdot FineStep\right)$$

Equation 2 - RC oscillator clock frequency

The
Note : Values marked with asterisks are not production tested and guaranteed by design.

Table 21 summarizes the characteristics of the oscillator.

Symbol	Description	Min	Typ	Max	Unit
f_0 [*]	Internal oscillator frequency	5.5	8.25	11	MHz
FineStep [*]	Fine tuning step	-	0.5		%
CoarseStep [*]	Coarse tuning step	-	7		%

Note : Values marked with asterisks are not production tested and guaranteed by design.

Table 21 – RC oscillator specifications

<u>Important note</u>: the system is not guaranteed to operate properly with a frequency f_{RC} greater than 14 MHz. Setting the RC oscillator over this limit may produce unpredictable results.

3.5.4 SLOW_CLOCK_IN

SLW_CLOCK_IN must be present and conform to the Bluetooth specifications if the Bluetooth sequencer deep-sleep mode is used. It is typically generated by the XE1413 radio chip. Its frequency is 32'000 Hz or 32'768 Hz.

3.5.5 SYS_CLOCK_IN

It is used by the Bluetooth sequencer and the Codec. Its frequency must be 13 MHz with a tolerance of ± 20 ppm. SYS_CLOCK_IN is typically generated by the XE1413 radio chip.

3.5.6 Clock Source Selection

Different clock sources can be selected independently for the application processor and the reset of the system. The clock of the Bluetooth sequencer is hard-coded and can not be chosen by the user.

The RC clock is always selected after power-up or a negative pulse on the NRESET pin. The CPU clock selection is done with the register **RegSysClock** according to the Table 22. Switching from one clock source to another is glitch free. See also Figure 11, Figure 12, and Figure 13.

Personal Area Network

Clock Sources					Clock Targets			
Mode name	EnableSysClock	EnableRC	EnableSlwClock	SelLowPresIn	CpuCk		High prescaler clock input	Low prescaler clock input
					CpuSel = 0	**CpuSel** = 1		
SlwClock	0	0	1	1	SLW_CLOCK_IN	SLW_CLOCK_IN	Off	On
RC	0	1	0	0	ckRC	high prescaler output	ckRC	high prescaler output
RC + SlwClock	0	1	1	1	ckRC	SLW_CLOCK_IN	ckRC	SLW_CLOCK_IN
SysClock	1	0	0	0	SYS_CLOCK_IN	high prescaler output	SYS_CLOCK_IN	high prescaler output
SysClock + SlwClock	1	0	1	1	SYS_CLOCK_IN	SLW_CLOCK_IN	SYS_CLOCK_IN	SLW_CLOCK_IN

Table 22 – SX1441 Clock configuration

Switching from one clock to one other and stopping the unused clock must be performed in three MOVE instructions to **RegSysClock**. First enable the new clock, then select the CPU clock, and finally stop the unused clock. Combining the different operations in one instruction may cause system malfunction.

3.5.7 RegSysMisc Description
When OutputCk32kHz is 1, the ck32kHz clock is output of the port B PB[3]. The CPU clock is output on the port B PB[2] when the bit OutputCkCpu is 1.

3.5.8 Prescalers
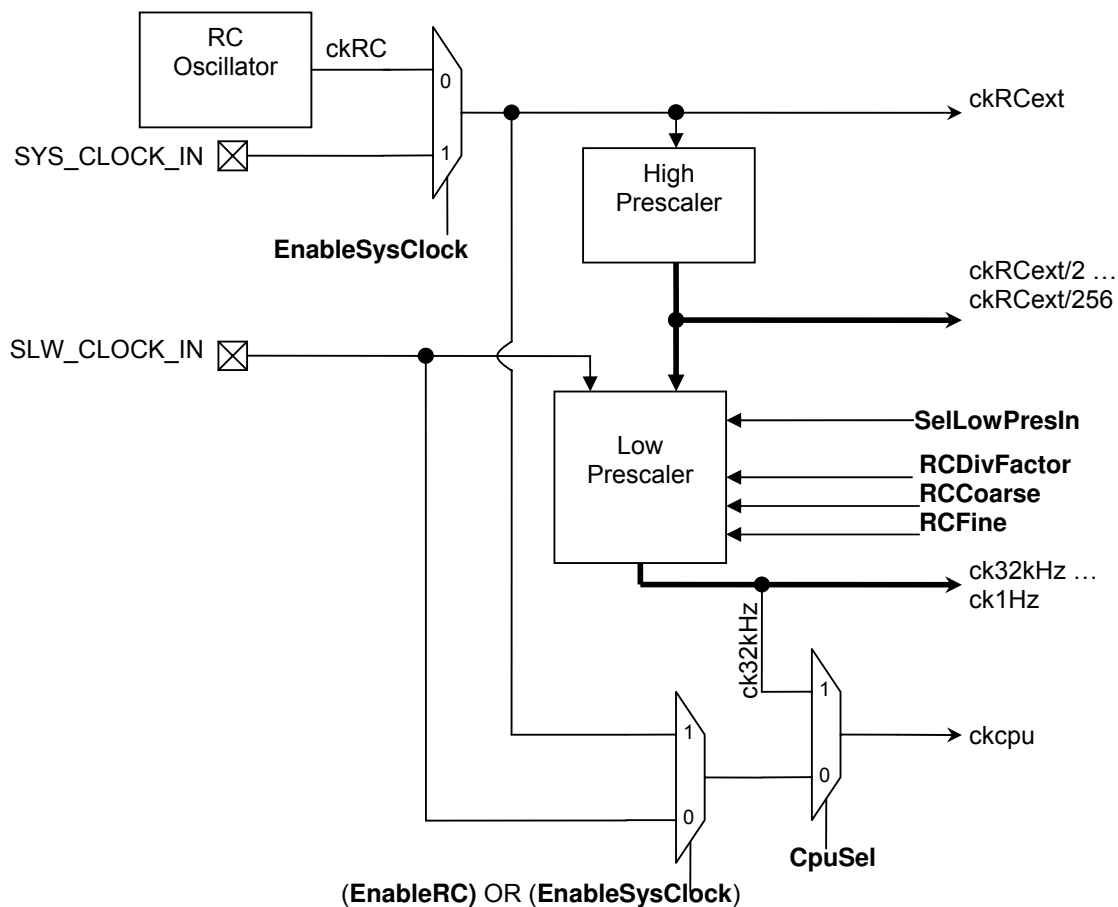The Figure 11 describes the overall structure of the prescaler.

Figure 11 - Prescaler Unit block diagram

3.5.8.1   High Prescaler

The high prescaler is made up of an 8-stage dividing chain. It can be driven with the RC oscillator clock or the SYS_CLOCK pin, depending on the **EnableSysClock** parameter.
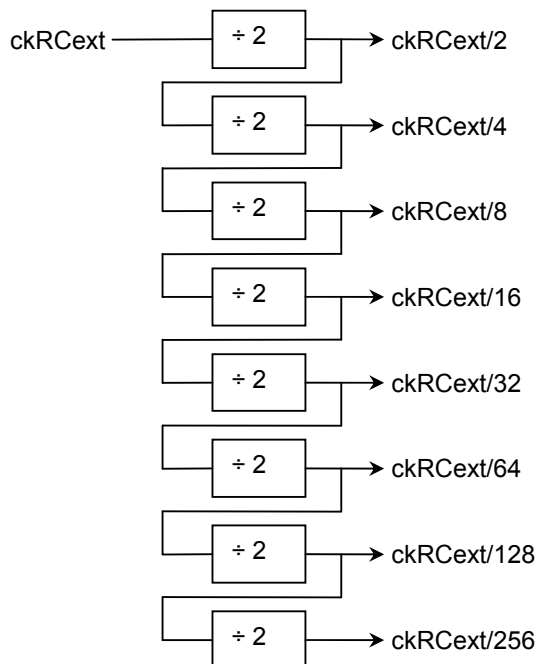

Figure 12 - High prescaler block diagram

The Table 23 summarizes which peripherals use the outputs of the high prescaler. Since each stage of the high prescaler divides the frequency by 2, the frequency of all the outputs of the high prescaler is proportional to the frequency of ckRCext.

High prescaler output	Peripherals
ckRCext	application UART, Bluetooth UART, SPI, counter/timer, port PA
ckRCext/2	application UART, Bluetooth UART
ckRCext/4	application UART, Bluetooth UART, SPI, counter/timer
ckRCext/8	application UART, Bluetooth UART, SPI
ckRCext/16	application UART, Bluetooth UART, SPI
ckRCext/32	application UART, Bluetooth UART
ckRCext/64	application UART, Bluetooth UART
ckRCext/128	application UART, Bluetooth UART

Table 23 - High prescaler outputs usage

3.5.8.2   Low Prescaler

The low prescaler can be driven from one of the high prescaler outputs ckRCext/2 to ckRCext/128 or directly with the SLW_CLOCK_OUT pin when the bit **EnableSlwClock** is set to 1 and bit **EnableSysClock** is reseted to 0. The bit **ResPre** in the register **RegSysPre0** synchronously resets the low prescaler. The low prescaler is also automatically cleared when the bit **EnableSlwClock** is set to 1. The bit **ColdSlwClock** value is 1 to indicate that the SLW_CLOCK_IN is in its starting phase. It automatically enters this phase when the bit **EnableSlwClock** is set to 1. During this phase, SLW_CLOCK_IN is not available. It becomes available after 32'768 cycles, when the bit **ColdSlwClock** returns to 0.
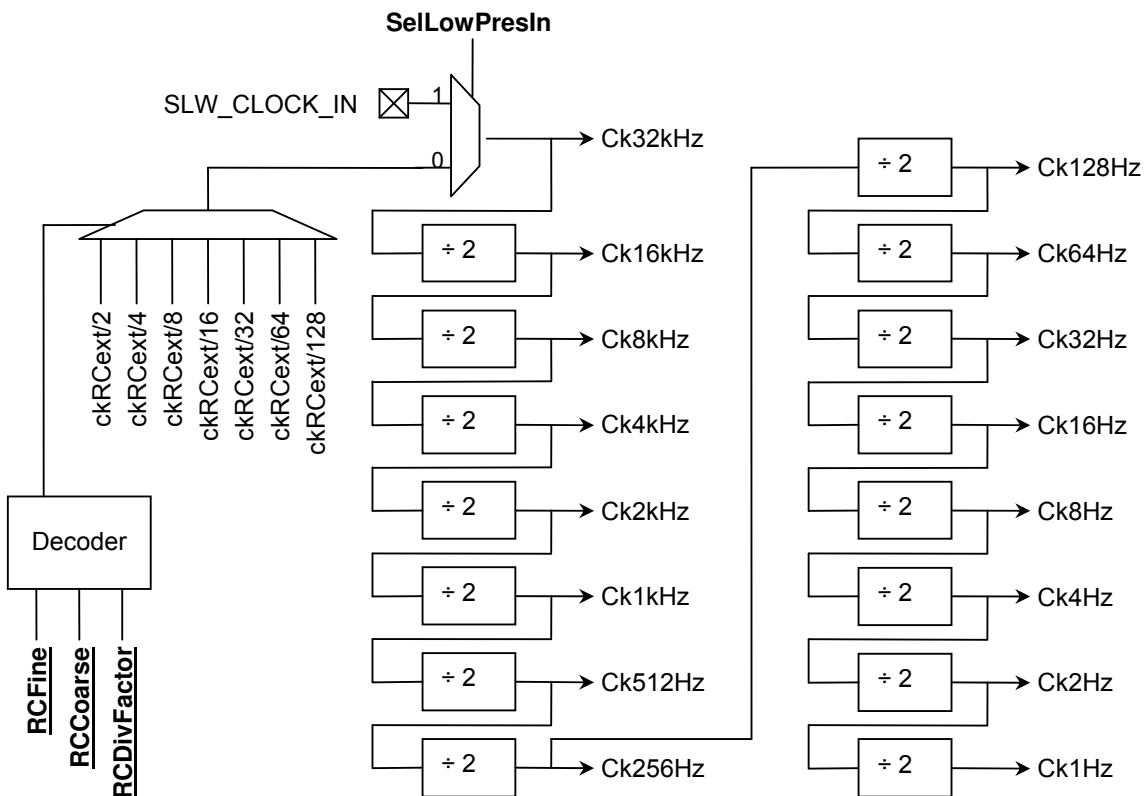
Figure 13 - Low prescaler block diagram

The high prescaler output may be used as the low prescaler input. A decoder is used to select from the high prescaler the frequency tap that is the closest to 32 kHz to operate the low prescaler when SLW_CLOCK_IN is not running. In this case, the RC oscillator frequency will also be valid for the low prescaler frequency outputs.

The Table 24 shows how the RC trimming values in the **RegSysRcTrim1** and **RegSysRcTrim2** registers are decoded to select the input frequency from the high prescaler. The least significant bits of the **RCFine** word are ignored.

In order to ensure the correct frequency selection for the low prescaler with an external clock, a proper value must be set in the RC trim registers. If the frequency is not set correctly, all timings derived from the low prescaler will be shifted accordingly (e.g. watchdog and interrupt frequencies).

In the Table 24, ckRCext stands for either ckRC or SYS_CLOCK_IN.

RCDivFactor & RCCoarseMSB & RCCoarseLSB & RCFine	Selected high prescaler tap	RCDivFactor & RCCoarseMSB & RCCoarseLSB & RCFine	Selected high prescaler tap
[0x0000]hex	ckRCext / 64	[0x04c8]hex	ckRCext / 32
[0x0002]hex	ckRCext / 128	[0x04d0]hex	ckRCext / 16
[0x0100]hex	ckRCext / 32	[0x04d6]hex	ckRCext / 32
[0x0102]hex	ckRCext / 64	[0x04e0]hex	ckRCext / 16
[0x010a]hex	ckRCext / 128	[0x04e5]hex	ckRCext / 32
[0x0110]hex	ckRCext / 64	[0x04f0]hex	ckRCext / 16
[0x0119]hex	ckRCext / 128	[0x04f3]hex	ckRCext / 32
[0x0120]hex	ckRCext / 64	[0x0500]hex	ckRCext / 2
[0x0127]hex	ckRCext / 128	[0x0502]hex	ckRCext / 4
[0x0130]hex	ckRCext / 64	[0x050a]hex	ckRCext / 8

Personal Area Network

RCDivFactor & RCCoarseMSB & RCCoarseLSB & RCFine	Selected high prescaler tap	RCDivFactor & RCCoarseMSB & RCCoarseLSB & RCFine	Selected high prescaler tap
[0x0135]hex	ckRCext / 128	[0x0510]hex	ckRCext / 4
[0x0140]hex	ckRCext / 64	[0x0519]hex	ckRCext / 8
[0x0144]hex	ckRCext / 128	[0x0520]hex	ckRCext / 4
[0x0150]hex	ckRCext / 64	[0x0527]hex	ckRCext / 8
[0x0152]hex	ckRCext / 128	[0x0530]hex	ckRCext / 4
[0x0160]hex	ckRCext / 64	[0x0535]hex	ckRCext / 8
[0x0161]hex	ckRCext / 128	[0x0540]hex	ckRCext / 4
[0x0200]hex	ckRCext / 16	[0x0544]hex	ckRCext / 8
[0x0202]hex	ckRCext / 32	[0x0550]hex	ckRCext / 4
[0x020a]hex	ckRCext / 64	[0x0552]hex	ckRCext / 8
[0x0210]hex	ckRCext / 32	[0x0560]hex	ckRCext / 4
[0x0219]hex	ckRCext / 64	[0x0561]hex	ckRCext / 8
[0x0220]hex	ckRCext / 32	[0x058e]hex	ckRCext / 16
[0x0227]hex	ckRCext / 64	[0x0590]hex	ckRCext / 8
[0x0230]hex	ckRCext / 32	[0x059d]hex	ckRCext / 16
[0x0235]hex	ckRCext / 64	[0x05a0]hex	ckRCext / 8
[0x0240]hex	ckRCext / 32	[0x05ab]hex	ckRCext / 16
[0x0244]hex	ckRCext / 64	[0x05b0]hex	ckRCext / 8
[0x0250]hex	ckRCext / 32	[0x05b9]hex	ckRCext / 16
[0x0252]hex	ckRCext / 64	[0x05c0]hex	ckRCext / 8
[0x0260]hex	ckRCext / 32	[0x05c8]hex	ckRCext / 16
[0x0261]hex	ckRCext / 64	[0x05d0]hex	ckRCext / 8
[0x028e]hex	ckRCext / 128	[0x05d6]hex	ckRCext / 16
[0x0290]hex	ckRCext / 64	[0x05e0]hex	ckRCext / 8
[0x029d]hex	ckRCext / 128	[0x05e5]hex	ckRCext / 16
[0x02a0]hex	ckRCext / 64	[0x05f0]hex	ckRCext / 8
[0x02ab]hex	ckRCext / 128	[0x05f3]hex	ckRCext / 16
[0x02b0]hex	ckRCext / 64	[0x0600]hex	ckRCext / 1
[0x02b9]hex	ckRCext / 128	[0x0602]hex	ckRCext / 2
[0x02c0]hex	ckRCext / 64	[0x060a]hex	ckRCext / 4
[0x02c8]hex	ckRCext / 128	[0x0610]hex	ckRCext / 2
[0x02d0]hex	ckRCext / 64	[0x0619]hex	ckRCext / 4
[0x02d6]hex	ckRCext / 128	[0x0620]hex	ckRCext / 2
[0x02e0]hex	ckRCext / 64	[0x0627]hex	ckRCext / 4
[0x02e5]hex	ckRCext / 128	[0x0630]hex	ckRCext / 2
[0x02f0]hex	ckRCext / 64	[0x0635]hex	ckRCext / 4
[0x02f3]hex	ckRCext / 128	[0x0640]hex	ckRCext / 2
[0x0300]hex	ckRCext / 8	[0x0644]hex	ckRCext / 4
[0x0302]hex	ckRCext / 16	[0x0650]hex	ckRCext / 2
[0x030a]hex	ckRCext / 32	[0x0652]hex	ckRCext / 4
[0x0310]hex	ckRCext / 16	[0x0660]hex	ckRCext / 2
[0x0319]hex	ckRCext / 32	[0x0661]hex	ckRCext / 4
[0x0320]hex	ckRCext / 16	[0x068e]hex	ckRCext / 8
[0x0327]hex	ckRCext / 32	[0x0690]hex	ckRCext / 4
[0x0330]hex	ckRCext / 16	[0x069d]hex	ckRCext / 8
[0x0335]hex	ckRCext / 32	[0x06a0]hex	ckRCext / 4
[0x0340]hex	ckRCext / 16	[0x06ab]hex	ckRCext / 8
[0x0344]hex	ckRCext / 32	[0x06b0]hex	ckRCext / 4
[0x0350]hex	ckRCext / 16	[0x06b9]hex	ckRCext / 8
[0x0352]hex	ckRCext / 32	[0x06c0]hex	ckRCext / 4

www.semtech.com